조합논리회로 설계

(Summary)

Combinational Logic Design

Honam University

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Outline

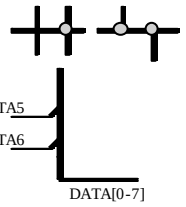
- Documentation Standard for Digital System.
- Digital Circuit Timing and Propagation Delay
- Combinational Logic Design Structure :
  - Decoder
  - Encoder
  - Three-State Buffer
  - Multiplexer
  - Demultiplexer
  - Exclusive-OR Gates
  - Parity Circuit
  - Comparator
  - Adder/ Subtractor
  - Arithmetic Logic Unit (ALU)

DocumentationStandard

- Documentation of a digital system should provide the necessary information for building, testing, operating, and maintaining the system.
- Documentation include:
  1. Block Diagram : showing the inputs, outputs, the main building blocks (modules) of the system and how they are connected.
  2. Schematic Diagram : showing all the components, their types, and all interconnections.
  3. Timing Diagram : showing the logic signals as a function of time.
  4. Structured Logic Description : the operation of the Structure.
     - Example
       - Function Table of multiplexer, Program Listing of PLD (Programmable Logic Device).
  5. Circuit Description : explaining of the operation of the logic circuit.

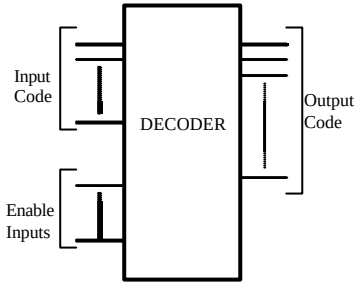
Drawing Layout

- Inputs to the left, outputs to the right.
- Signals flow from left to right.
- Signal paths should be connected.
- Broken signal paths should be flagged to indicate the source or destination and direction.
- Crossing Lines/Connected Lines (T-type connection)
- Buses should be named : DATA[0-7], CONTROL
- A signal extracted from a bus should be named
- Bus Flags : - Unidirection
  - Bidirection
- Multiple Pages Schematic:
  - Flat Structure.
  - Hierarchical Structure.



Decoder

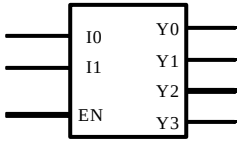
- Multiple-input/Multiple-output device.
- Converts input code into output code.
- Input Codes :
  - Binary Code
  - Gray Code
  - BCD Code
  - Your Code ..



Binary Decoder

- n-to-2^n Decoder : n inputs and 2^n outputs.
- Input code : Binary Code.
- Output code : 1-out-of-2^n, One output is asserted for each input code.
- Example : n=2, 2-to-4 Decoder

Inputs			Outputs			
EN	I1	I0	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

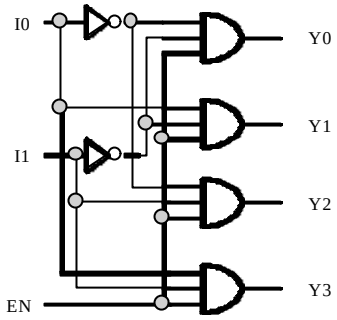


- Logic Diagram

Logic Diagram of 2-to-4 Decoder

1 of 4 Decoder

- Y0 = I0'I1'EN
- Y1 = I0 I1'EN
- Y2 = I0'I1 EN
- Y3 = I0 I1 EN

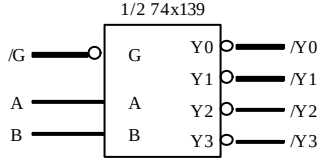


74x139 : 1 of 4 Decoder

- Active Low Enable, Active Low Outputs
- Truth Table

Inputs			Outputs			
/G	B	A	Y3	Y2	Y1	Y0
1	x	x	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

Logic Symbol

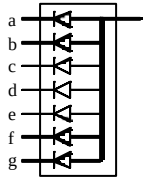


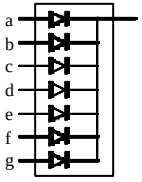
74x138 1 of 8 Decoder

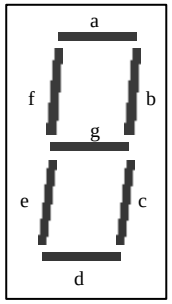
Inputs						Outputs							
G1	/G2A	/G2B	C	B	A	/Y7	/Y6	/Y5	/Y4	/Y3	/Y2	/Y1	/Y0
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

7-Segment Display

- Displays decimal numbers and some characters
- LED (Light Emitting Diode) or
  LCD (Liquid Crystal Display)
- LED type
  - Common Anode(CA) /Common Cathode(CC) type





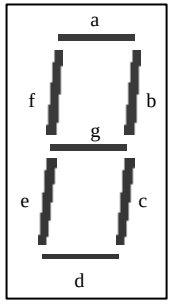


  - CA : requires Active Low inputs (a driver with Active Low outputs)
  - CC : requires Active High inputs (a driver with Active High outputs)

7-Segment Decoder/Driver

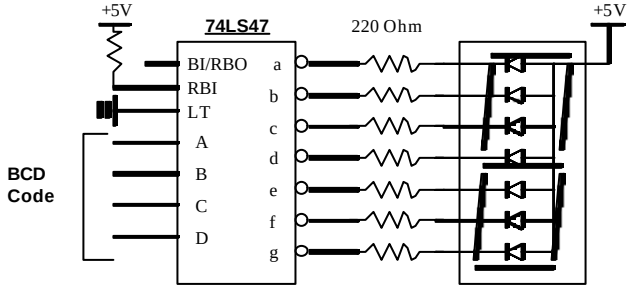
- Input Code : BCD Code
  Output Code : 7-Segment Code
- Truth Table for Active High 7-Segment Decoder/Driver

Input				Output						
D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1



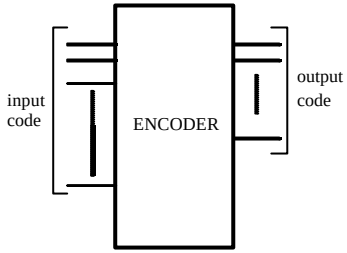
74x47 7-Segment Decoder/Driver

- Driving CC 7-Segment Display



Encoder

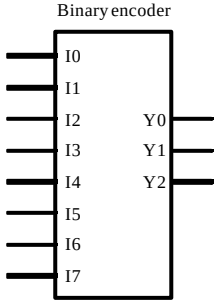
- Multiple-input/multiple-output device.
- Perfoms the inverse function of a Decoder.
- Outputs (m) are less than inputs (n).
- Converts input code words into output code words.



Binary Encoder

- 2^n-to-n Encoder : 2^n Inputs and n Outputs
- Input code : 1-out-of-2^n
- Output code : Binary Code
- Example : n=3, 8-to-3 encoder

Inputs								Outputs		
I0	I1	I2	I3	I4	I5	I6	I7	Y0	Y1	Y2
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



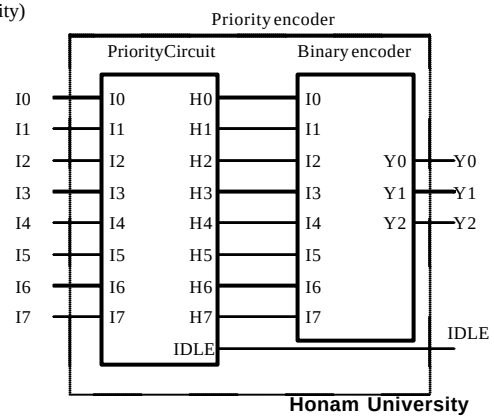
Priority Encoder

- Assign priorities to the inputs
- When more than one input are asserted, the output generates the code of the input with the highest priority
- Priority Encoder :

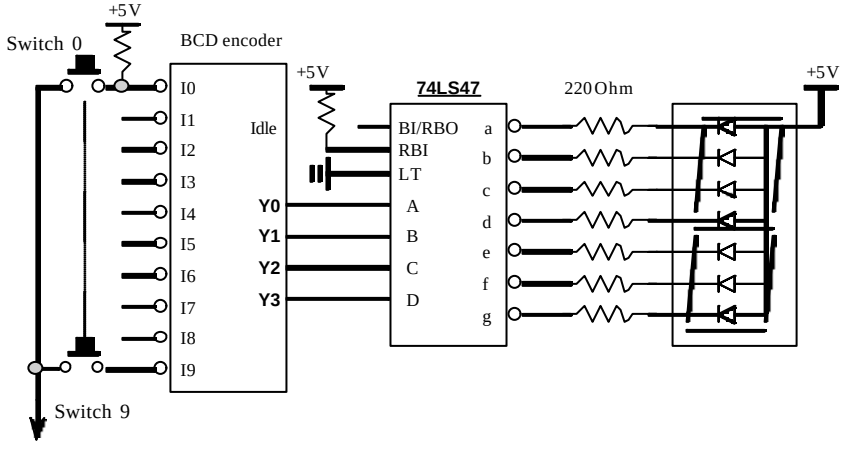
H7=I7 (Highest Priority)
H6=I6.I7'
H5=I5.I6'.I7'
H4=I4.I5'.I6'.I7'
H3=I3.I4'.I5'.I6'.I7'
H2=I2.I3'.I4'.I5'.I6'.I7'
H1=I1. I2'.I3'.I4'.I5'.I6'.I7'
H0=I0.I1'. I2'.I3'.I4'.I5'.I6'.I7'
IDLE= I0'.I1'. I2'.I3'.I4'.I5'.I6'.I7'

- Encoder

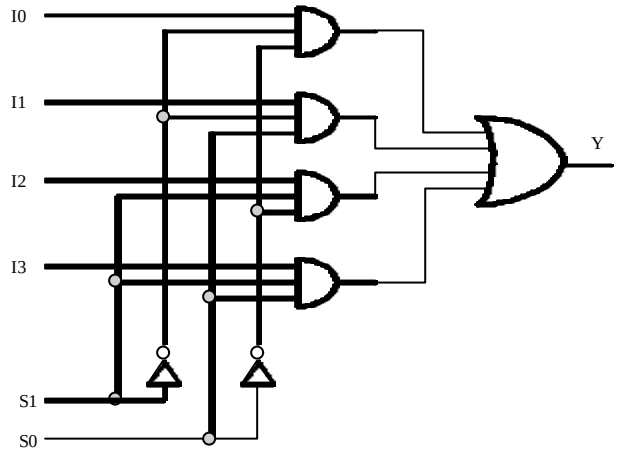
Y0 = I1 + I3 + I5 + I7
Y1 = I2 + I3 + I6 + I7
Y2 = I4 + I5 + I6 + I7



BCD Encoder (Application)



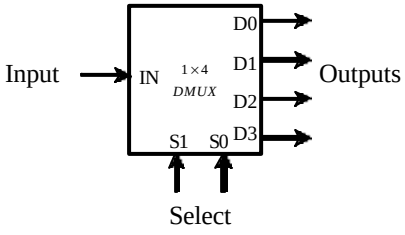
Logic Diagram of 4-to-1 Multiplexer



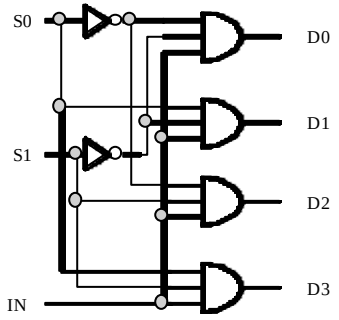
1-to-4 DMUX

1-to-4 DEMUX
Function Table

IN	S1	S0	D0	D1	D2	D3
x	0	0	IN	0	0	0
x	0	1	0	IN	0	0
x	1	0	0	0	IN	0
x	1	1	0	0	0	IN



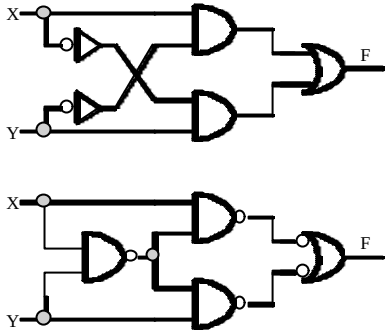
Logic Diagram



Exclusive OR & Exclusive NOR Gate

- XOR : $X \oplus Y = X' \cdot Y + X \cdot Y'$
- XNOR : $(X \oplus Y)' = X \cdot Y + X' \cdot Y'$
- Truth Table :

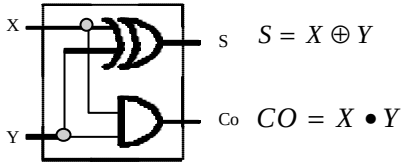
X	Y	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1



Half Adder

- Truth table :

X	Y	S=(X+Y)	Co
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



$S = X \oplus Y$

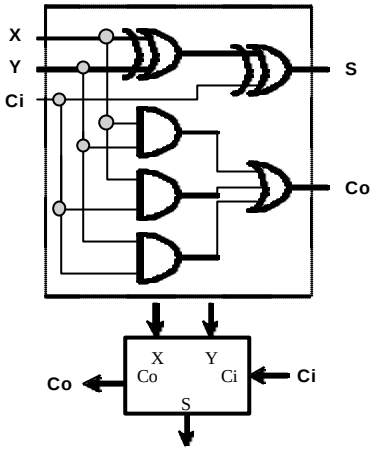
$CO = X \bullet Y$

Full Adder

- Truth Table

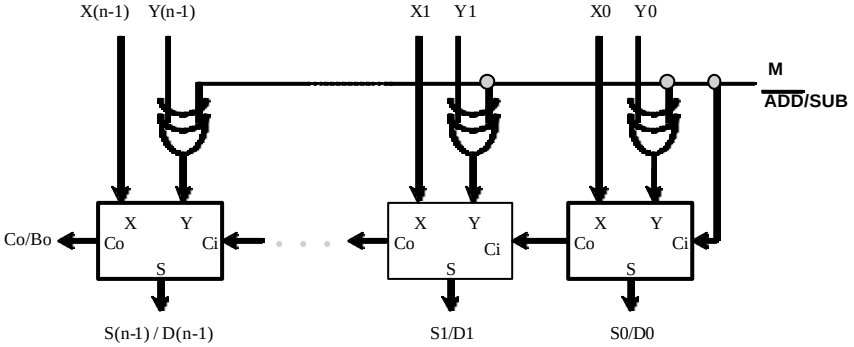
X	Y	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- S = X'Y'Ci+ X'YCi'+XY'Ci'+XYCi
  $S = X \oplus Y \oplus CIN$
- Co = XY+X Ci+Y Ci



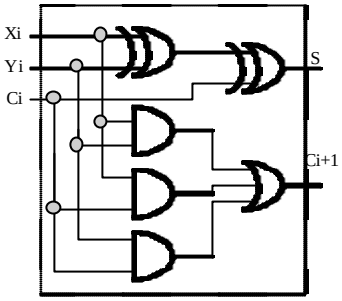
Adder/Subtractor Circuit

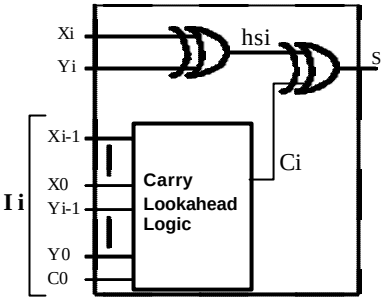
- M=0 : Ripple Adder
- M=1 : Ripple Subtractor



Full Adder vs. Carry Lookahead Adder

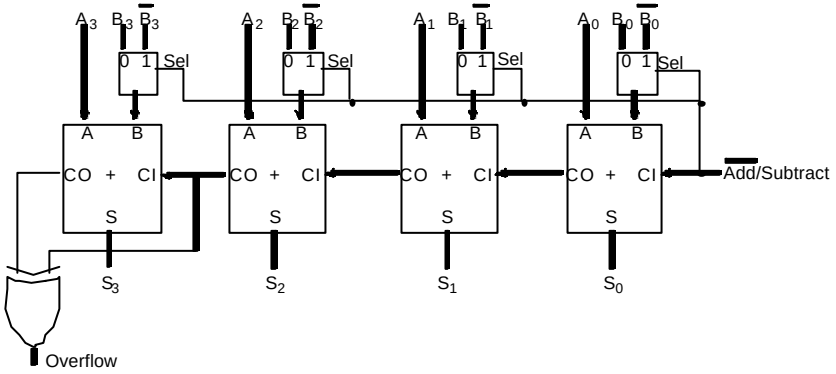
- Full Adder
- Carry Lookahead Adder





Networks for Binary Addition

Adder/Subtractor - assumes2 'scomplementrepresentation



A - B = A + (-B) = A + $\overline{B}$ + 1