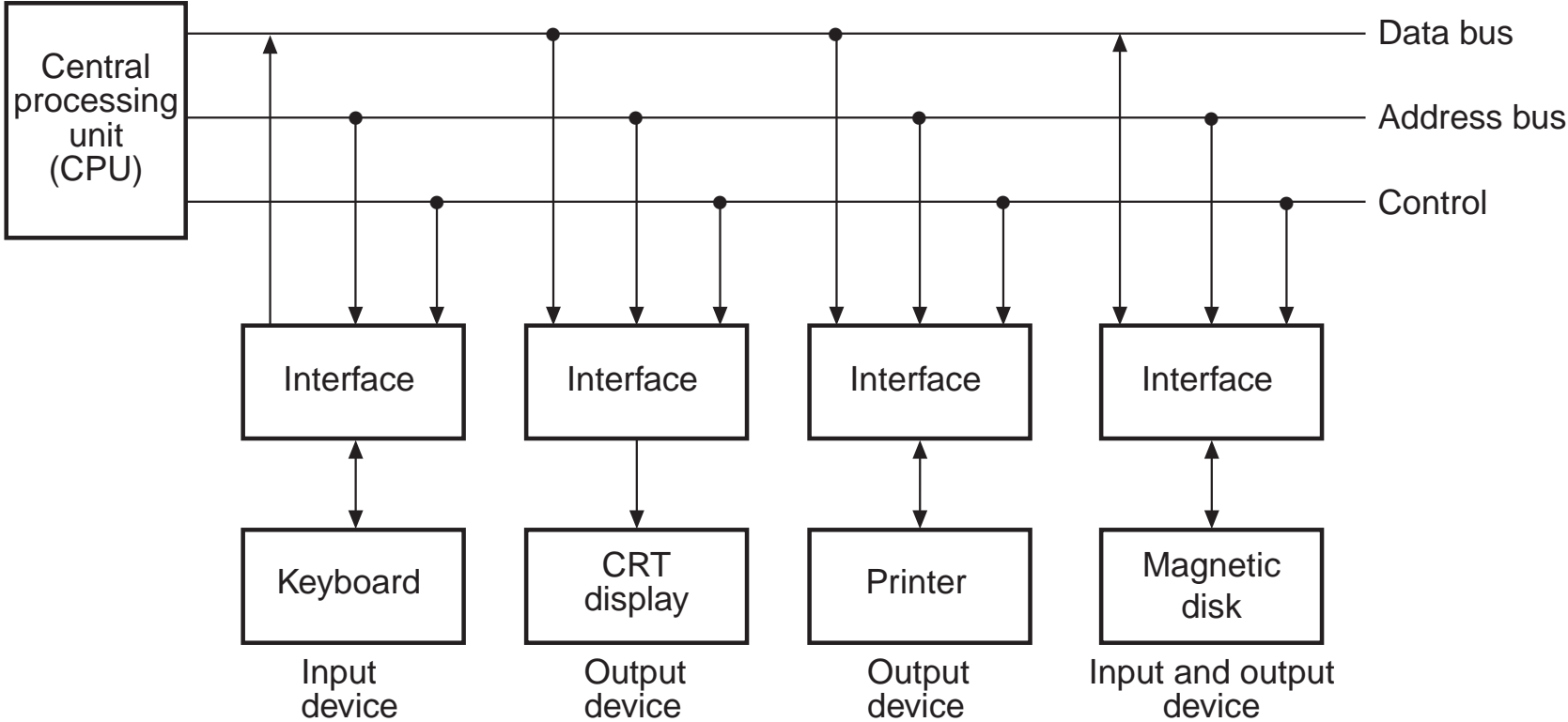
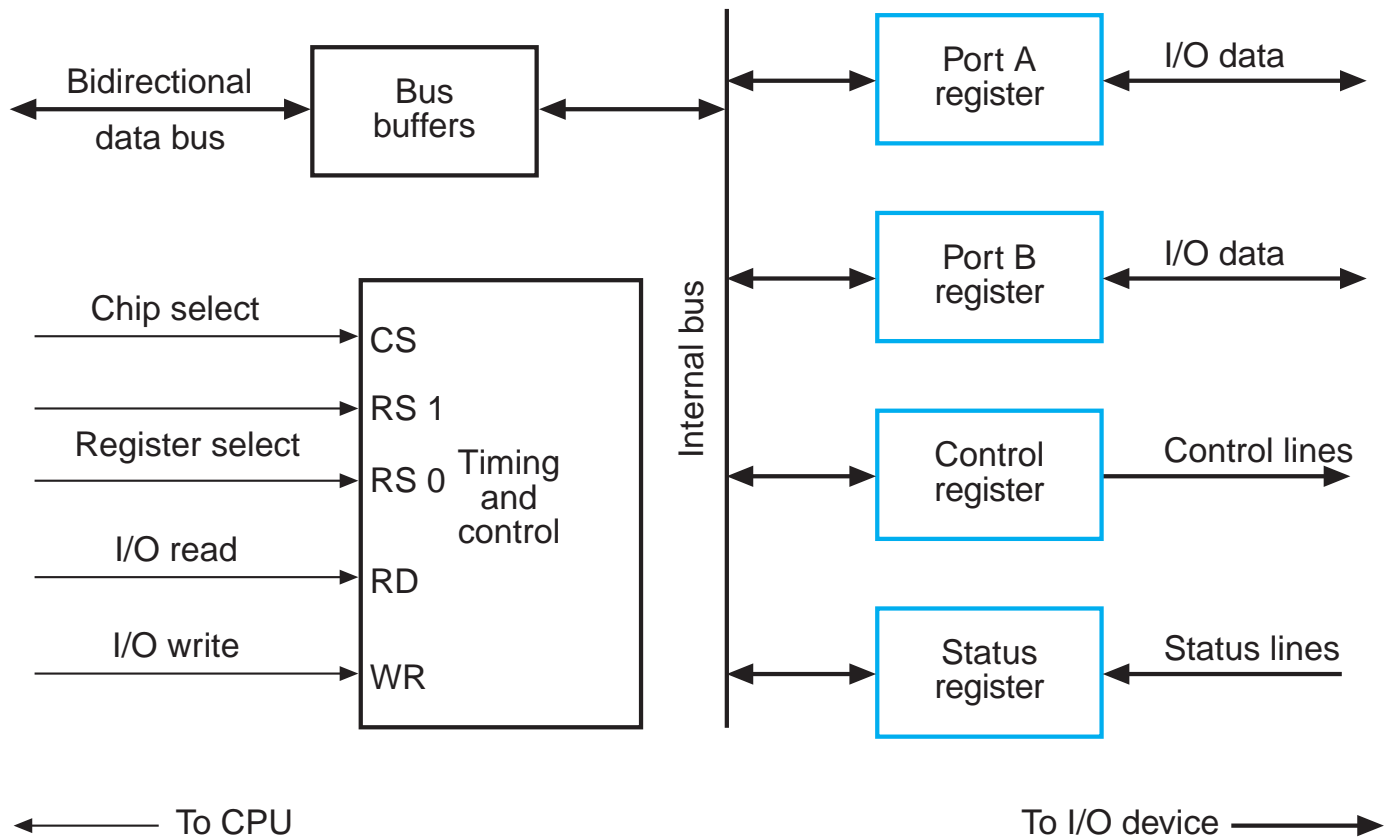
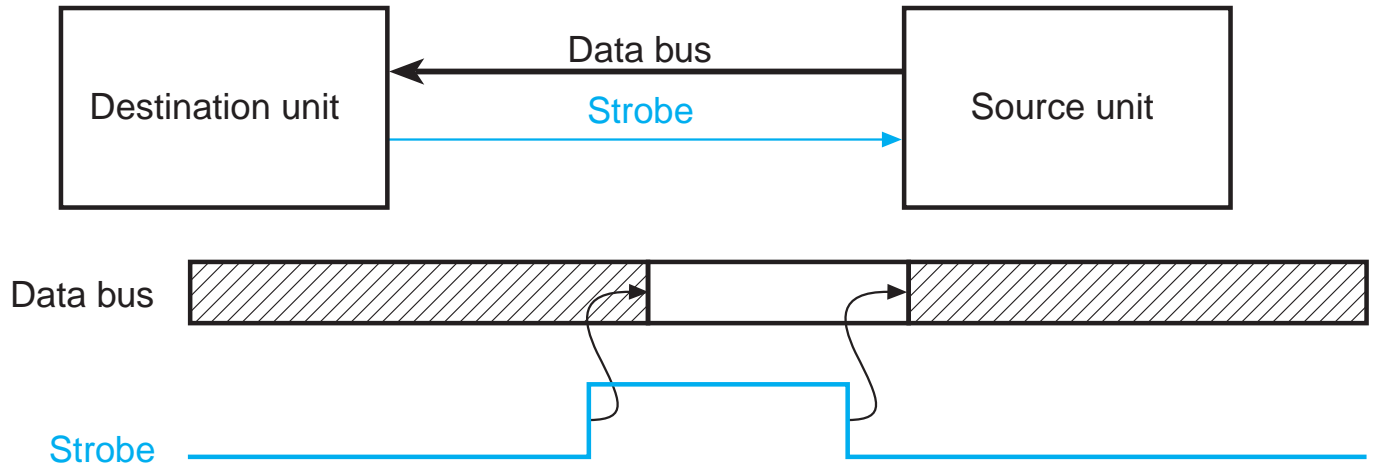


Connection of I/O Devices to CPU

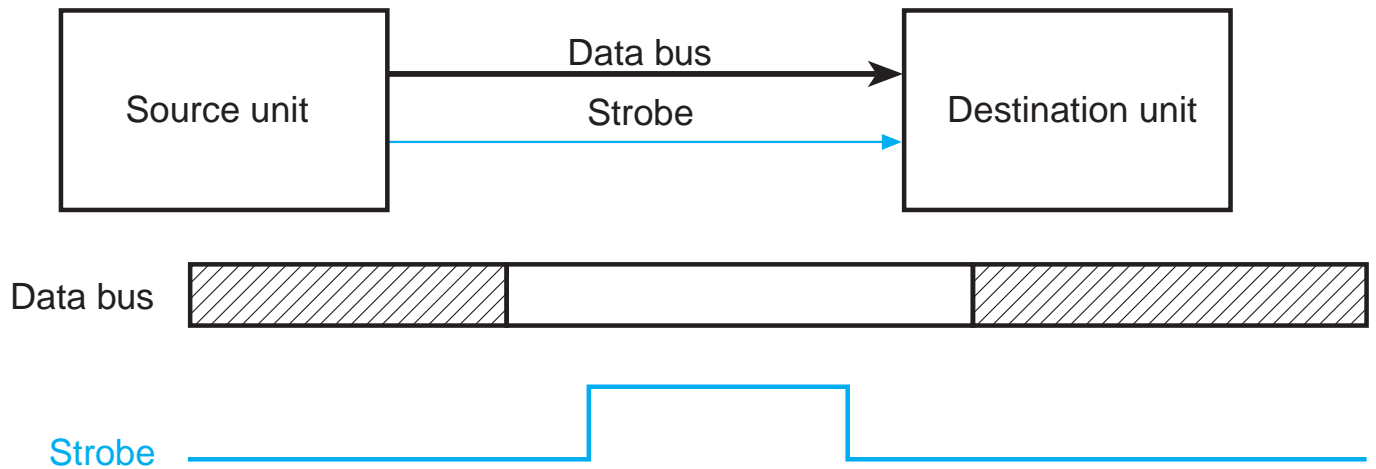




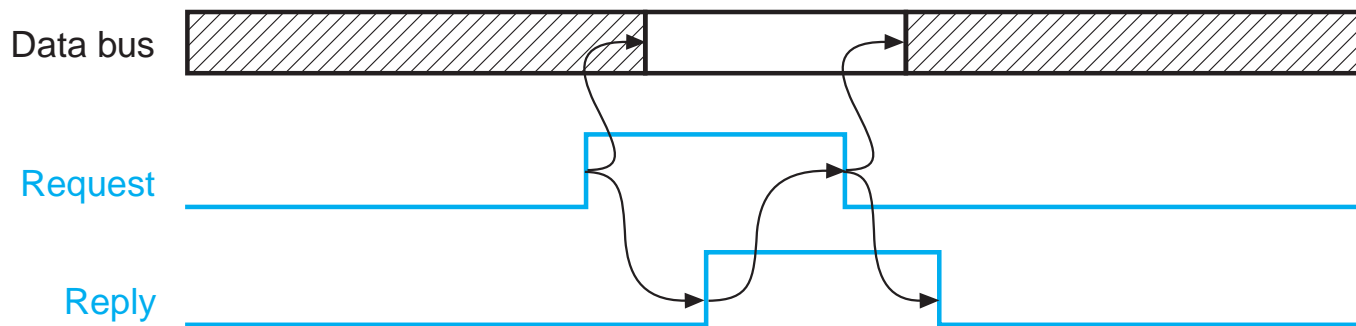
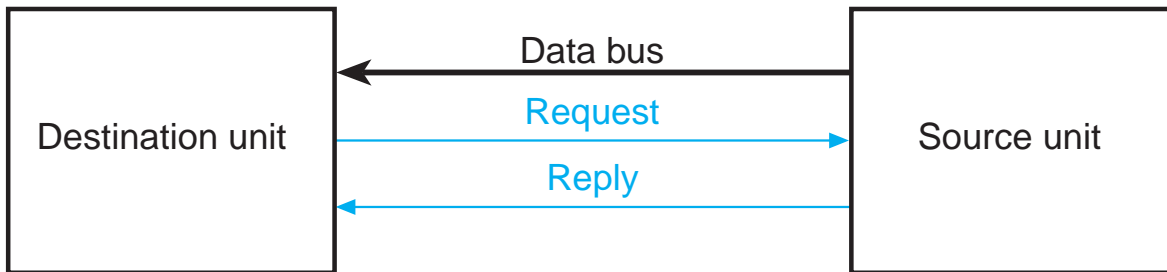
CS	RS1	RS0	Register selected
0	x	x	None: data bus in high-impedance state
1	0	0	Port A register
1	0	1	Port B register
1	1	0	Control register
1	1	1	Status register



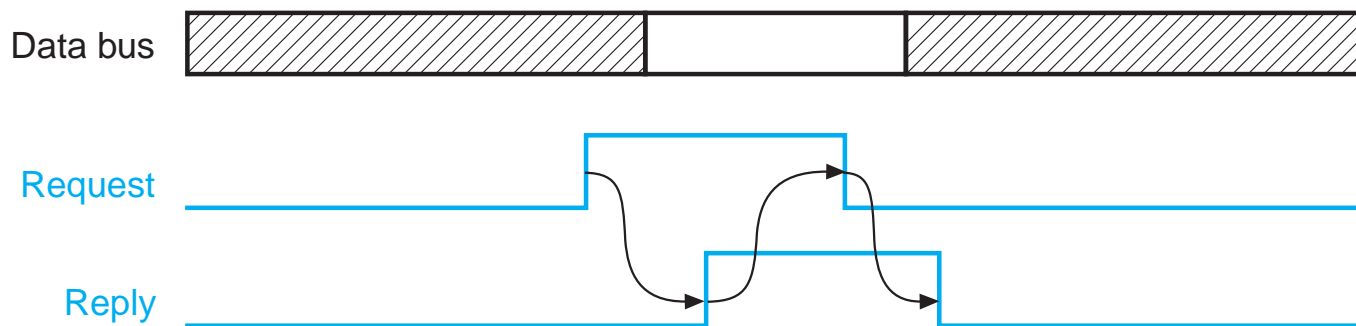
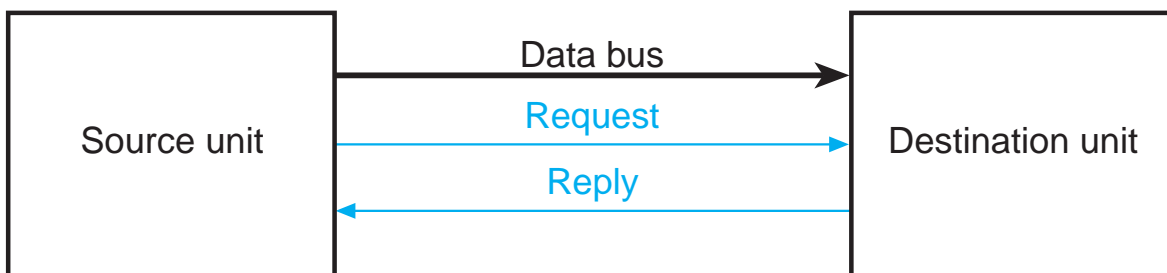
(a) Destination-initiated transfer



(b) Source-initiated transfer

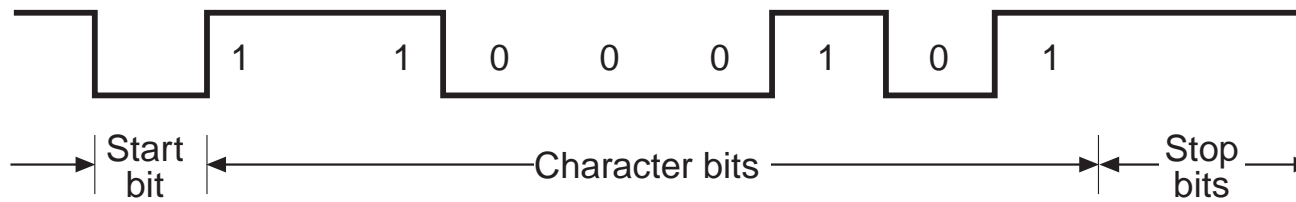


(a) Destination-initiated transfer

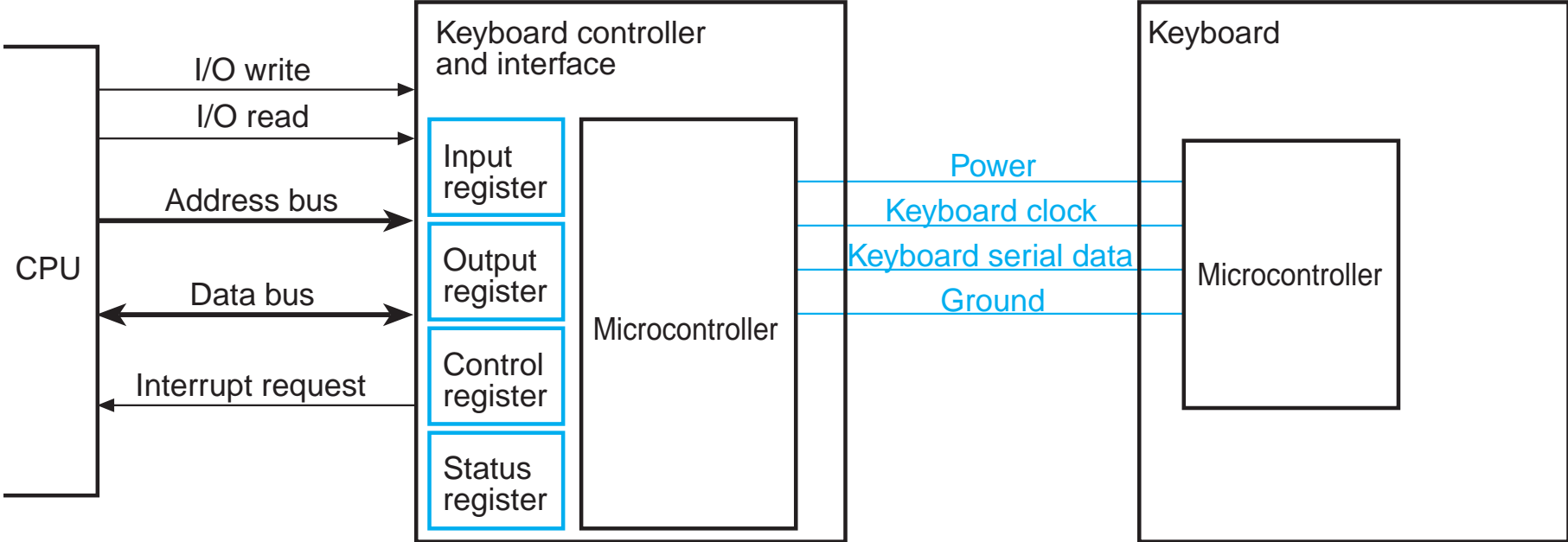


(b) Source-initiated transfer

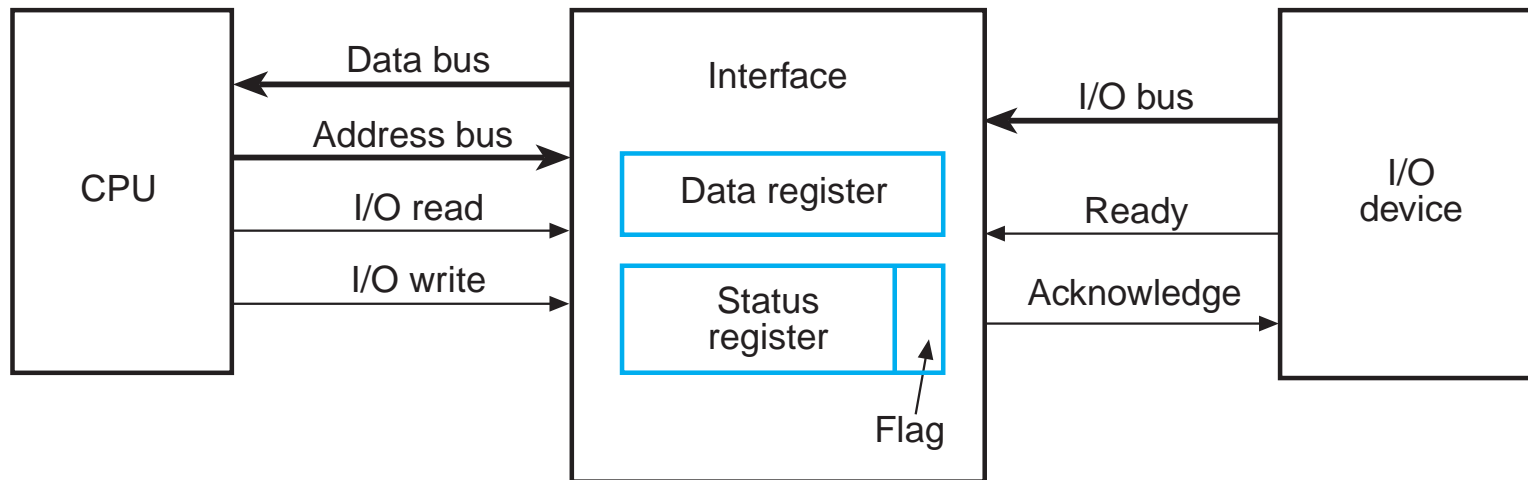
Format of Asynchronous Serial Transfer of Data

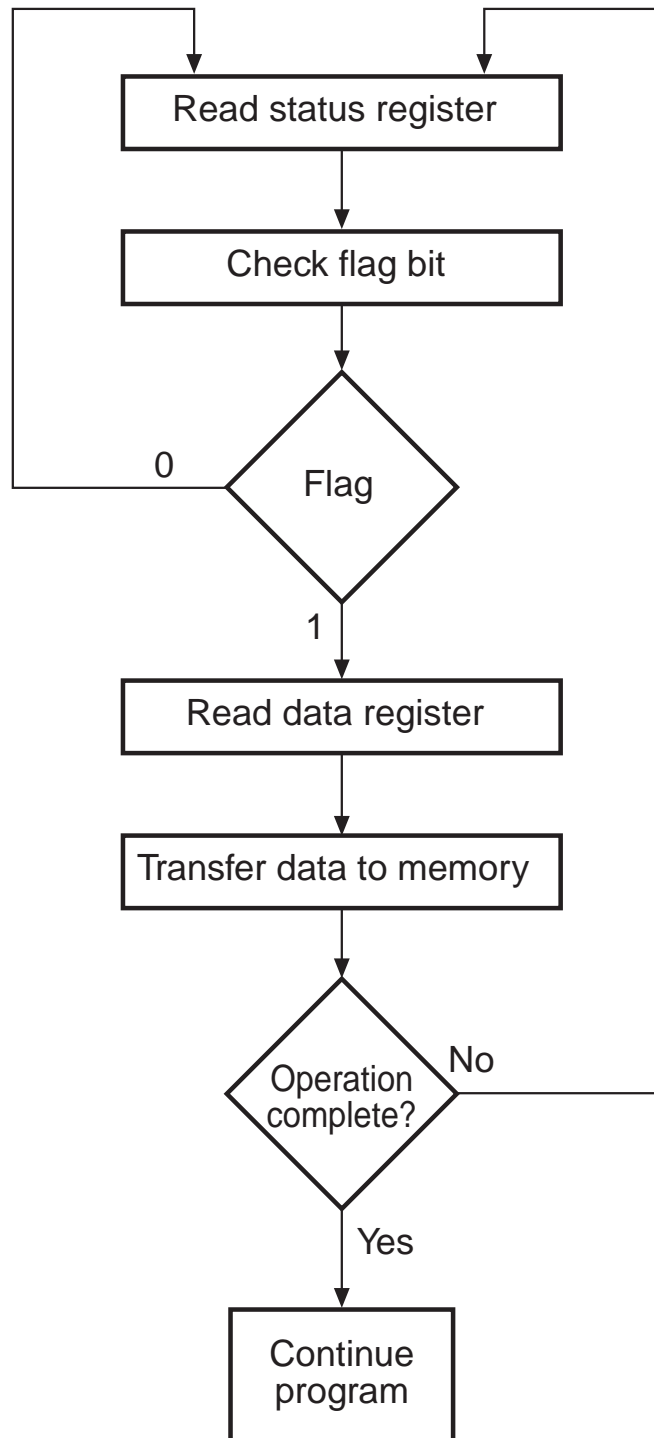


Keyboard Controller and Interface

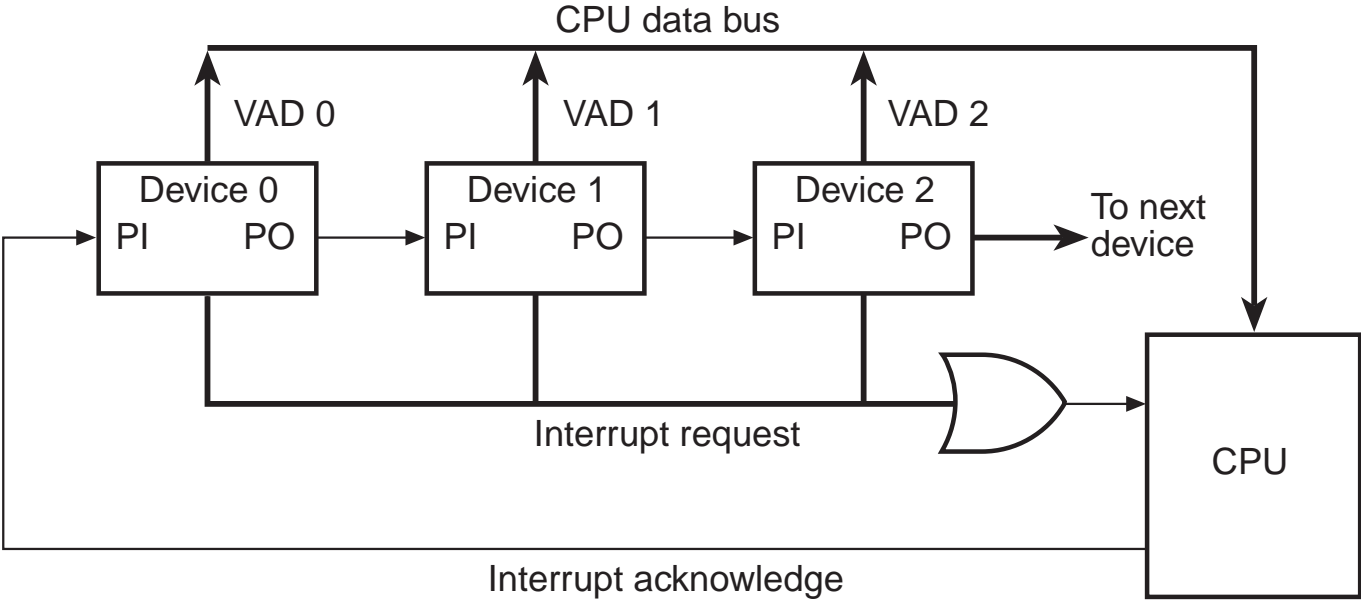


Data Transfer from I/O Device to CPU

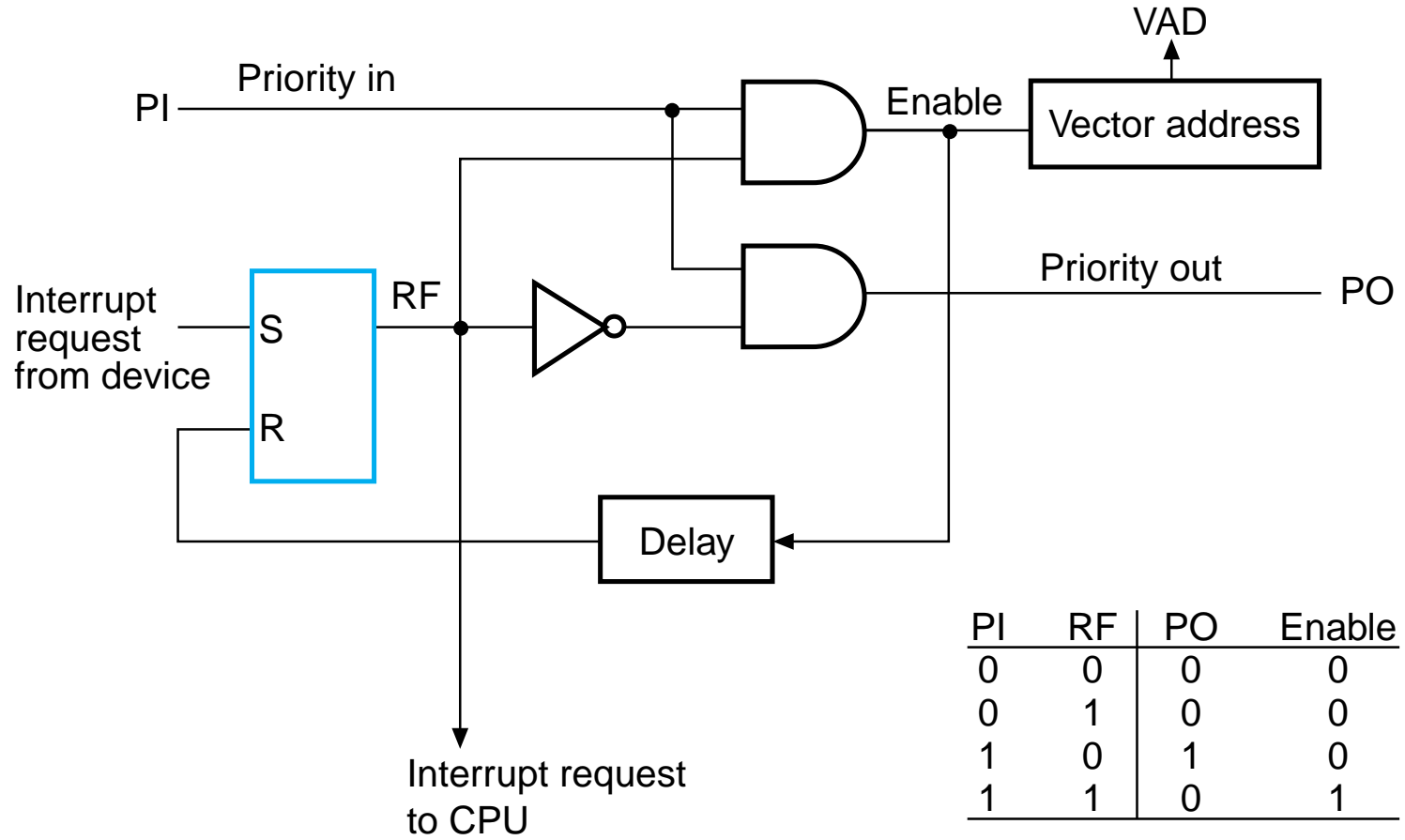




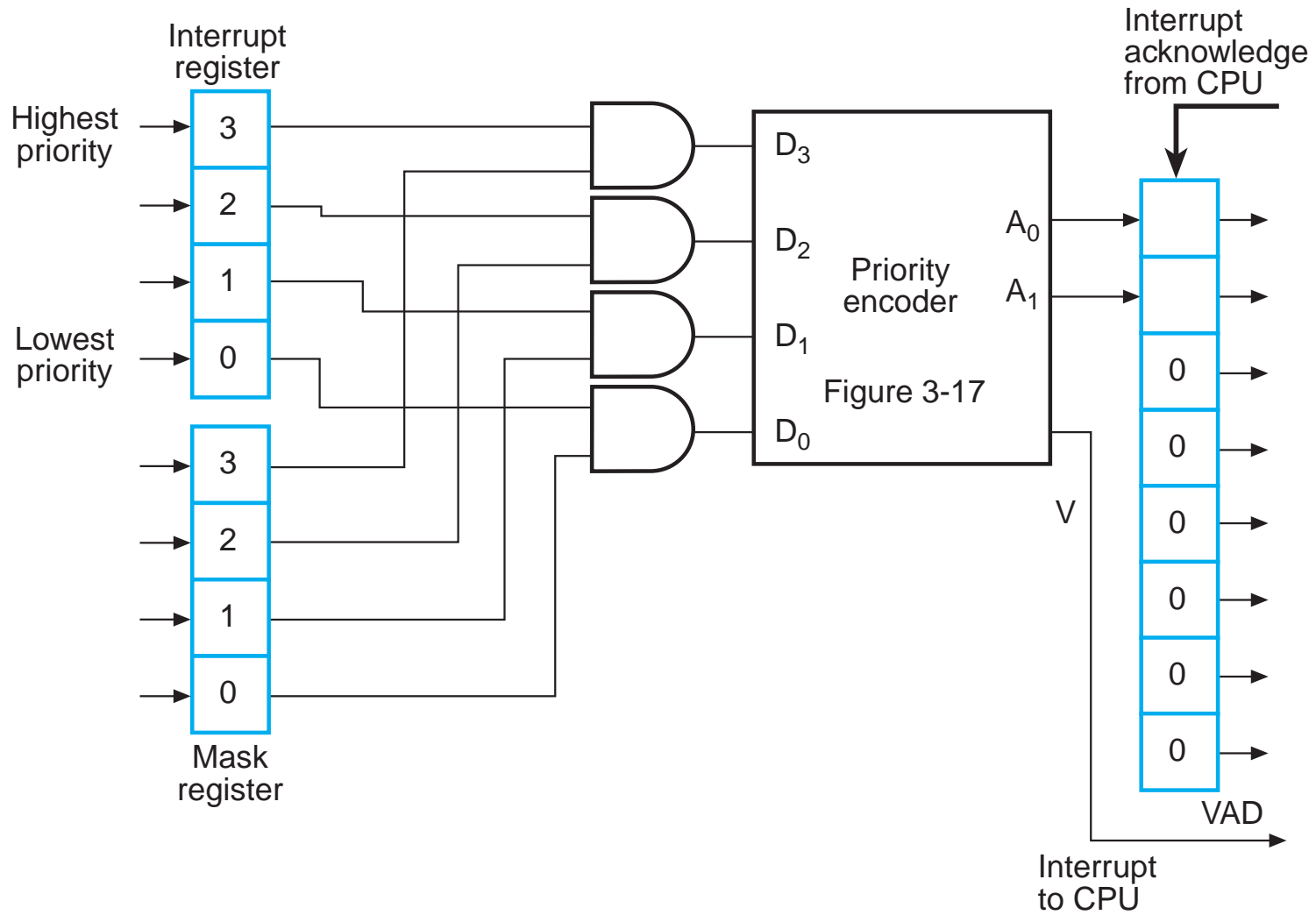
Daisy Chain Priority Interrupt



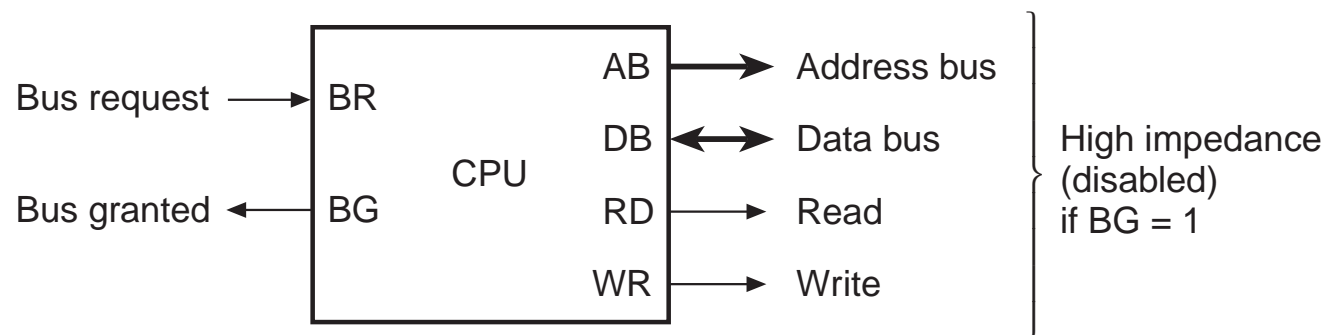
One Stage of the Daisy Chain Priority Arrangement



Parallel Priority Interrupt Hardware



CPU Bus Control Signals



Block Diagram of a DMA Controller

