Truth Table for Code Converter Example

Decimal Digit	Input BCD				Output Excess-3			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

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Truth Table for BCD–to–Seven-Segment Decoder

BCD Input				Seven-Segment Decoder						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
All other inputs				0	0	0	0	0	0	0

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Truth Table for 3–to–8-Line Decoder

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

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Truth Table for Octal-to-Binary Encoder

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

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Truth Table of Priority Encoder

Inputs				Outputs		
D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

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Signed Binary Numbers

Decimal	Signed 2's Complement	Signed 1's Complement	Signed Magnitude
+7	0111	0111	0111
+6	0110	0110	0110
+5	0101	0101	0101
+4	0100	0100	0100
+3	0011	0011	0011
+2	0010	0010	0010
+1	0001	0001	0001
+0	0000	0000	0000
−0	—	1111	1000
−1	1111	1110	1001
−2	1110	1101	1010
−3	1101	1100	1011
−4	1100	1011	1100
−5	1011	1010	1101
−6	1010	1001	1110
−7	1001	1000	1111
−8	1000	—	—

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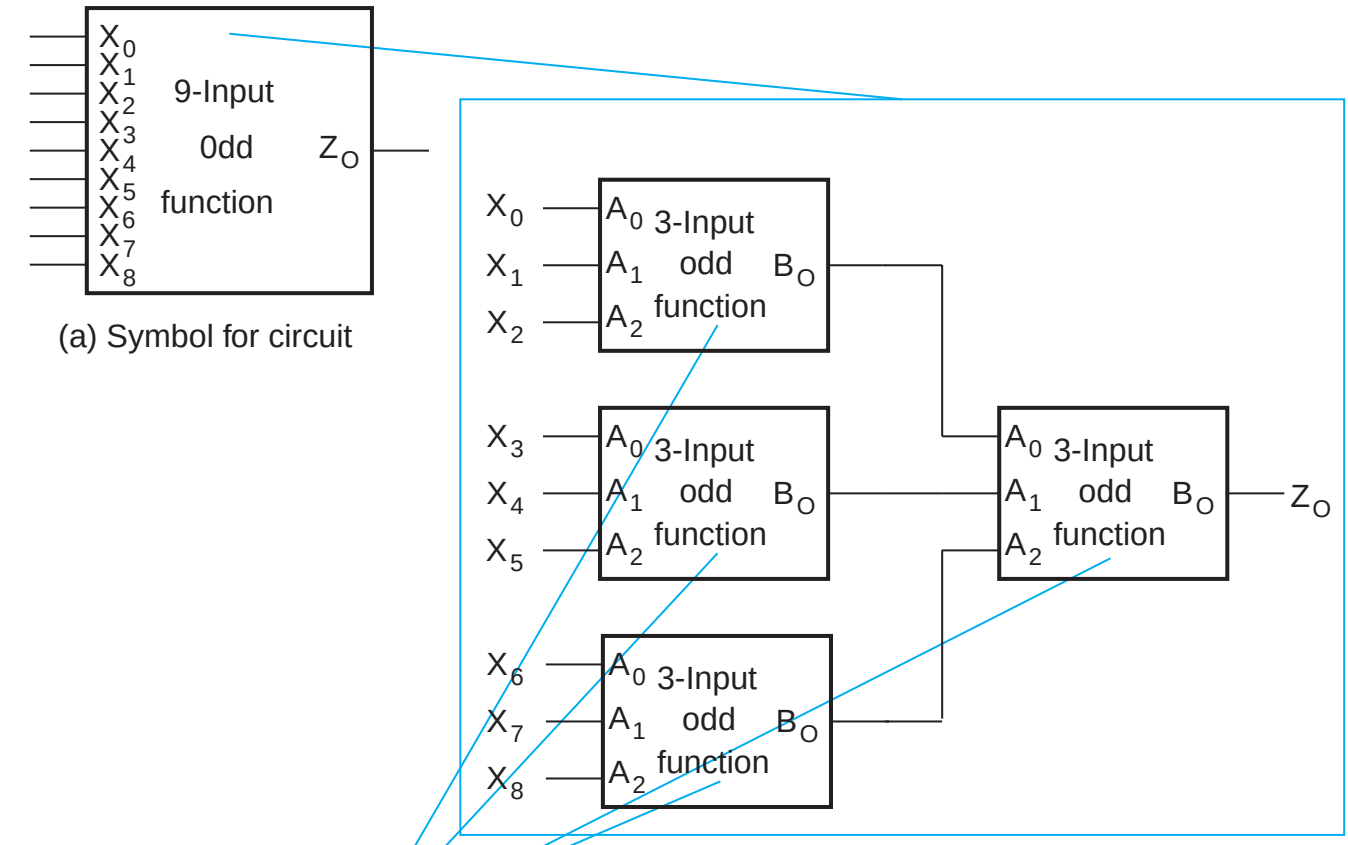
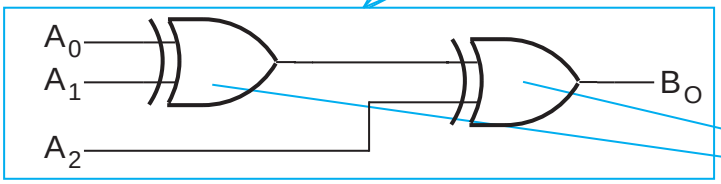
Example of Design Hierarchy and Reusable Blocks

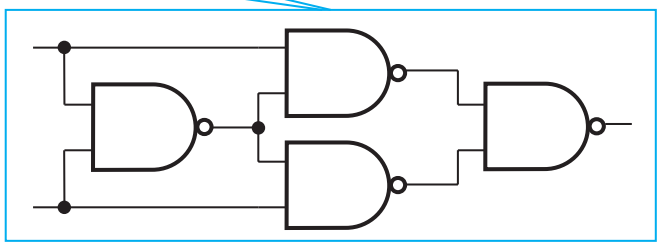


(a) Symbol for circuit

(b) Circuit as interconnected 3-input odd function blocks



(c) 3-input odd function circuit as interconnected exclusive-OR blocks



(d) Exclusive-OR block as interconnected NANDs

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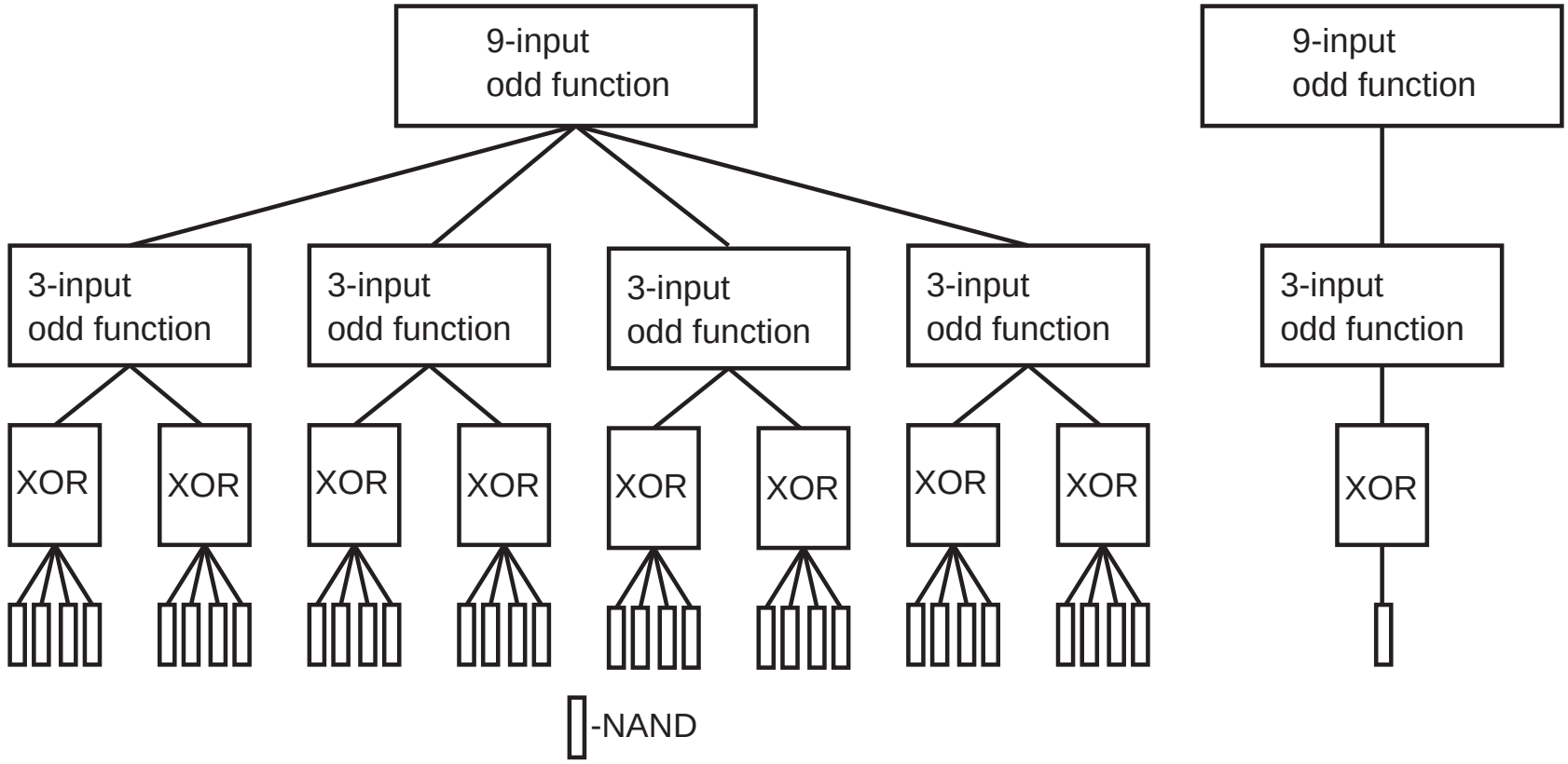
Diagrams Representing the Hierarchy for Figure 3-2



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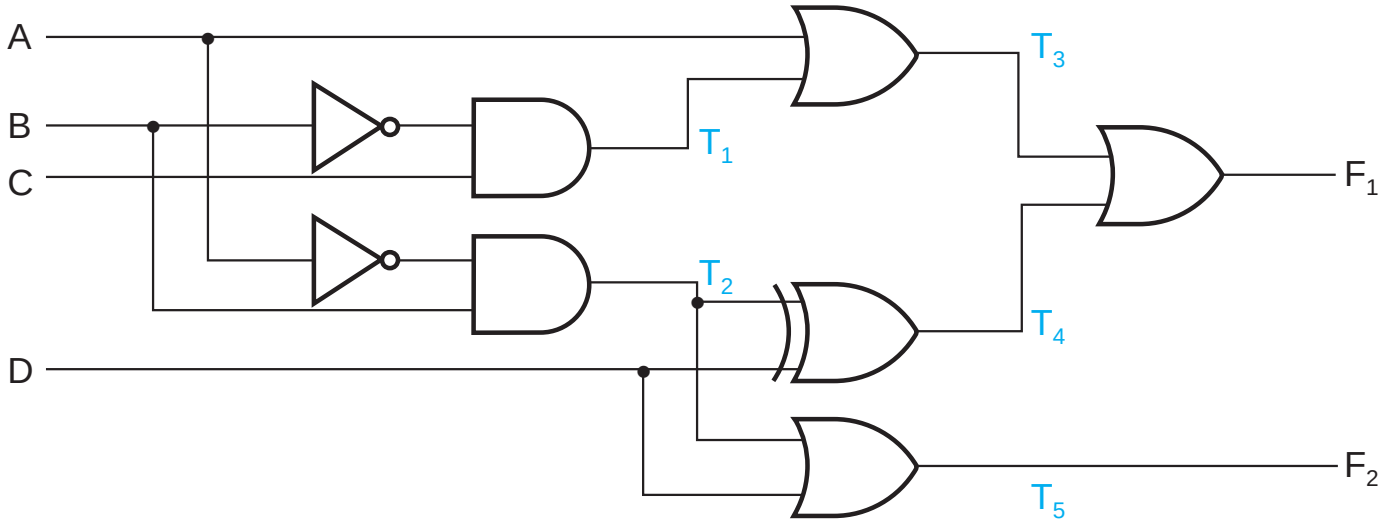
Logic Diagram for Analysis Example



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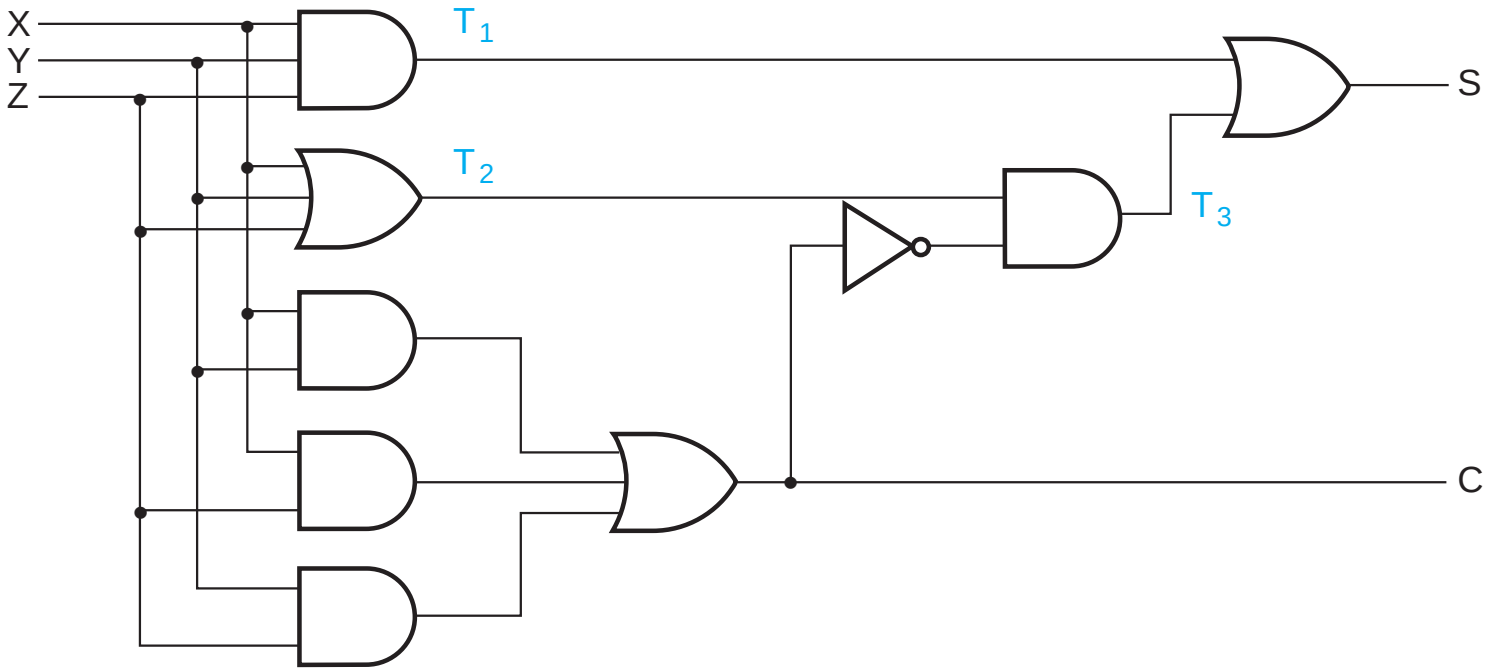
Logic Diagram for Binary Adder



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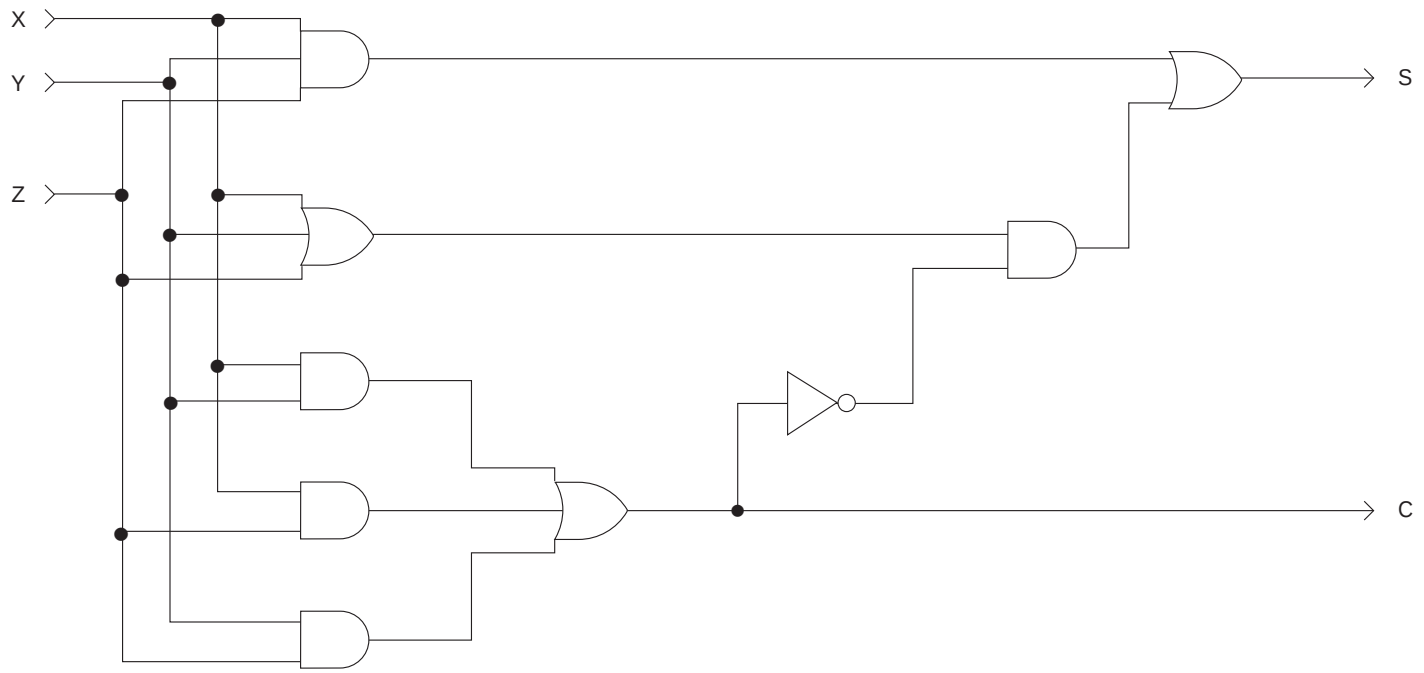
ViewDraw® Schematic for Binary Adder in Figure 3-5



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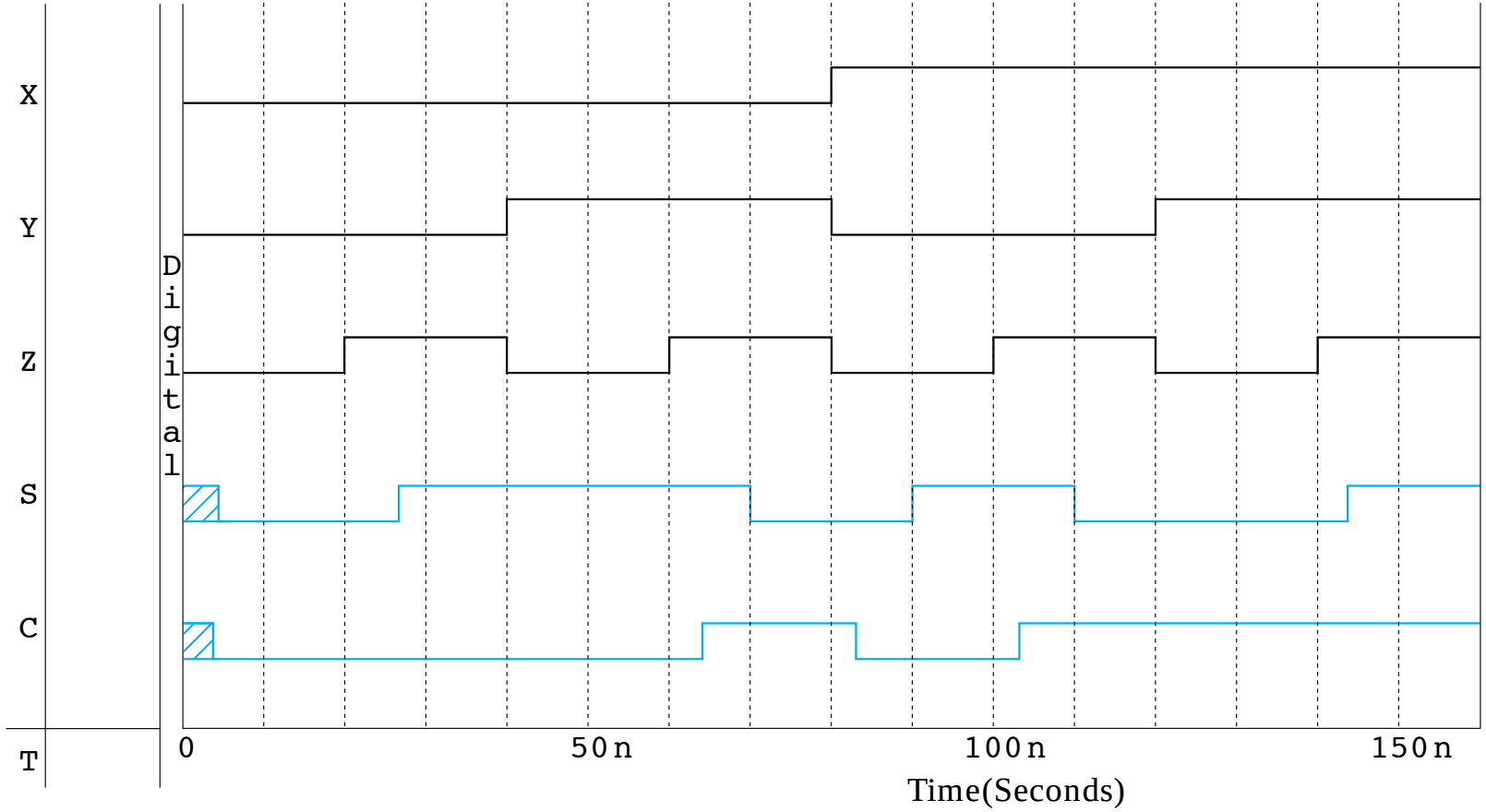
ViewTrace® Input and Output Waveforms for the Binary Adder Schematic in Figure 3-6



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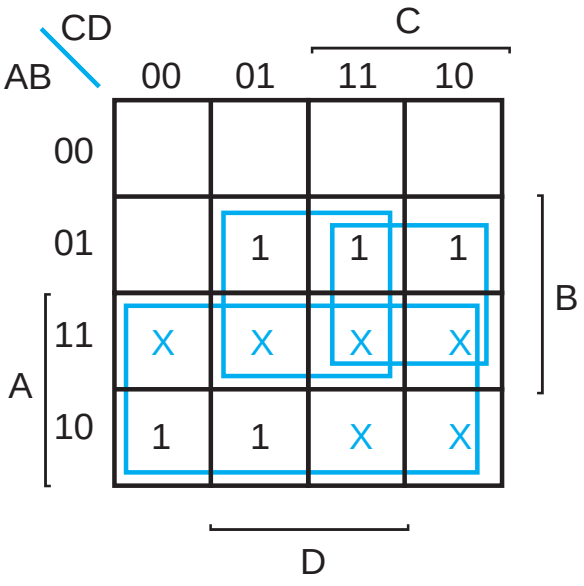
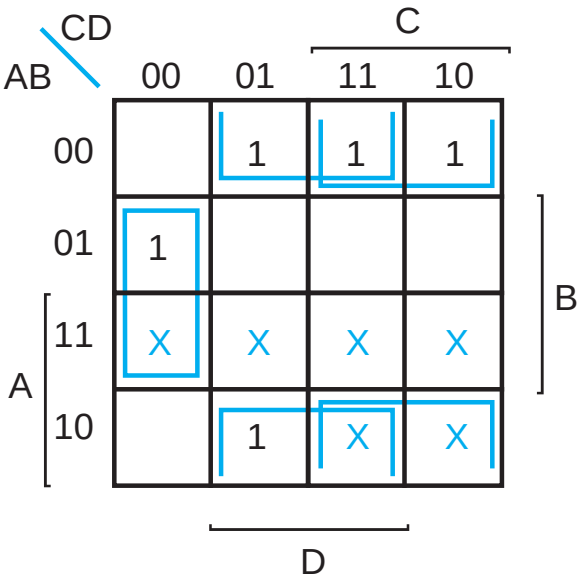
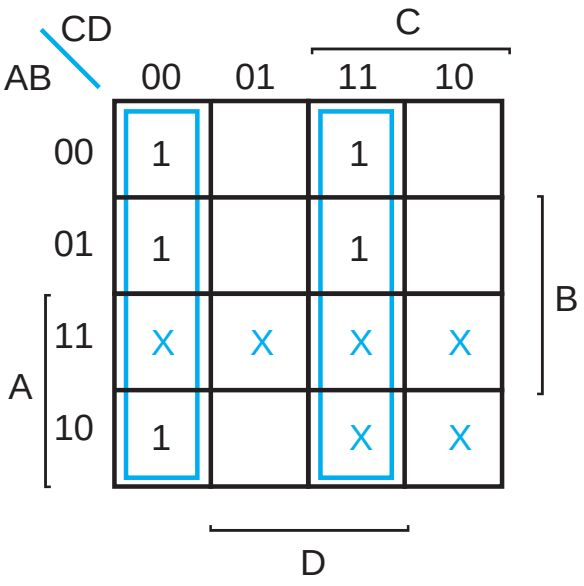
Maps for BCD–to–Excess-3 Code Converter



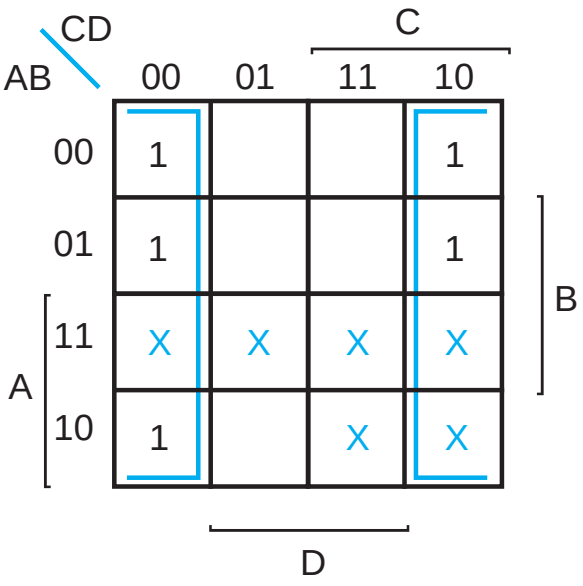
$W = A + BC + BD$



$X = \overline{B}C + BD + B\overline{C}\overline{D}$



$Y = CD + \overline{C}\,\overline{D}$



$Z = \overline{D}$

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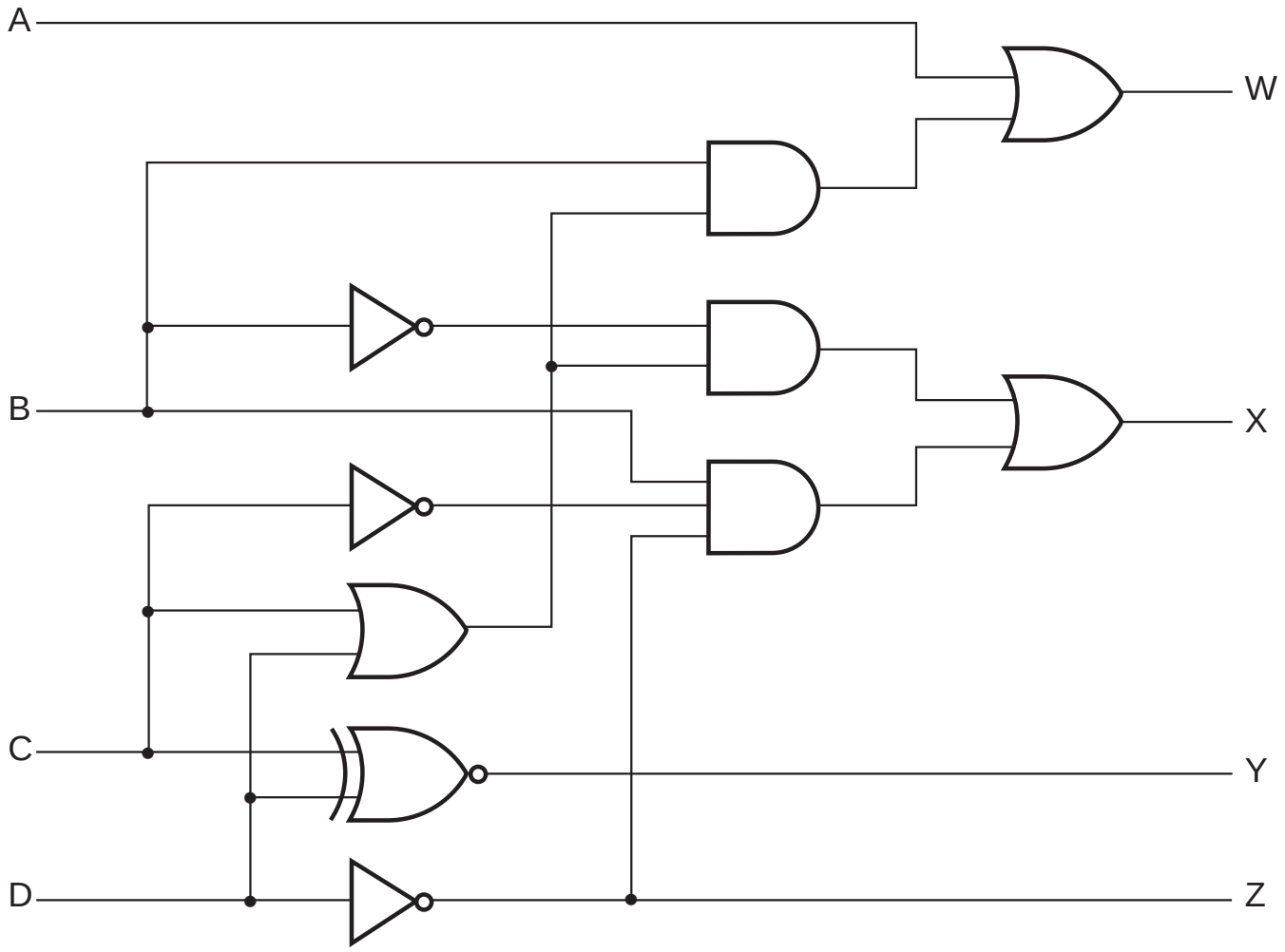
Logic Diagram of BCD–to–Excess-3 Code Converter



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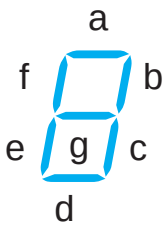
Seven-Segment Display



(a) Segment designation

(b) Numeric designation for display

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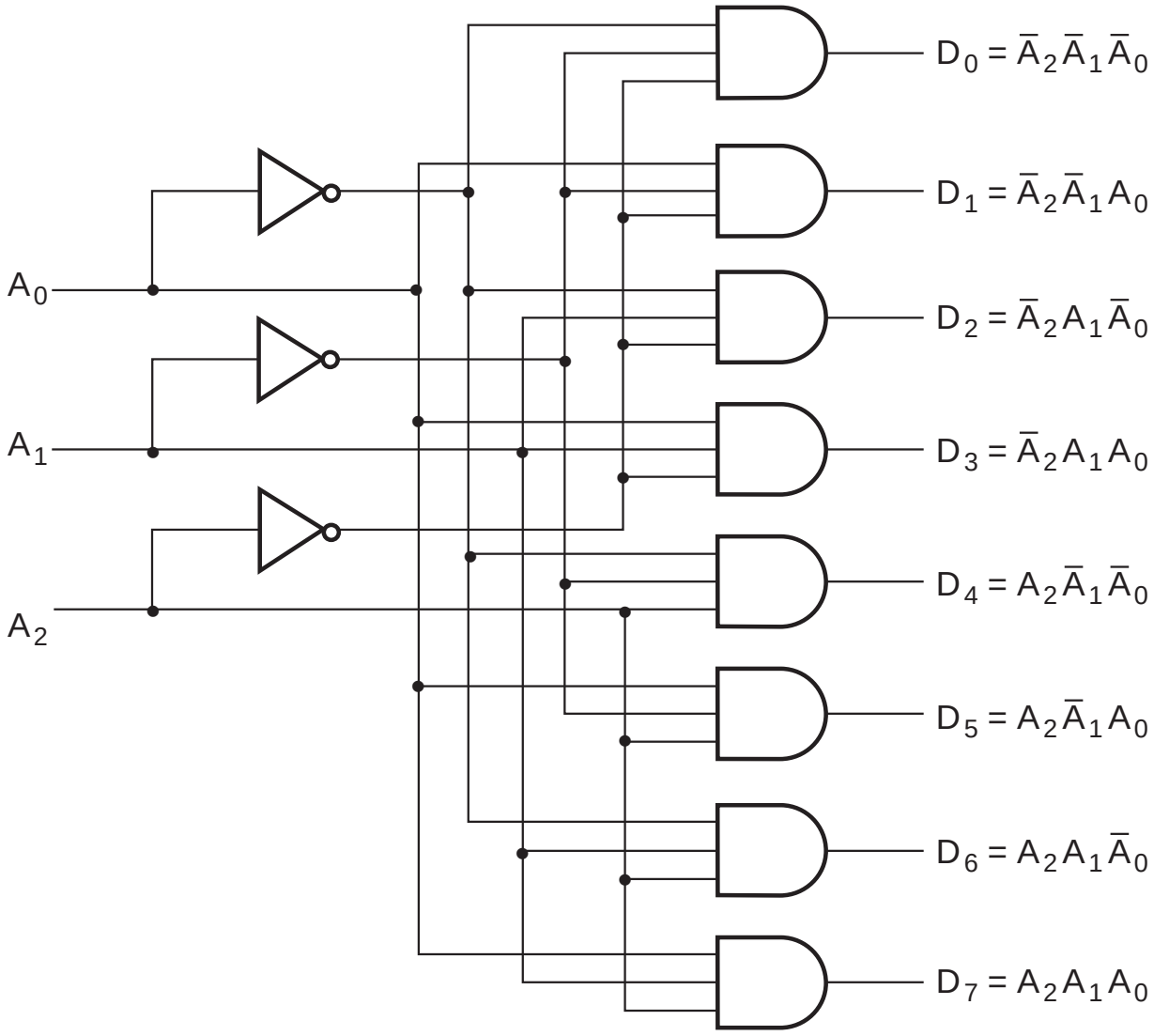
3–to–8-Line Decoder



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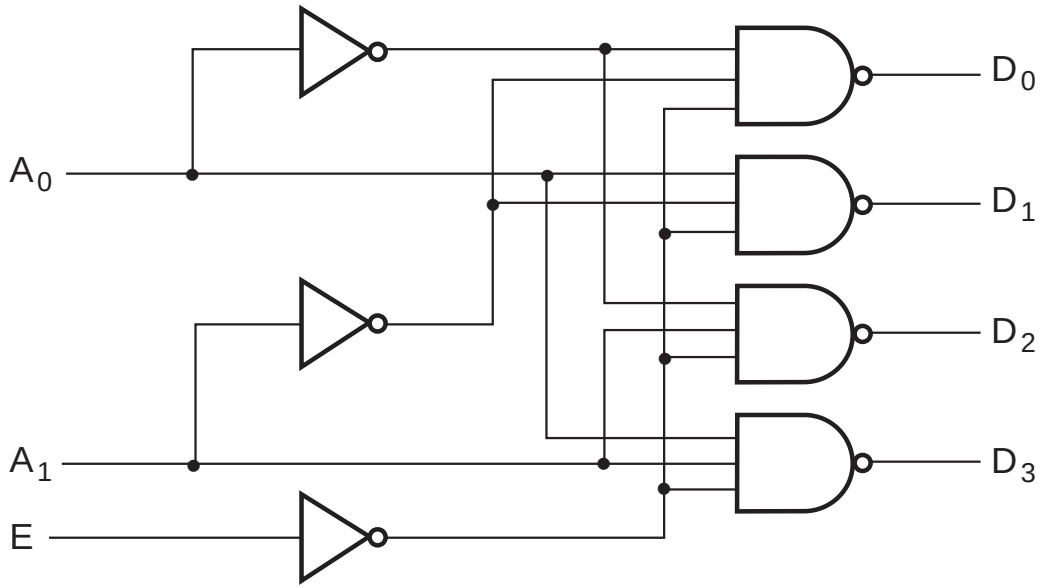
A 2–to–4-Line Decoder with Enable Input



(a) Logic diagram

E	A_1	A_0	D_0	D_1	D_2	D_3
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

(b) Truth table

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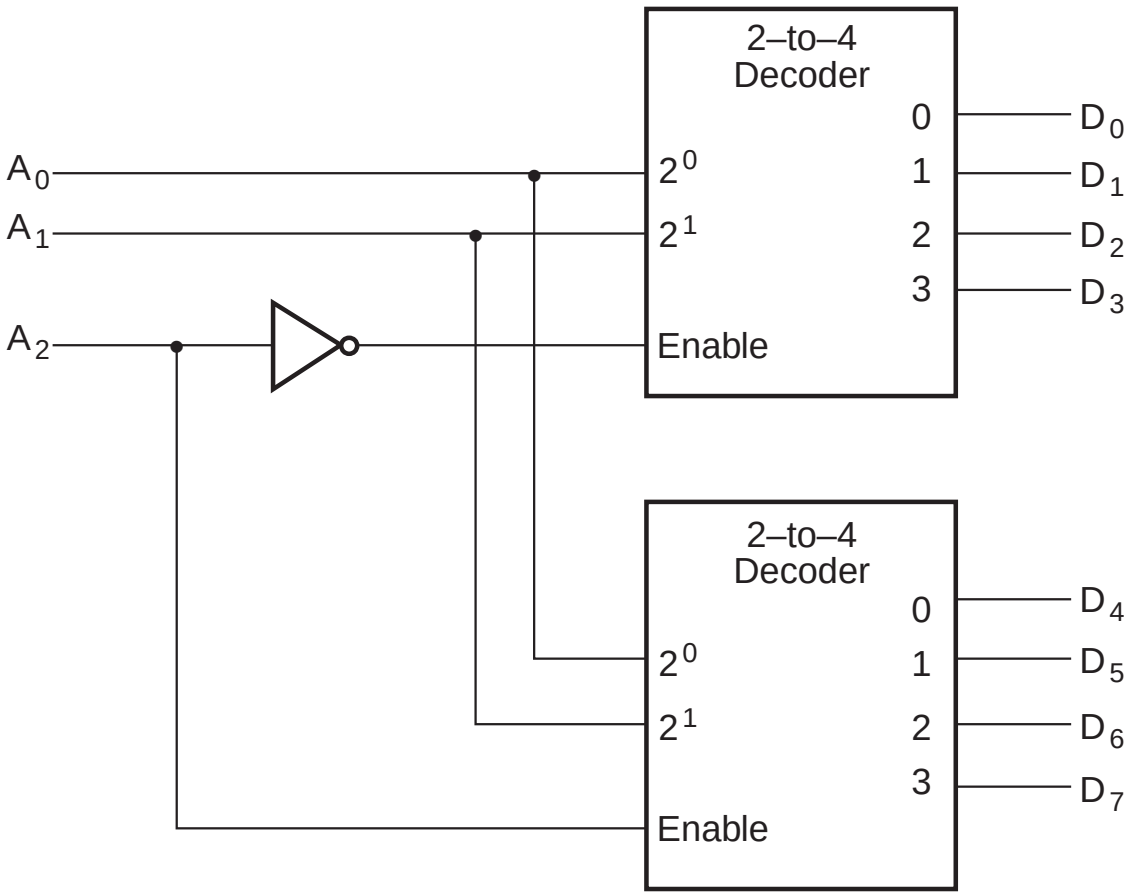
T-45 A 3–to–8 Decoder Constructed with Two 2–to–4 Decoders



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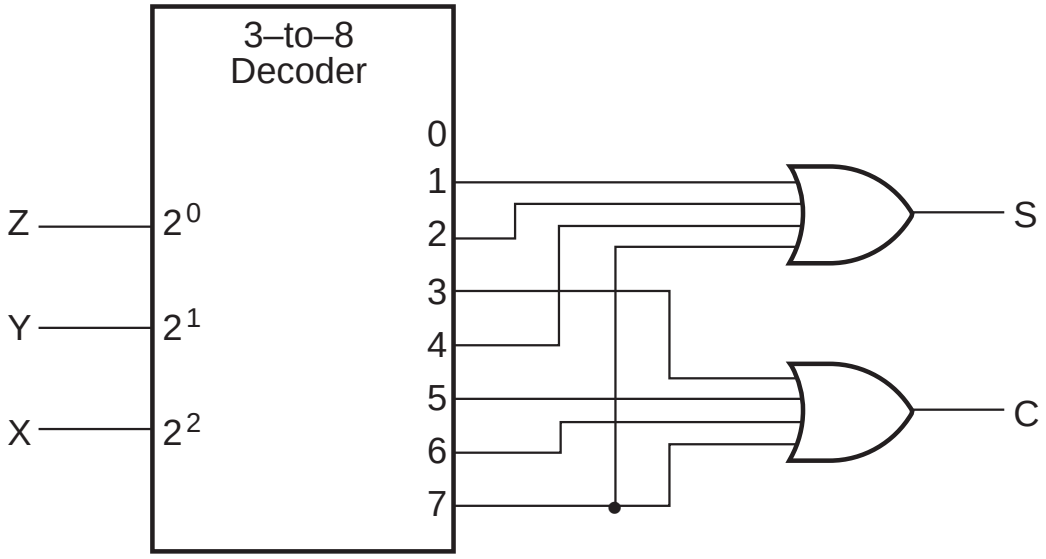
Implementing a Binary Adder Using a Decoder



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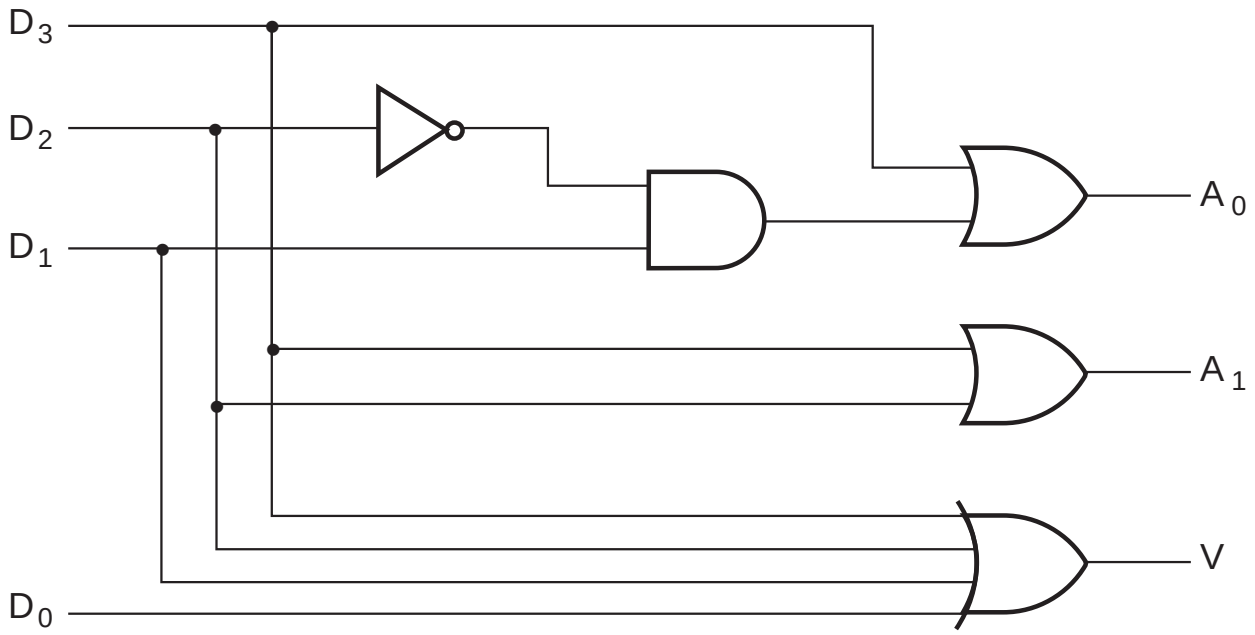
Logic Diagram of a 4-Input Priority Encoder



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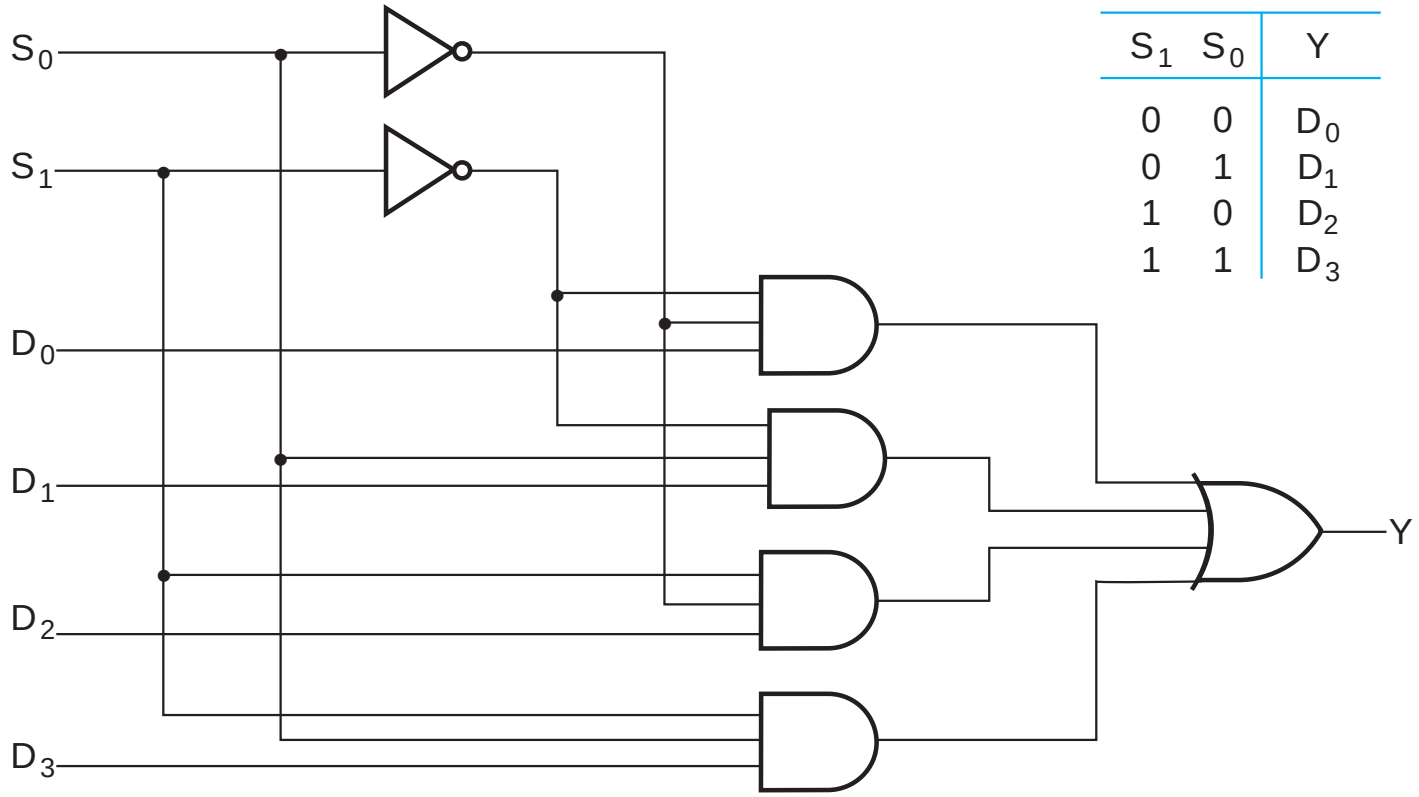
4–to–1-Line Multiplexer



Function table

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

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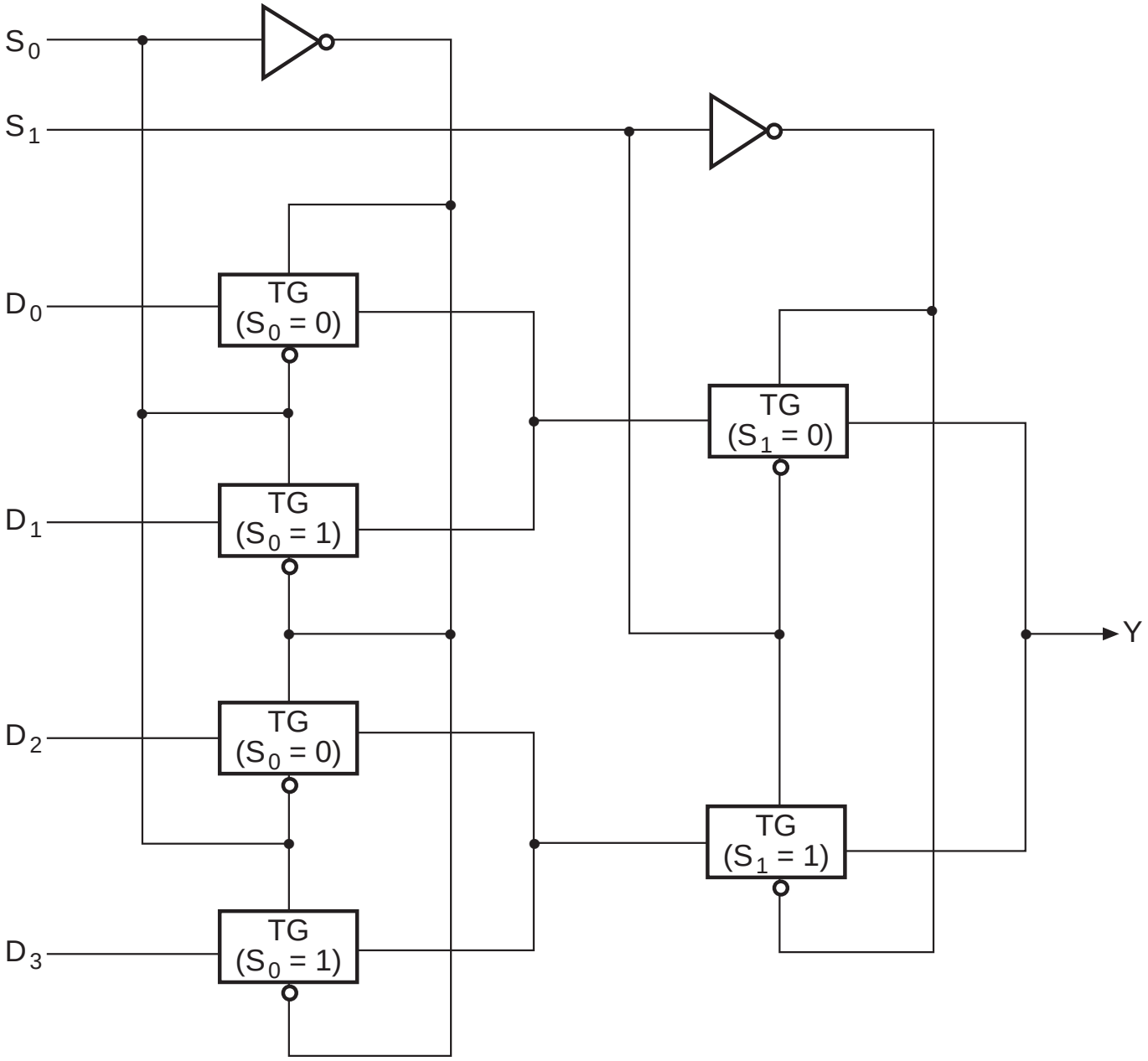
4–to–1-Line Multiplexer with Transmission Gates



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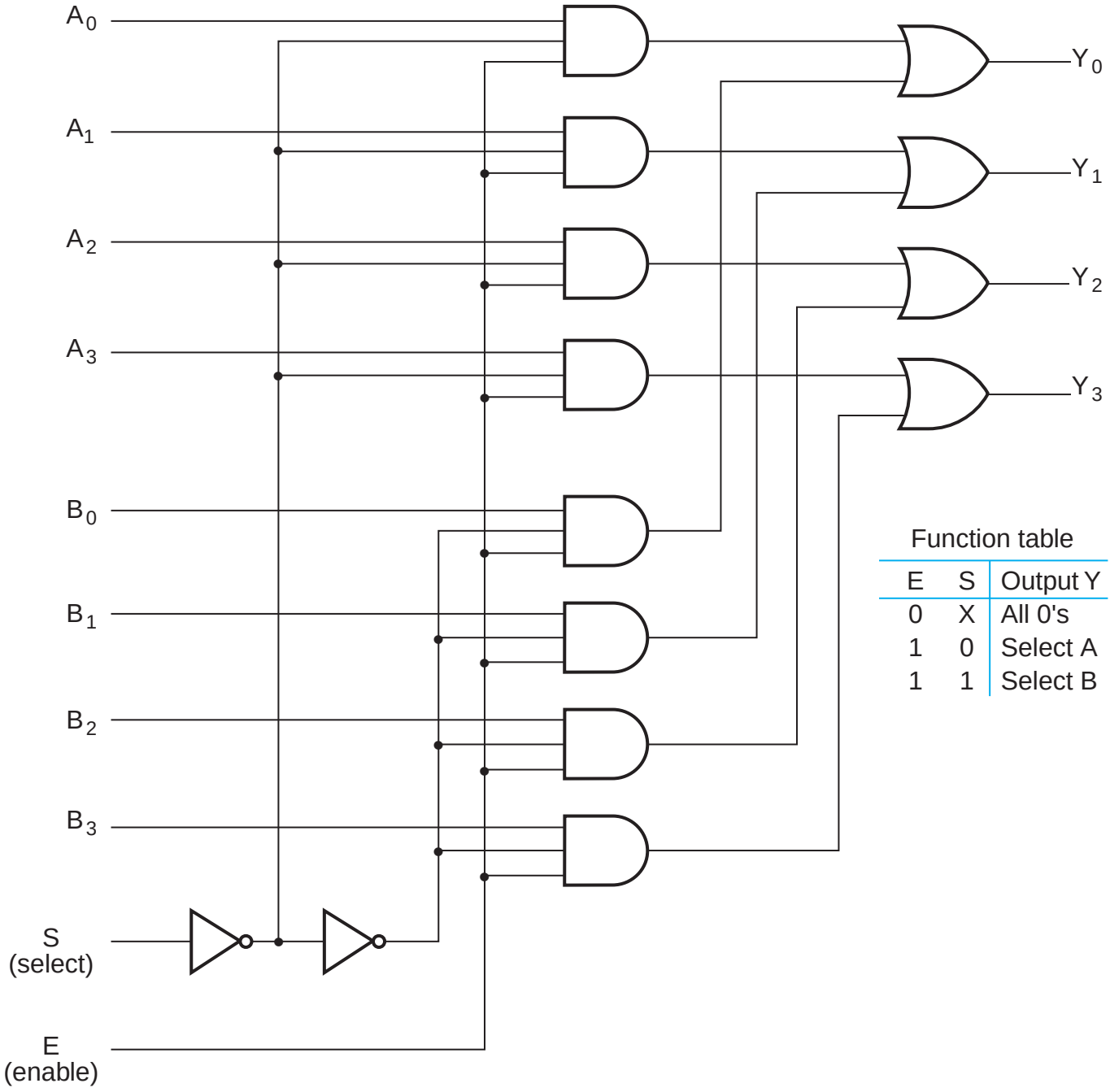
Quadruple 2–to–1-Line Multiplexer



Function table

E	S	Output Y
0	X	All 0's
1	0	Select A
1	1	Select B

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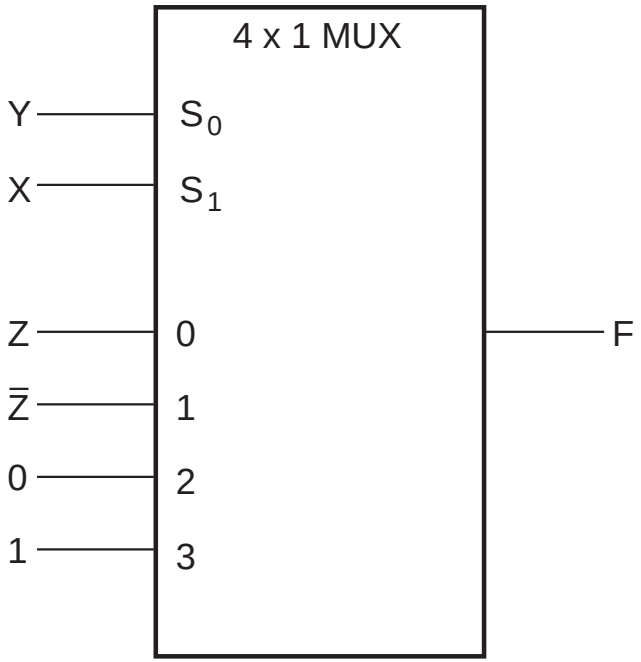
Implementing a Boolean Function with a Multiplexer

X	Y	Z	F	
0	0	0	0	F = Z
0	0	1	1	
0	1	0	1	F = $\bar{Z}$
0	1	1	0	
1	0	0	0	F = 0
1	0	1	0	
1	1	0	1	F = 1
1	1	1	1	

(a) Truth table



(b) Multiplexer implementation

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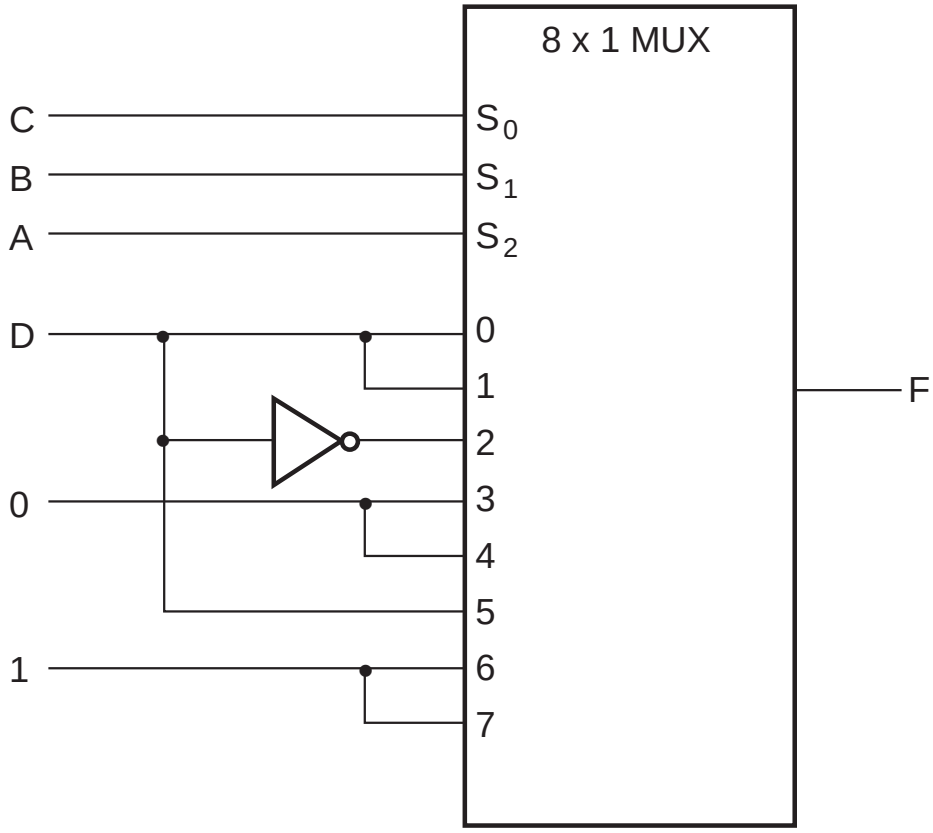
Implementing a Four-Input Function with a Multiplexer

A	B	C	D	F	
0	0	0	0	0	F = D
0	0	0	1	1	
0	0	1	0	0	F = D
0	0	1	1	1	
0	1	0	0	1	F = $\overline{D}$
0	1	0	1	0	
0	1	1	0	0	F = 0
0	1	1	1	0	
1	0	0	0	0	F = 0
1	0	0	1	0	
1	0	1	0	0	F = D
1	0	1	1	1	
1	1	0	0	1	F = 1
1	1	0	1	1	
1	1	1	0	1	F = 1
1	1	1	1	1	



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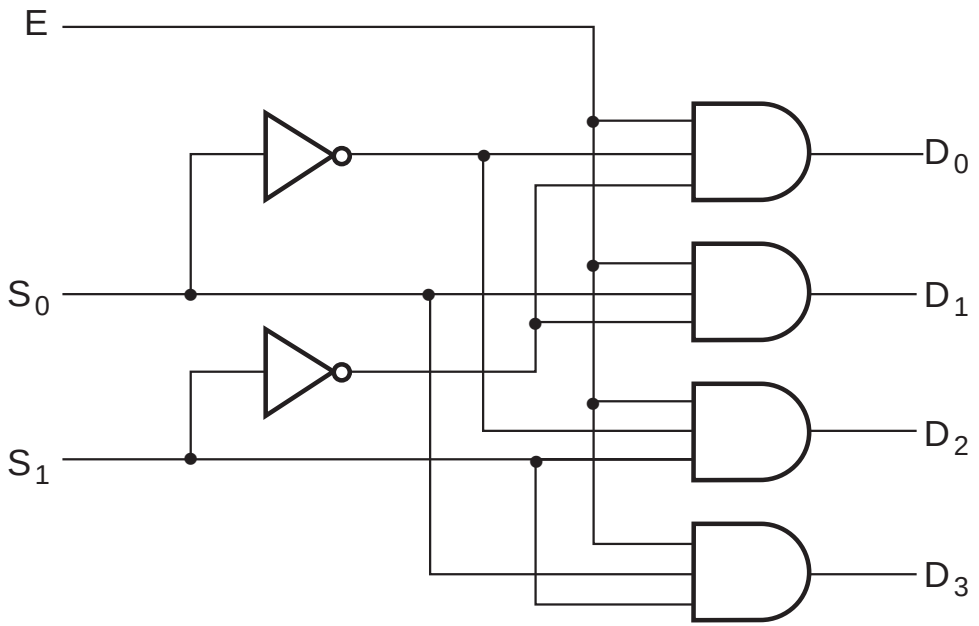
1–to–4-Line Demultiplexer



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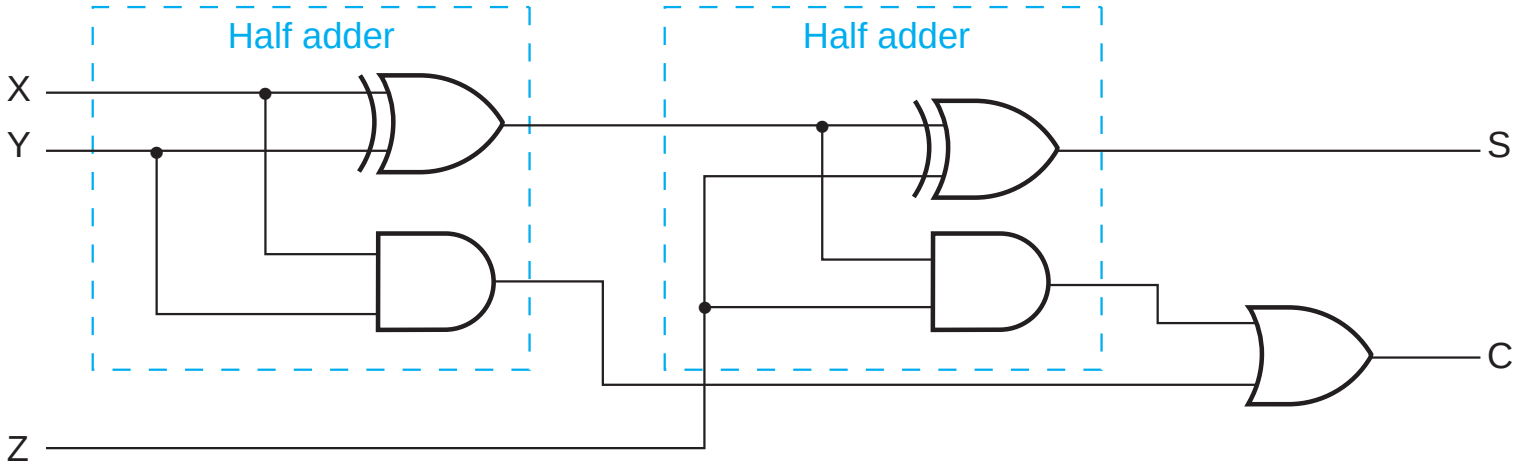
Logic Diagram of Full Adder



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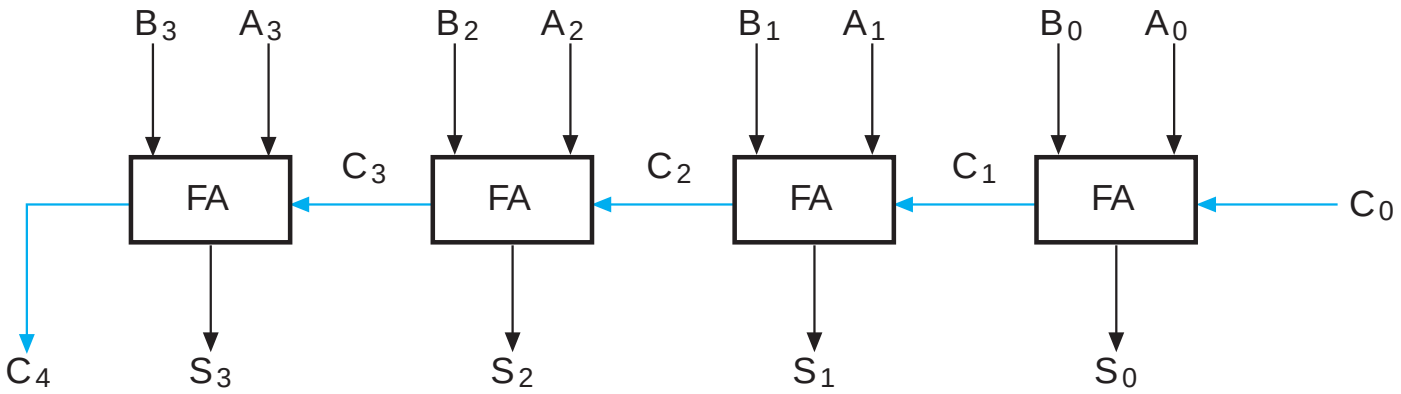
4-Bit Ripple Carry Adder



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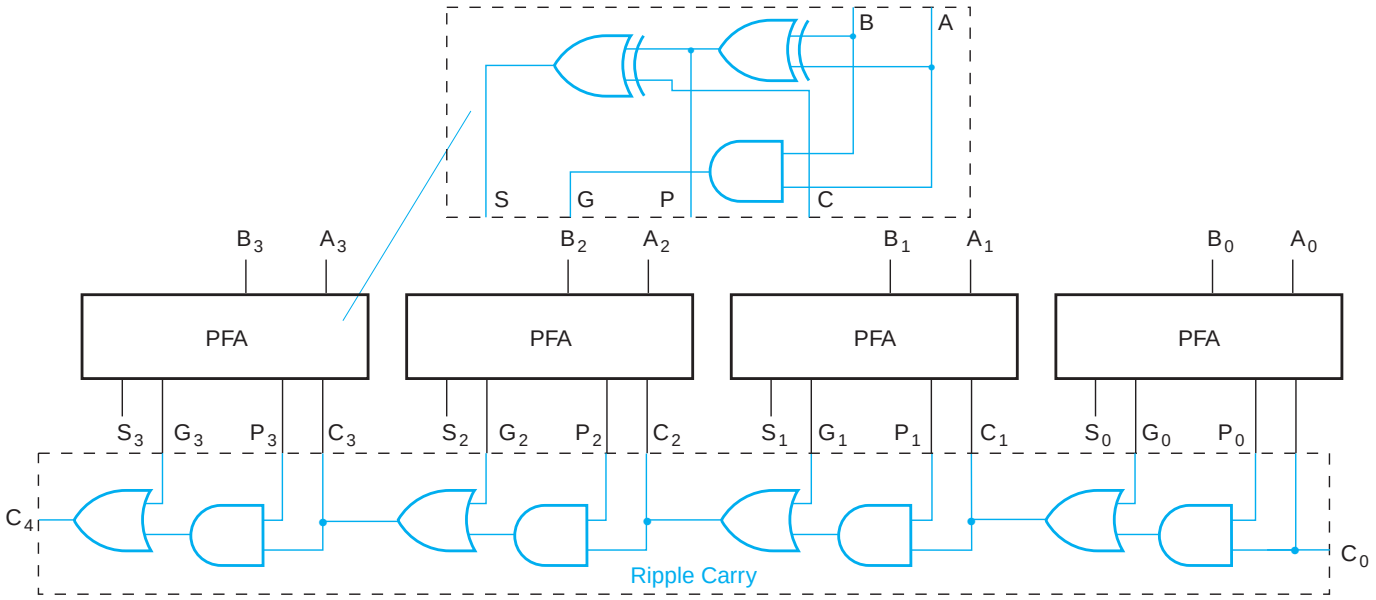
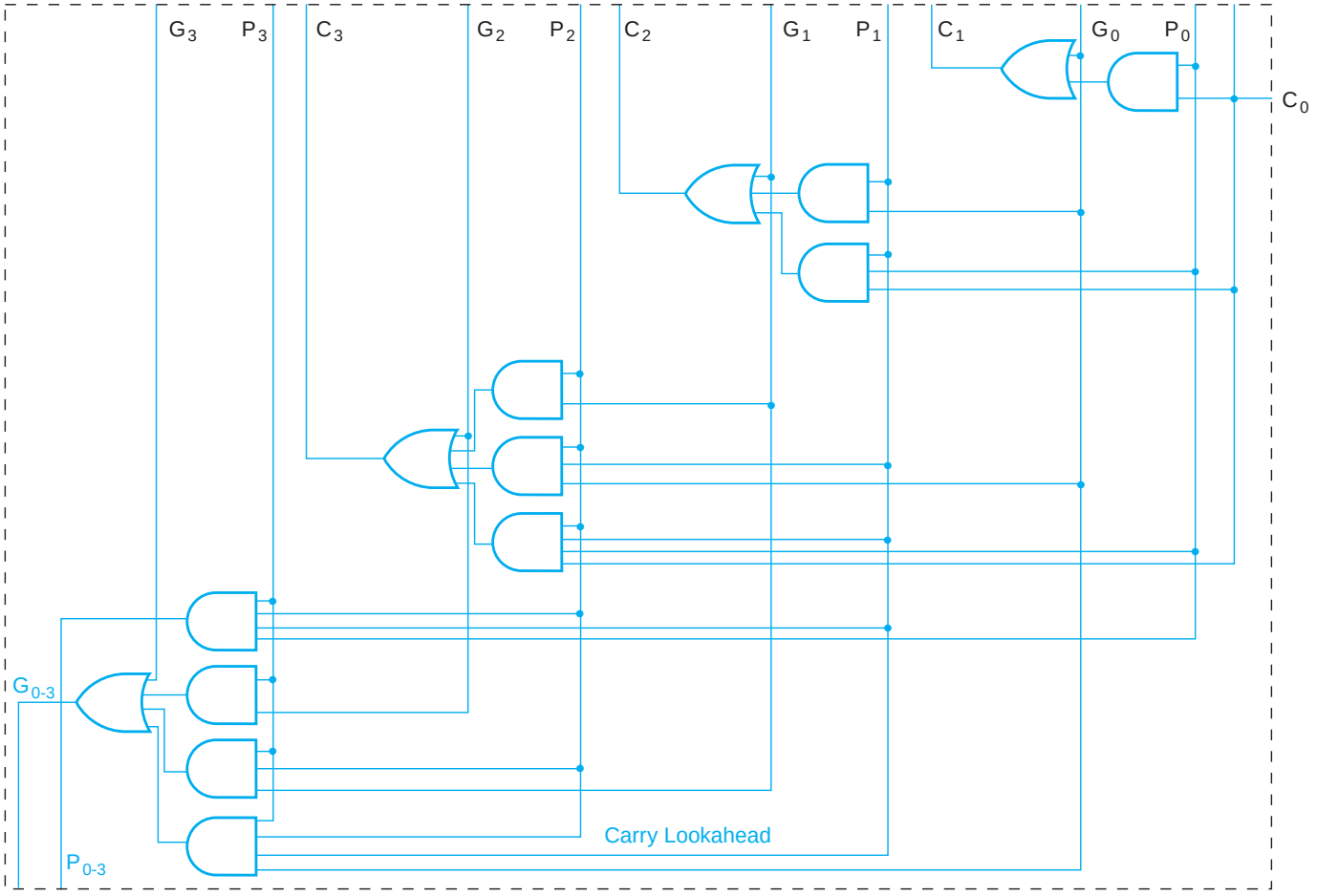
Development of a Carry Lookahead Adder



(a)



(b)

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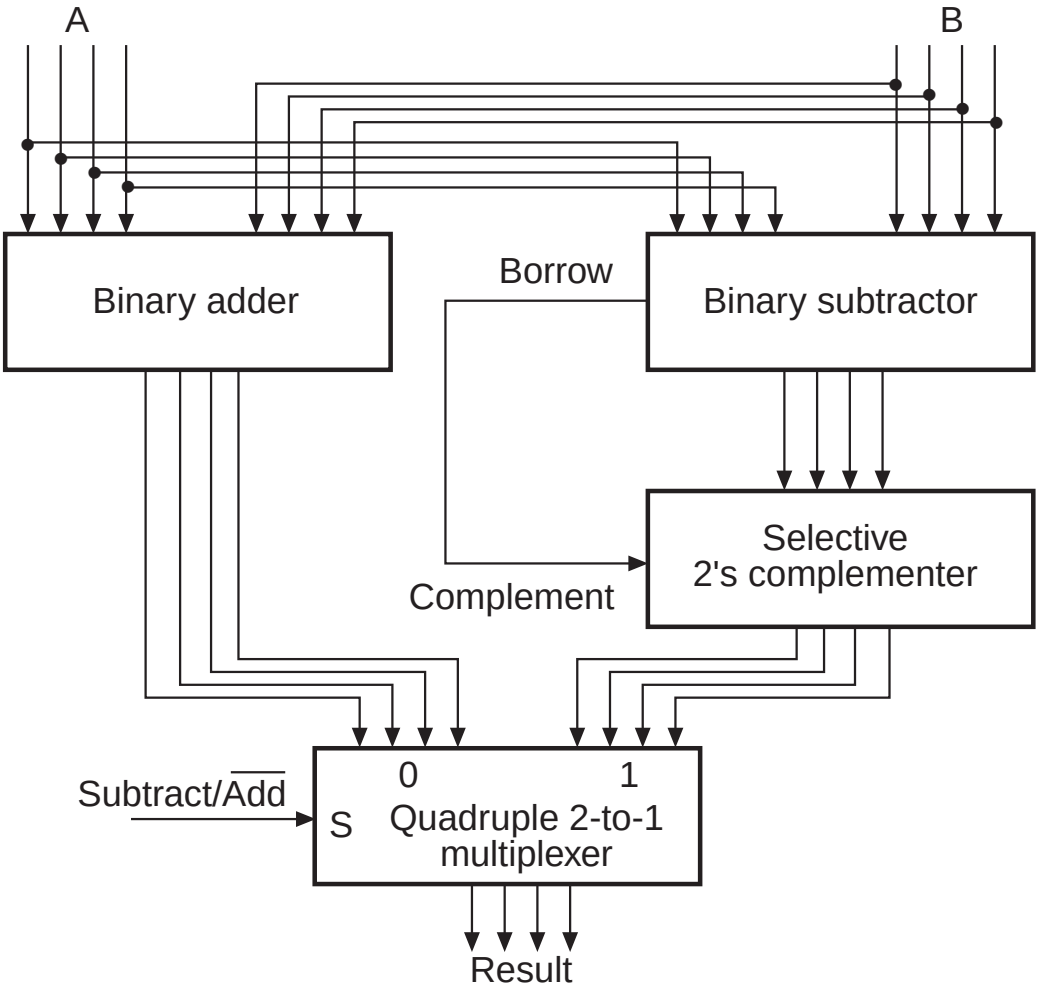
Block Diagram of Binary Adder-Subtractor



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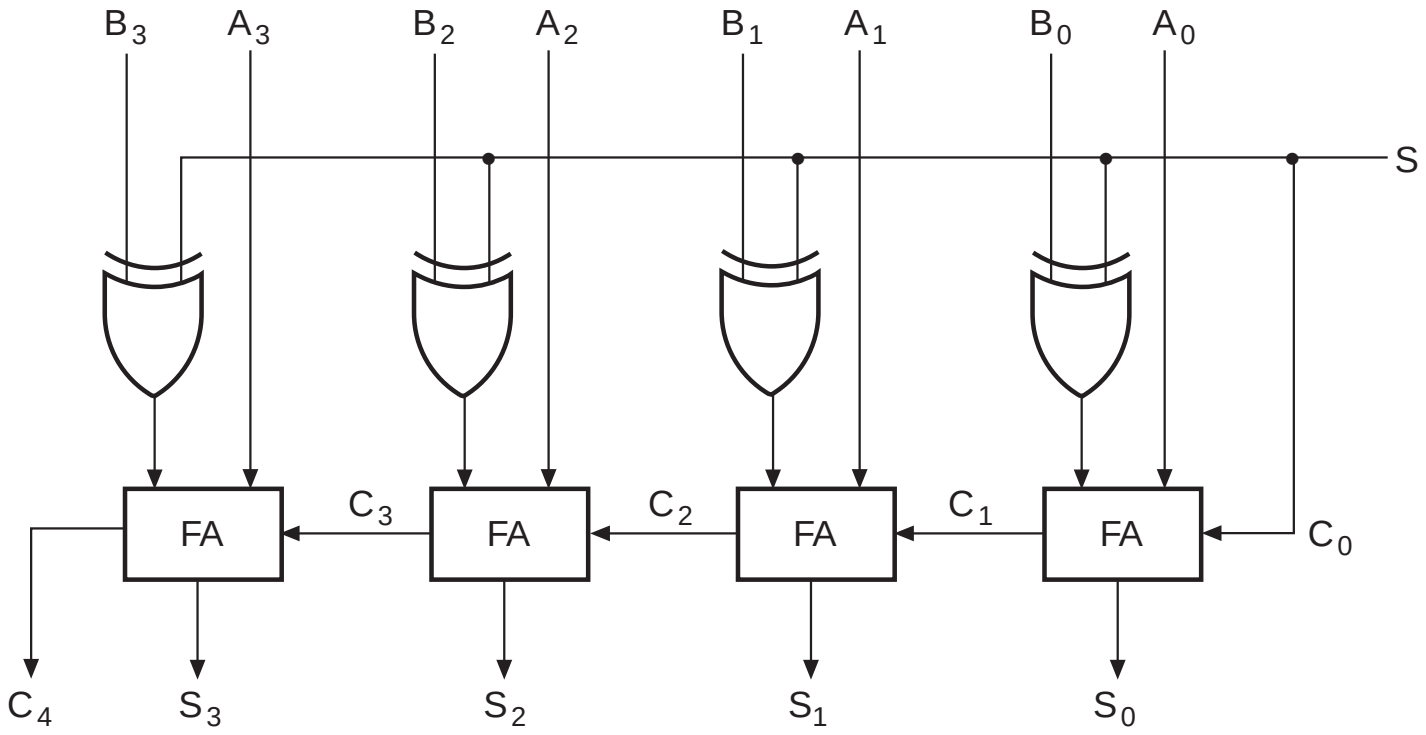
Adder-Subtractor Circuit



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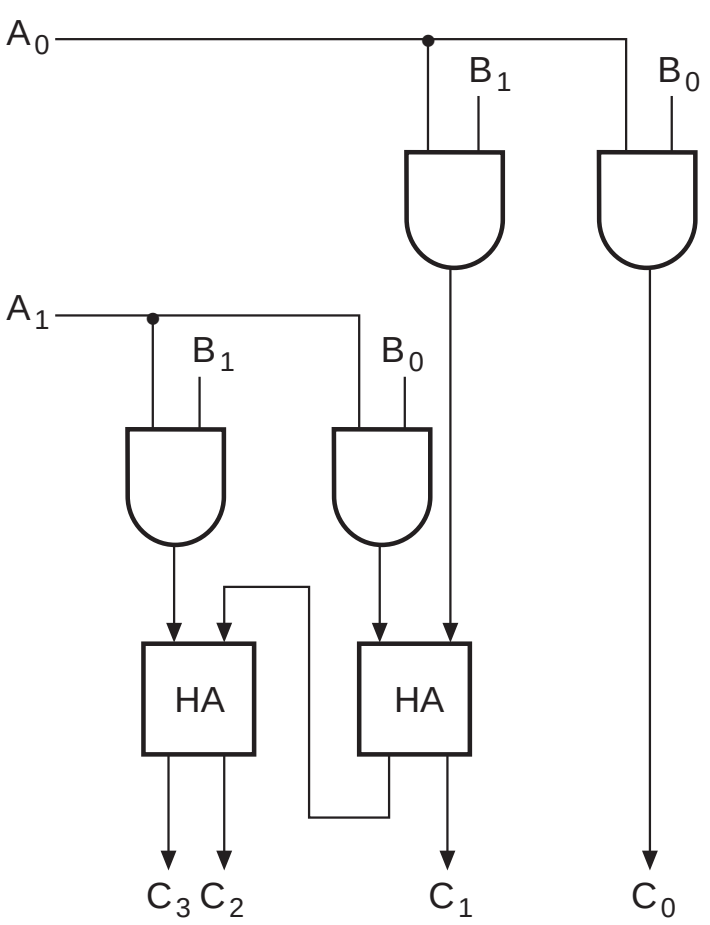
A 2-Bit by 2-Bit Binary Multiplier

$$
\begin{array}{cccc}
 & & B_1 & B_0 \\
 & & A_1 & A_0 \\
\hline
 & & A_0B_1 & A_0B_0 \\
 & A_1B_1 & A_1B_0 & \\
\hline
C_3 & C_2 & C_1 & C_0
\end{array}
$$



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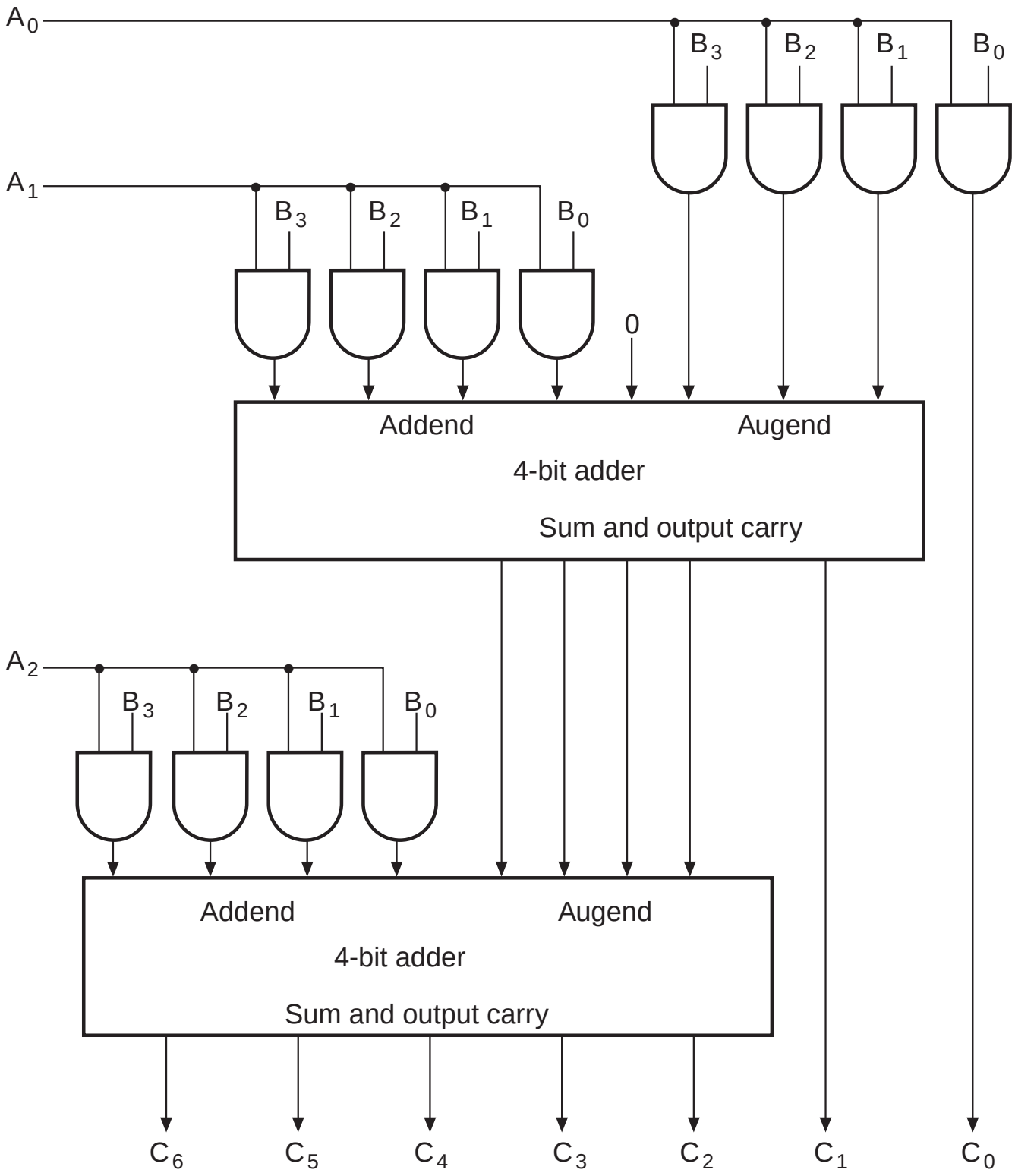
A 4-Bit by 3-Bit Binary Multiplier



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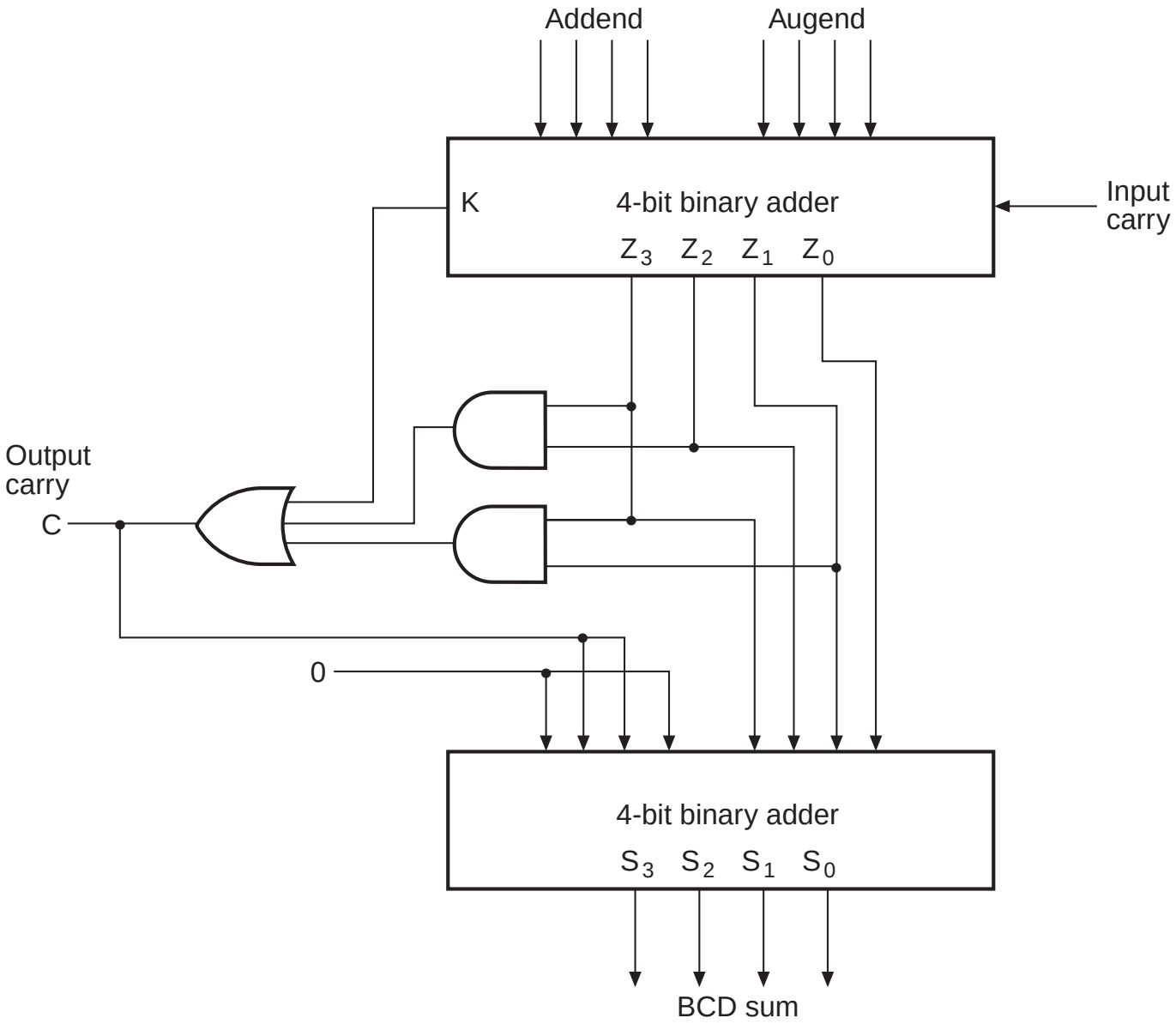
Block Diagram of BCD Adder



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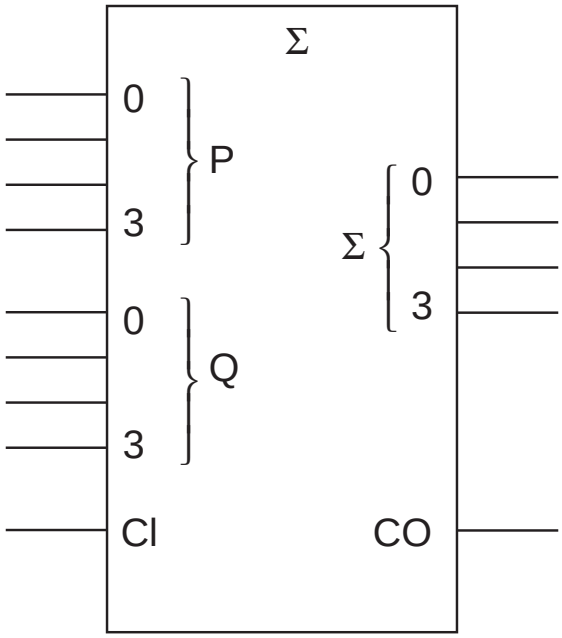
Standard Graphics Symbol for a 4-Bit Parallel Adder



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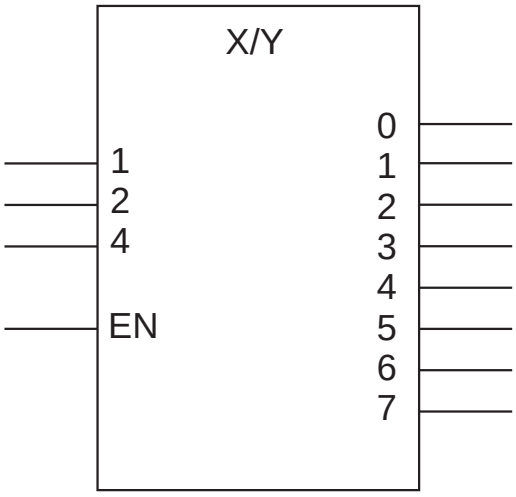
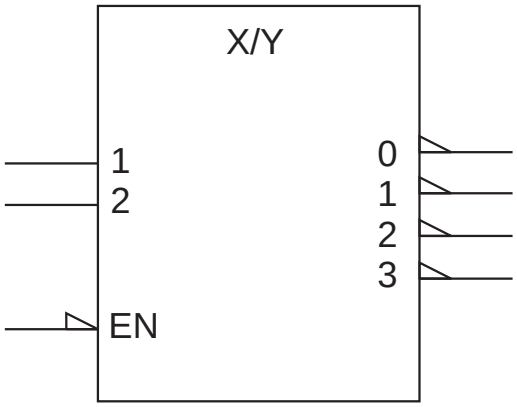
Standard Graphics Symbols for Decoders



(a) 3-to-8 line



(b) 2-to-4 line

EN	A_1	A_0	D_0	D_1	D_2	D_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

(c) Truth table for decoder in (b) with EN and outputs negative logic

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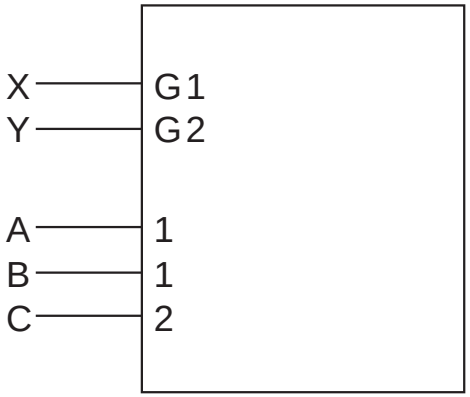
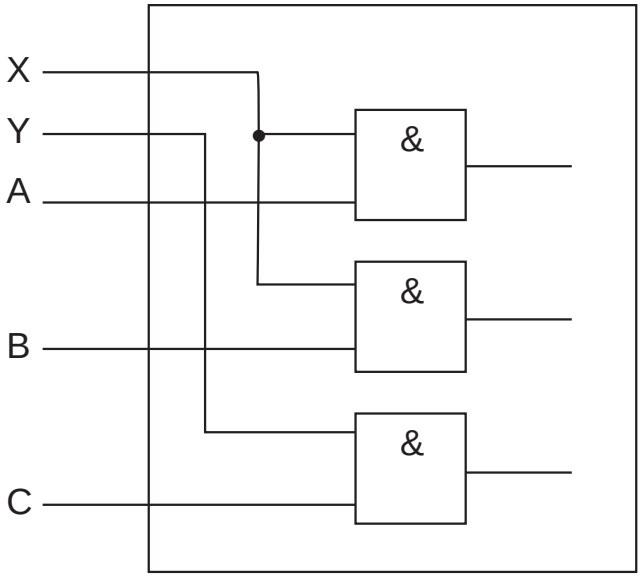
Example of a G-(AND) Dependency



(a) Block with G 1 and G 2



(b) Equivalent interpretation

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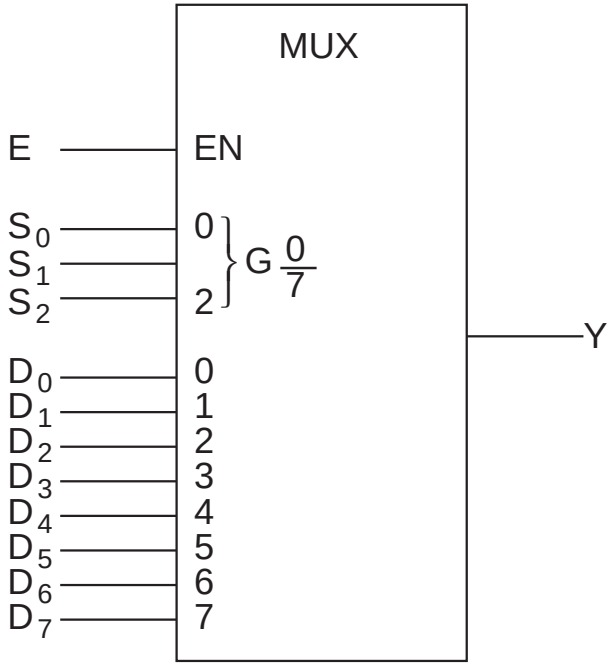
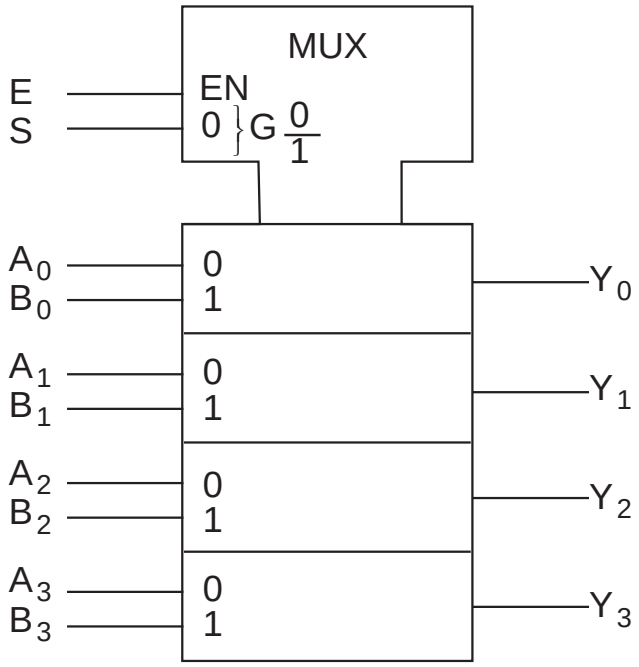
Standard Graphics Symbols for Multiplexers



(a) 8–to–1 line



(b) Quadruple 2–to–1 line

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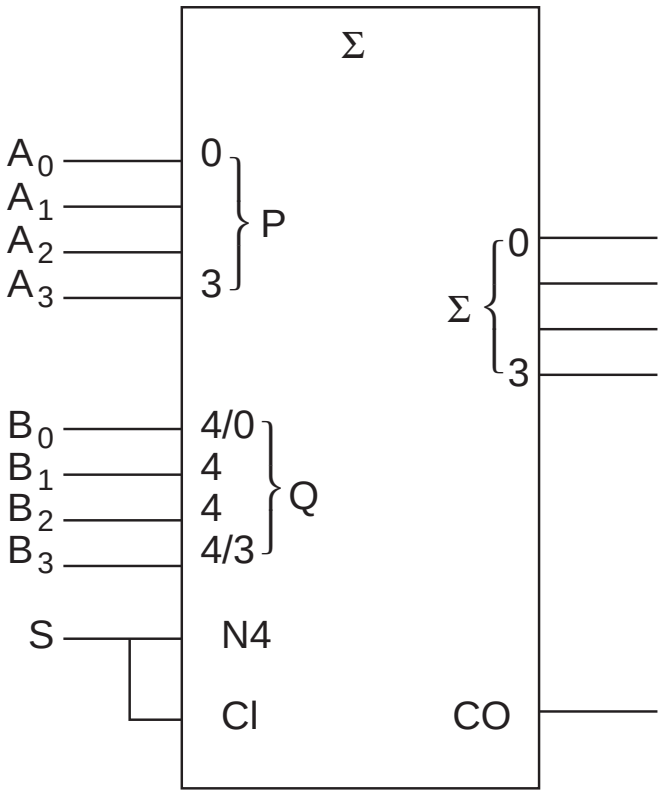
Graphics Symbol for an Adder-Subtractor



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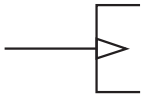
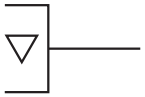
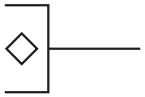
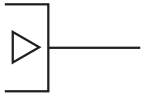
Qualifying Symbols Associated with Inputs and Outputs

Symbol	Description
	Active-low input or output
	Logic negation input or output
	Enable input: enables all outputs when active
	Dynamic input
	Three-state output
	Open-circuit output
	Output with special amplification

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