ROM Truth Table (Partial)

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		.							.			
		.							.			
		.							.			
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

Truth Table for Circuit of Example 6-1

Inputs			Outputs						
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

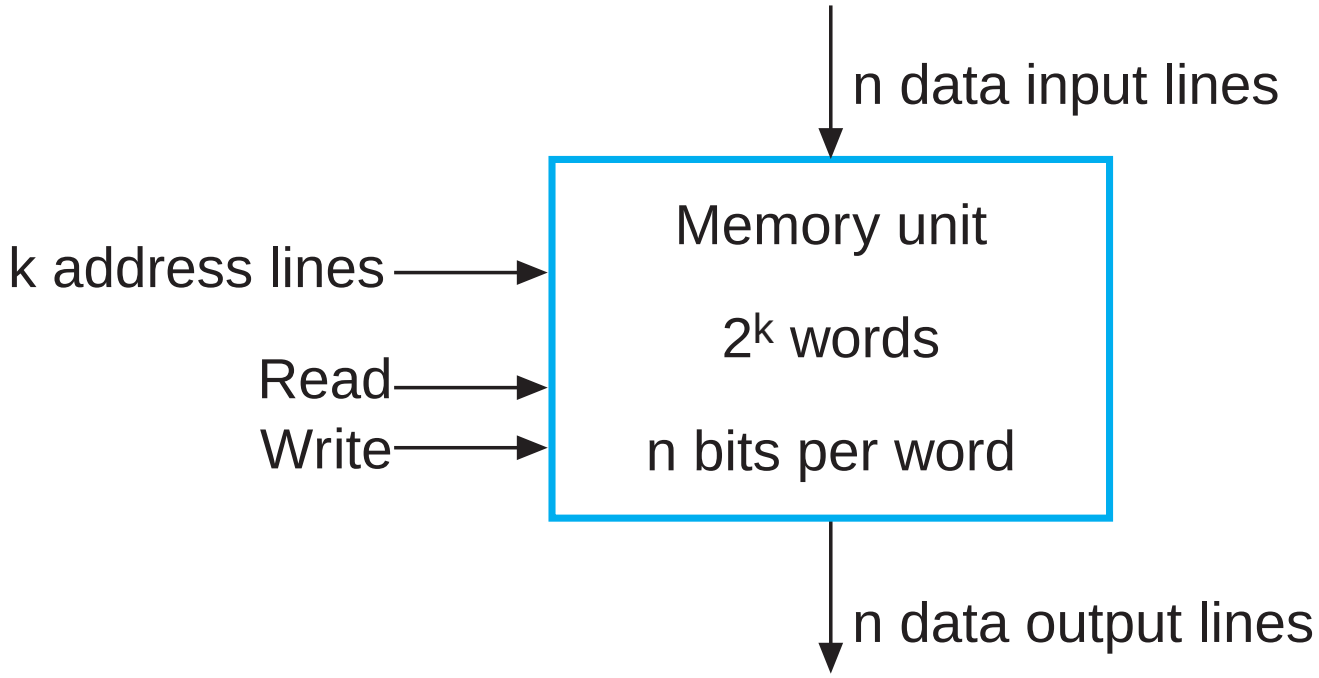
Programming Table for the PLA in Figure 6-20

	Product term	Inputs			Outputs	
		A	B	C	(T) F_1	(C) F_2
$A\overline{B}$	1	1	0	—	1	—
AC	2	1	—	1	1	1
BC	3	—	1	1	—	1
$\overline{A}B\overline{C}$	4	0	1	0	1	—

PAL® Programming Table

Product term	AND Inputs A	B	C	D	W	Outputs
1	1	1	0	—	—	$W = A B \overline{C}$
2	0	0	1	0	—	$+ \overline{A}\,\overline{B} C \overline{D}$
3	—	—	—	—	—	
4	1	—	—	—	—	$X = A$
5	—	1	1	1	—	$+ BCD$
6	—	—	—	—	—	
7	0	1	—	—	—	$Y = \overline{A} B$
8	—	—	1	1	—	$+ CD$
9	—	0	—	0	—	$+ \overline{B}\,\overline{D}$
10	—	—	—	—	1	$Z = W$
11	1	—	0	0	—	$+ A \overline{C}\,\overline{D}$
12	0	0	0	1	—	$+ \overline{A}\,\overline{B}\,\overline{C} D$

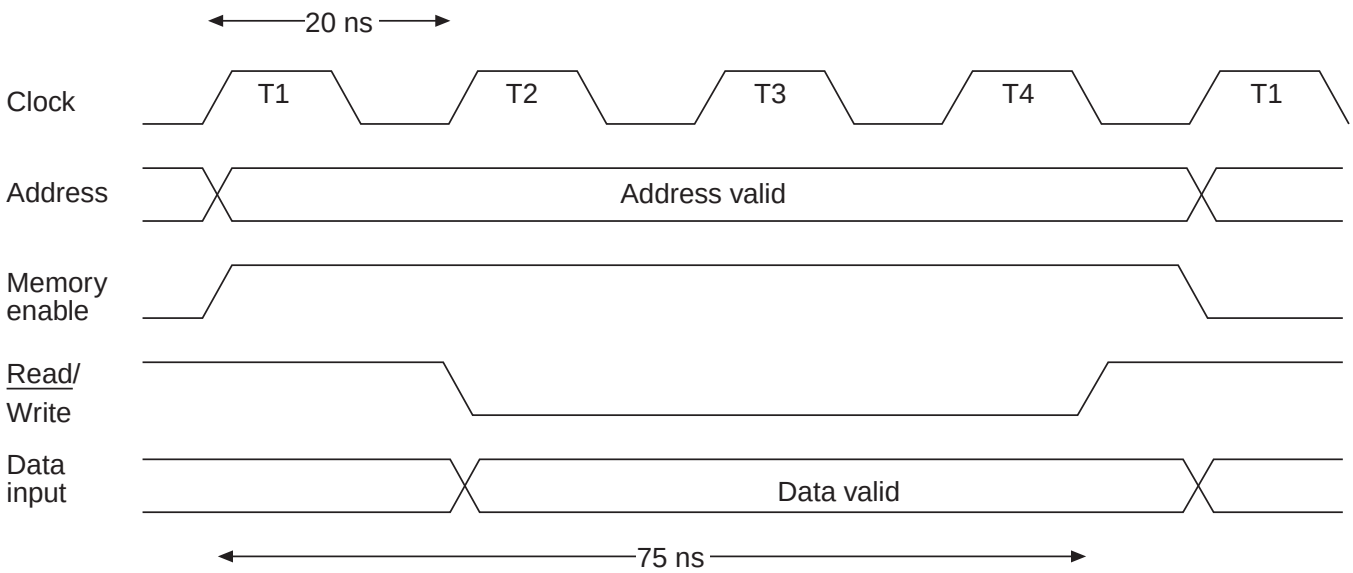
Block Diagram of Memory



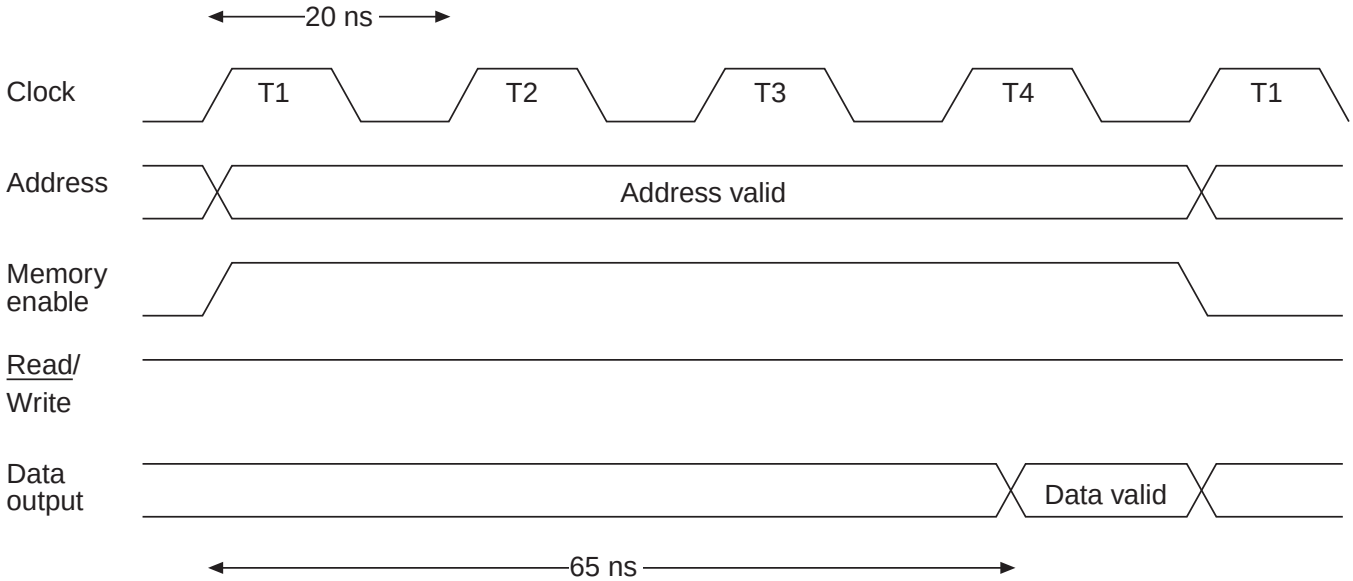
Contents of a 1024 x 16 Memory

Memory address		Memory contents
Binary	Decimal	
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	•	•
	•	•
	•	•
	•	•
	•	•
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

Memory Cycle Timing Waveforms

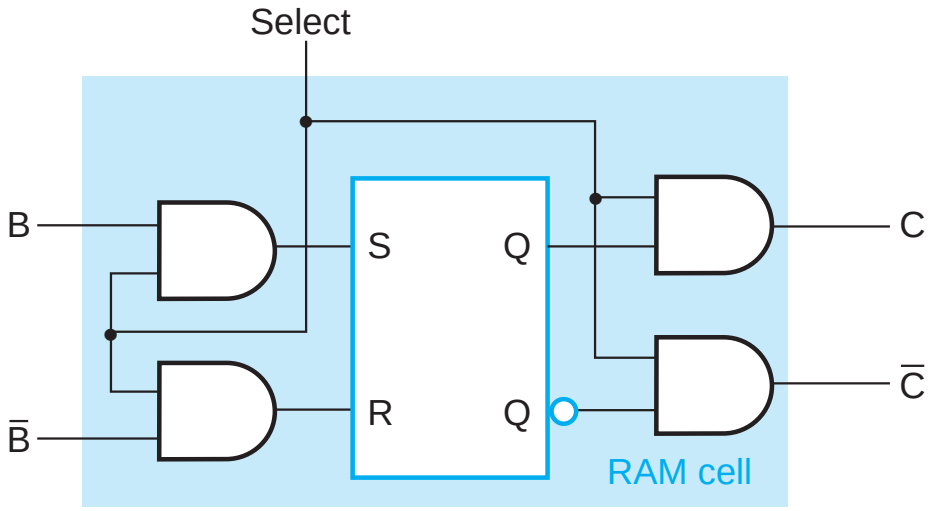


(a) Write cycle

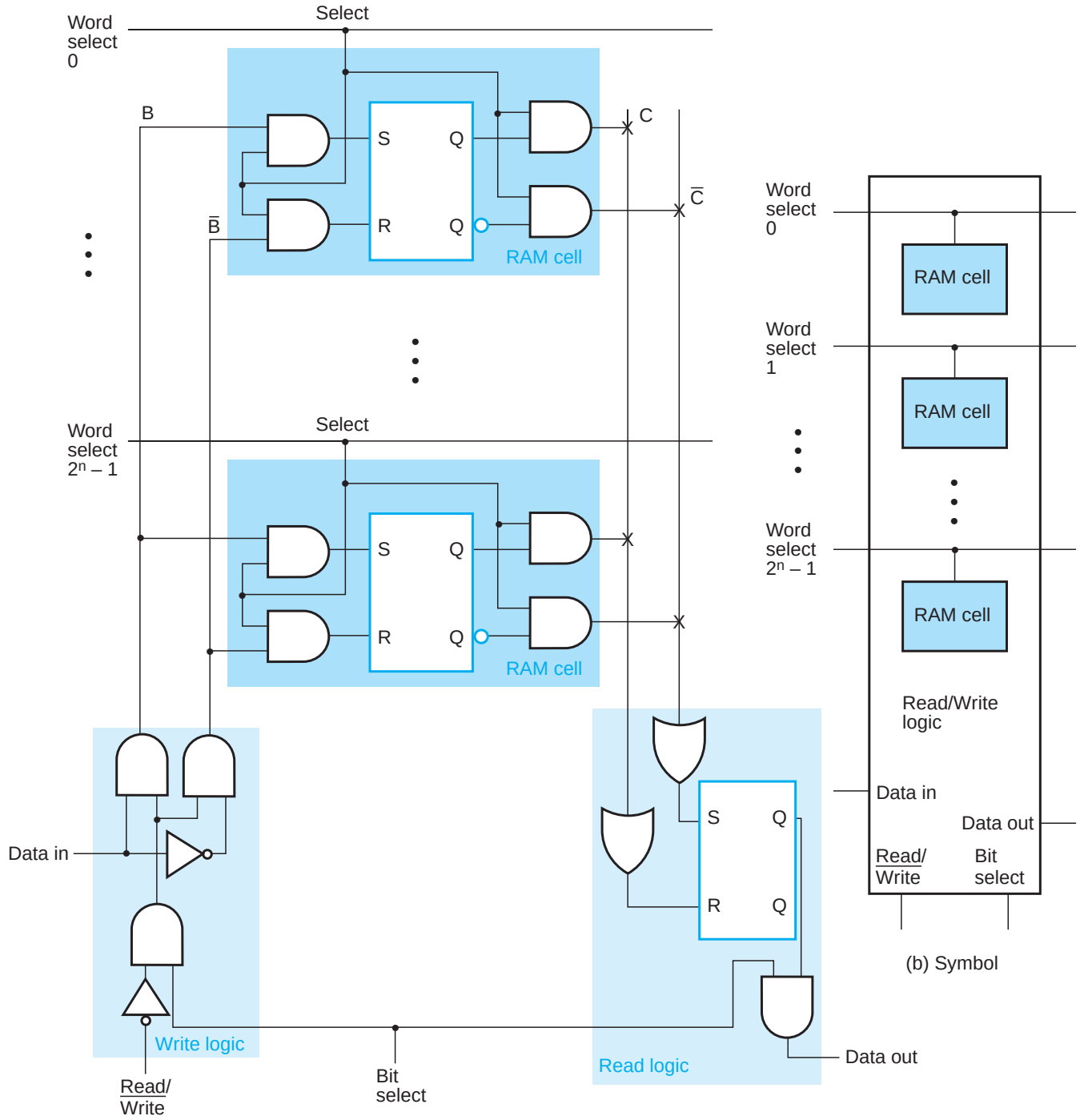


(b) Read cycle

Static RAM Cel



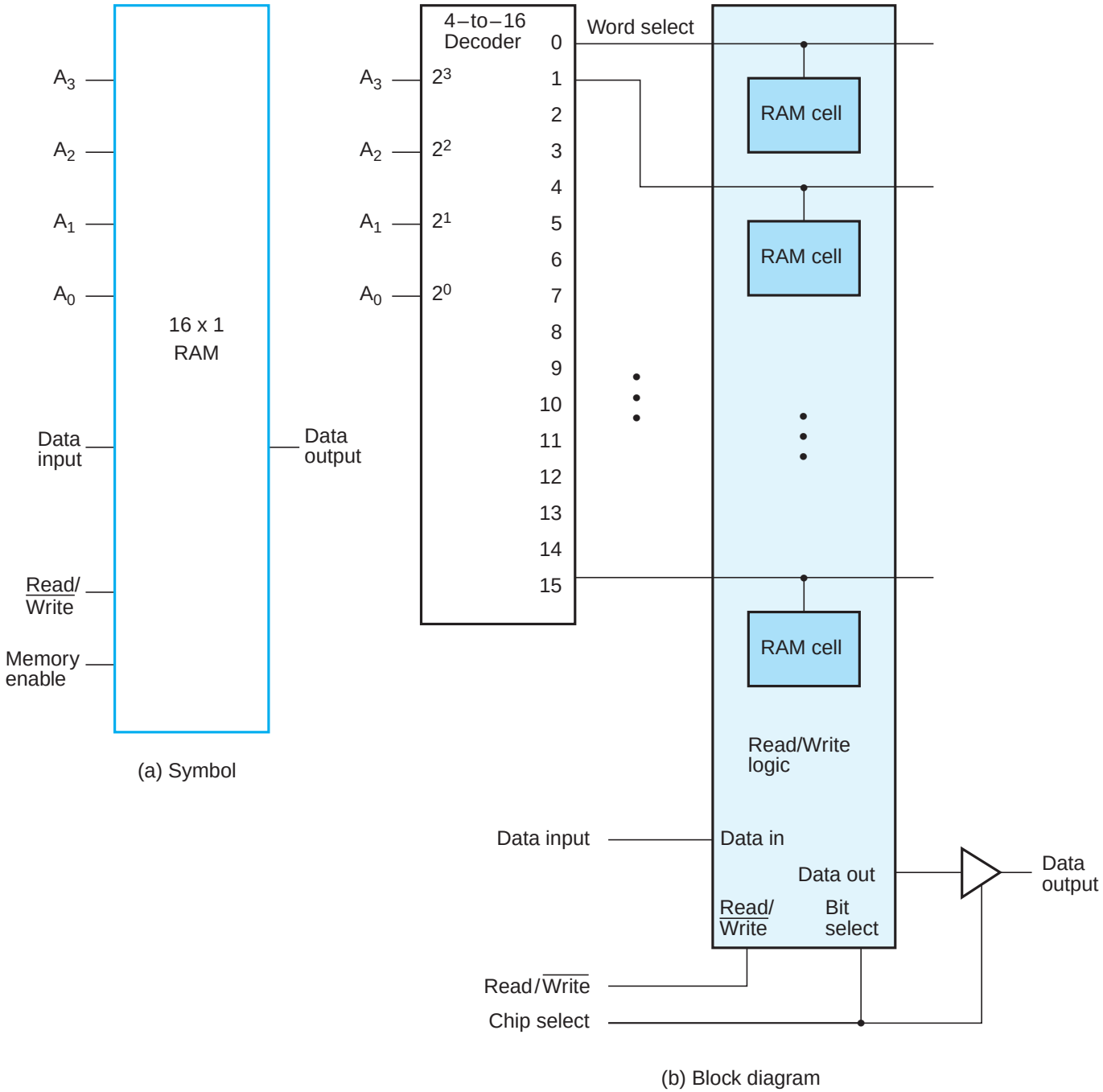
RAM Bit Slice Model



(a) Logic diagram

(b) Symbol

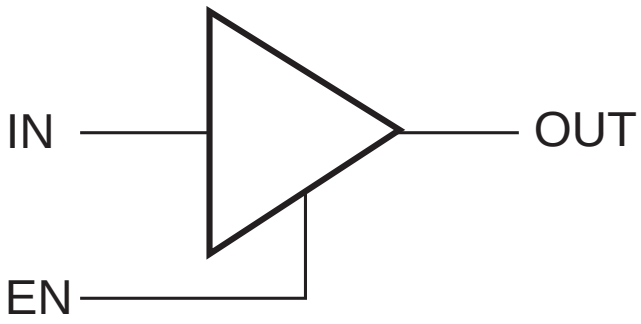
16-Word by 1-Bit RAM Chip



(a) Symbol

(b) Block diagram

Three-state Buffer

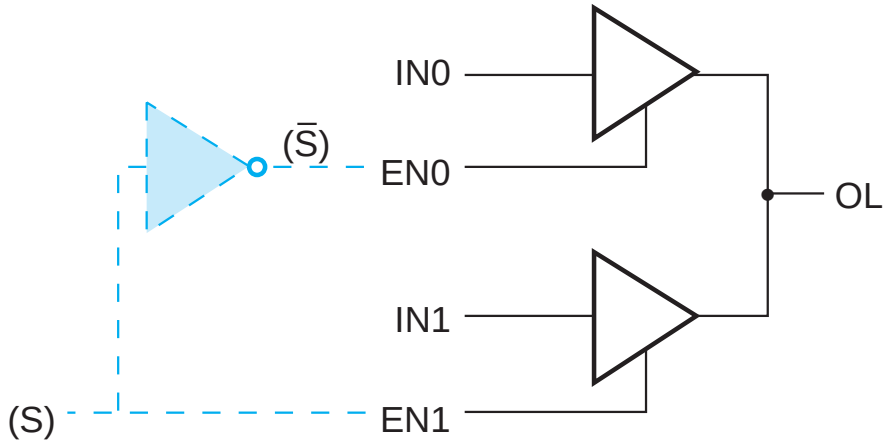


(a) Logic symbol

EN	IN	OUT
0	X	Hi-Z
1	0	0
1	1	1

(b) Truth table

Three-state Buffers Forming a Multiplexed Line OL

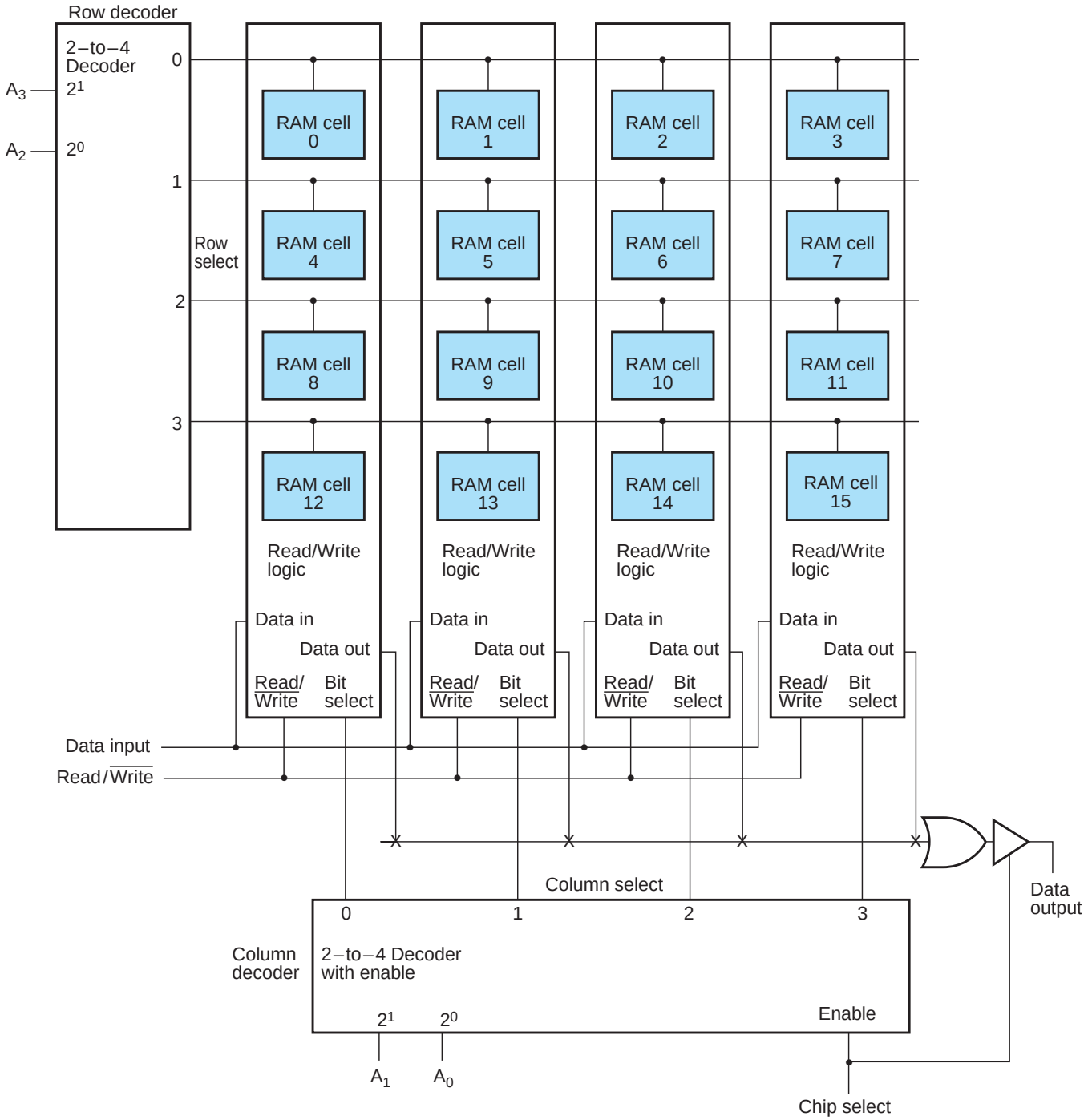


(a) Logic Diagram

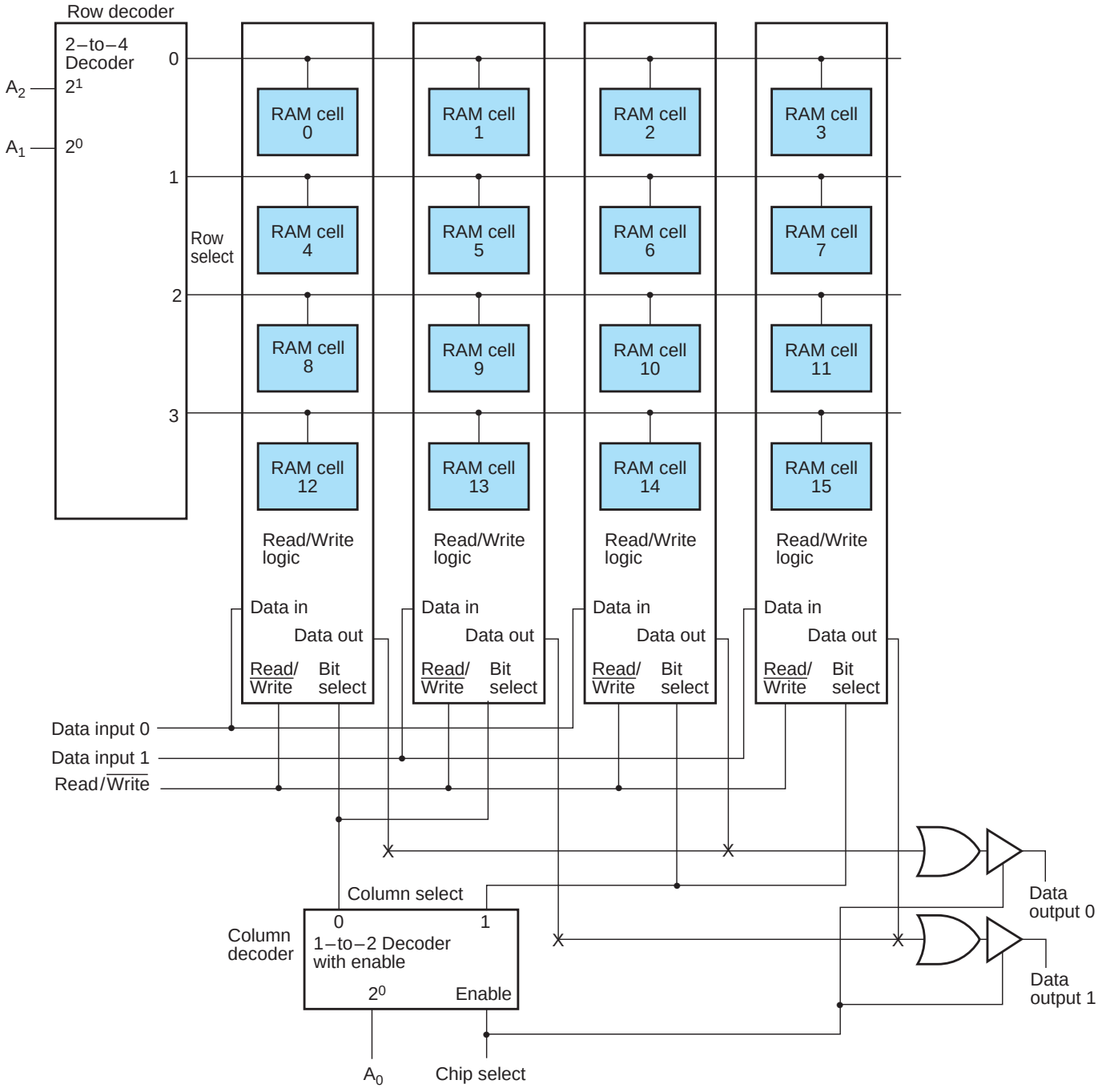
EN1	EN0	IN1	IN0	OL
0	0	X	X	Hi-Z
(S) 0	(S̄)1	X	0	0
0	1	X	1	1
1	0	0	X	0
1	0	1	X	1
1	1	0	0	0
1	1	1	1	1
1	1	0	1	
1	1	1	0	

(b) Truth table

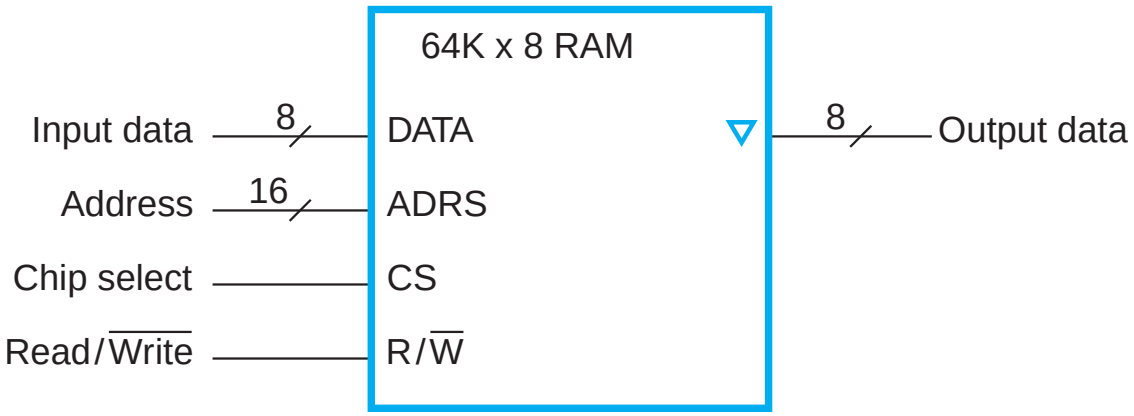
T-137 Diagram of a 16 x 1 RAM Using a 4 x 4 RAM Cell Array



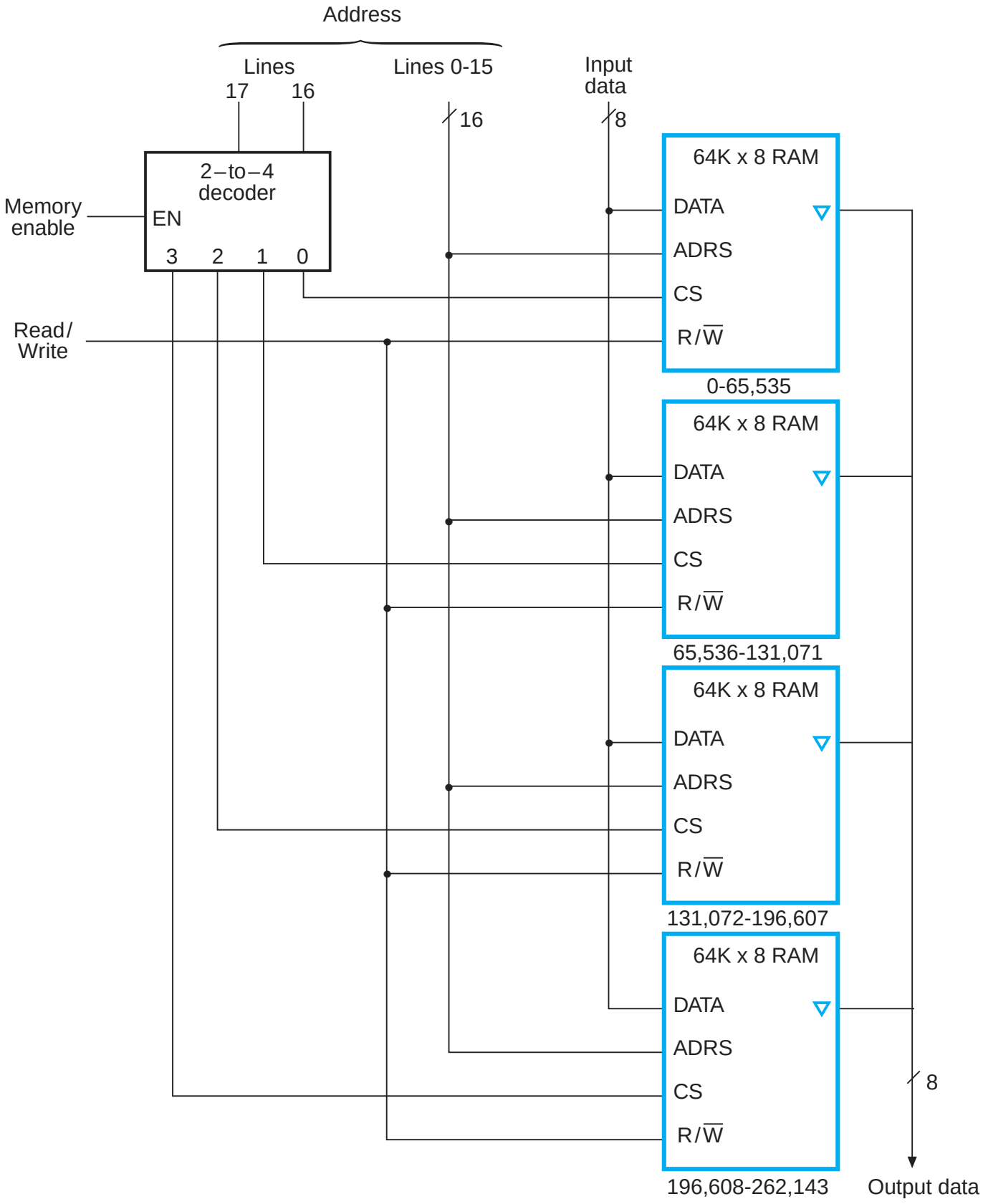
T-138 Block Diagram of an 8 x 2 RAM Using a 4 x 4 RAM Cell Array



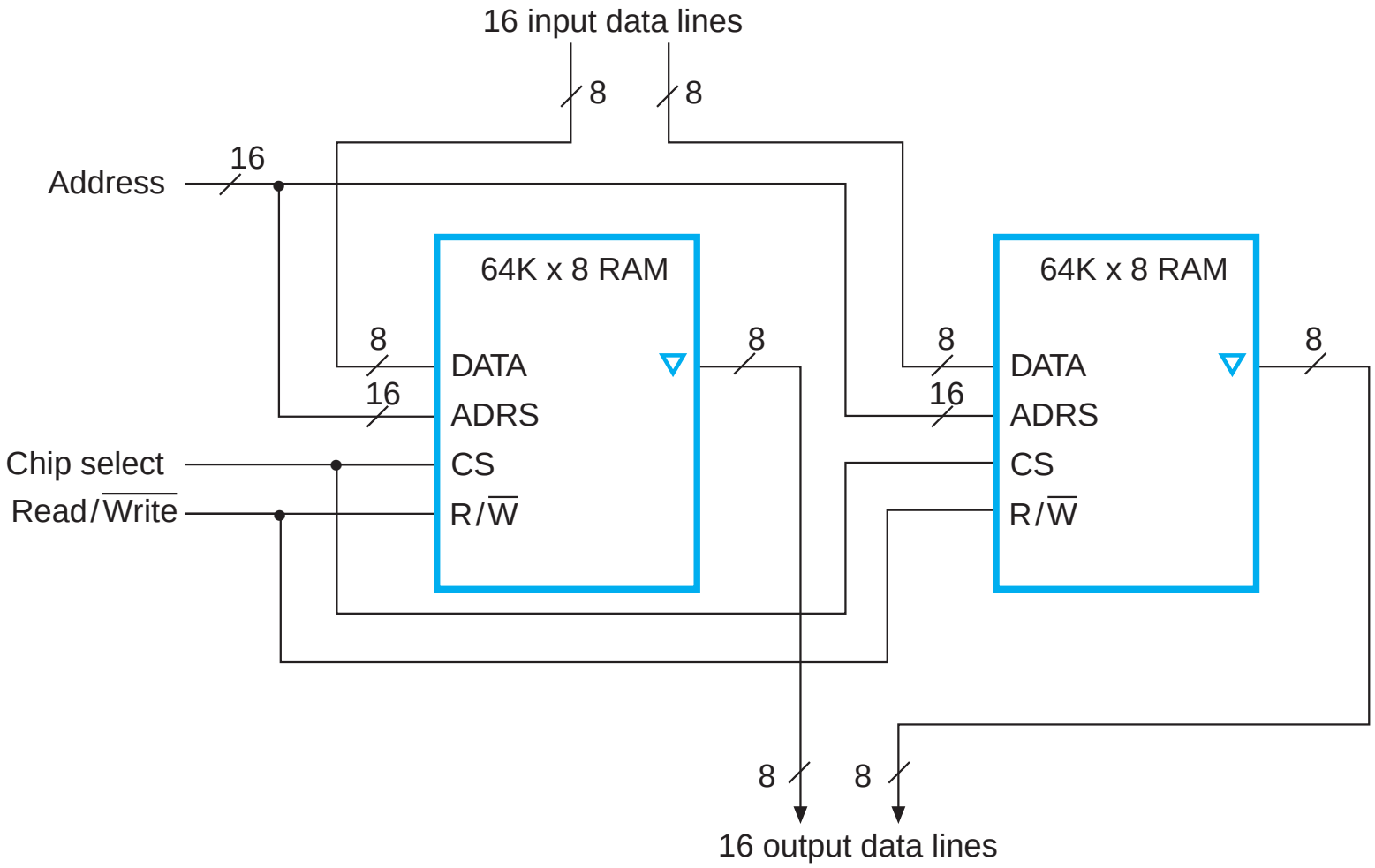
Symbol for a 64K x 8 RAM Chip



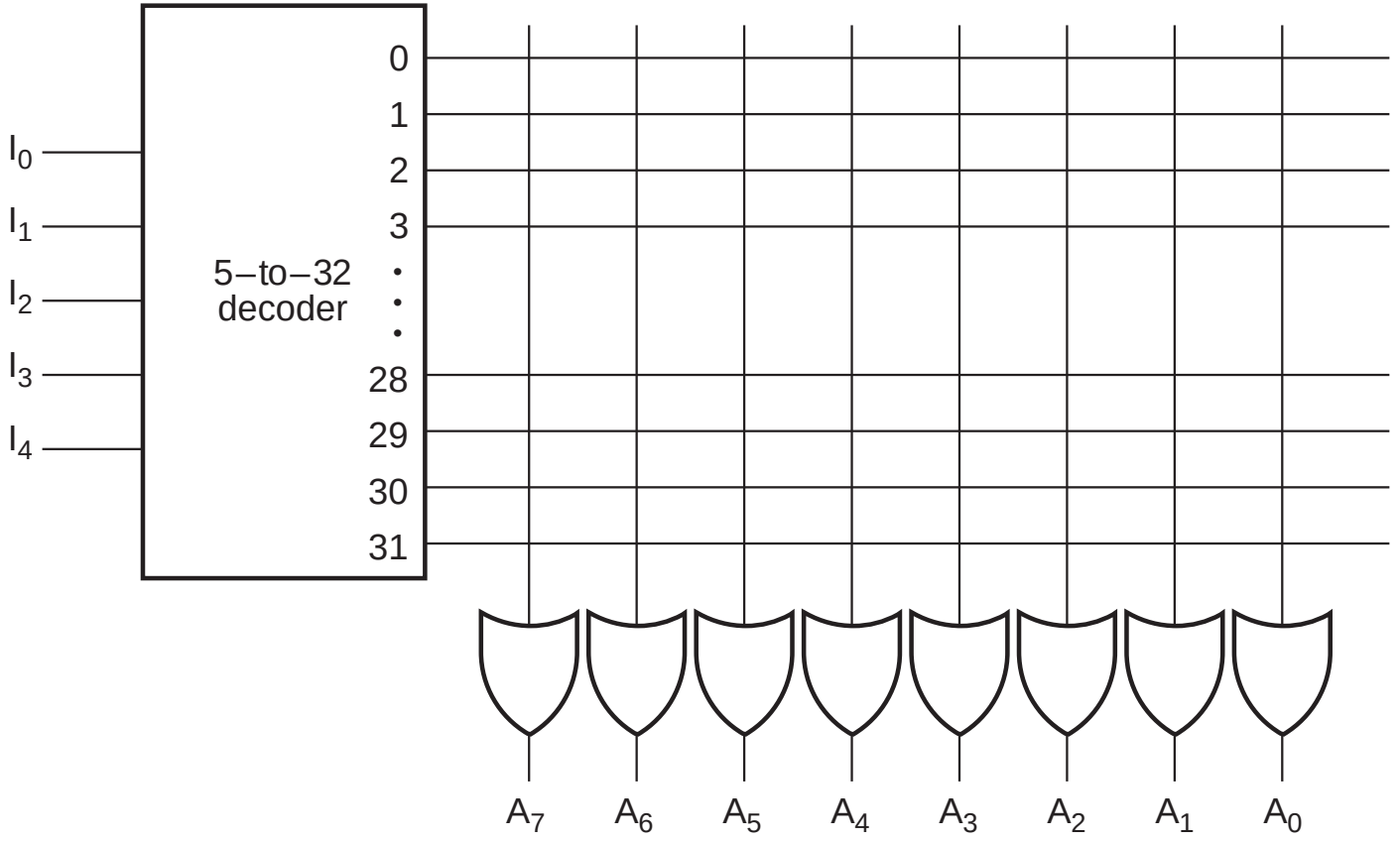
Block Diagram of a 256K x 8 RAM



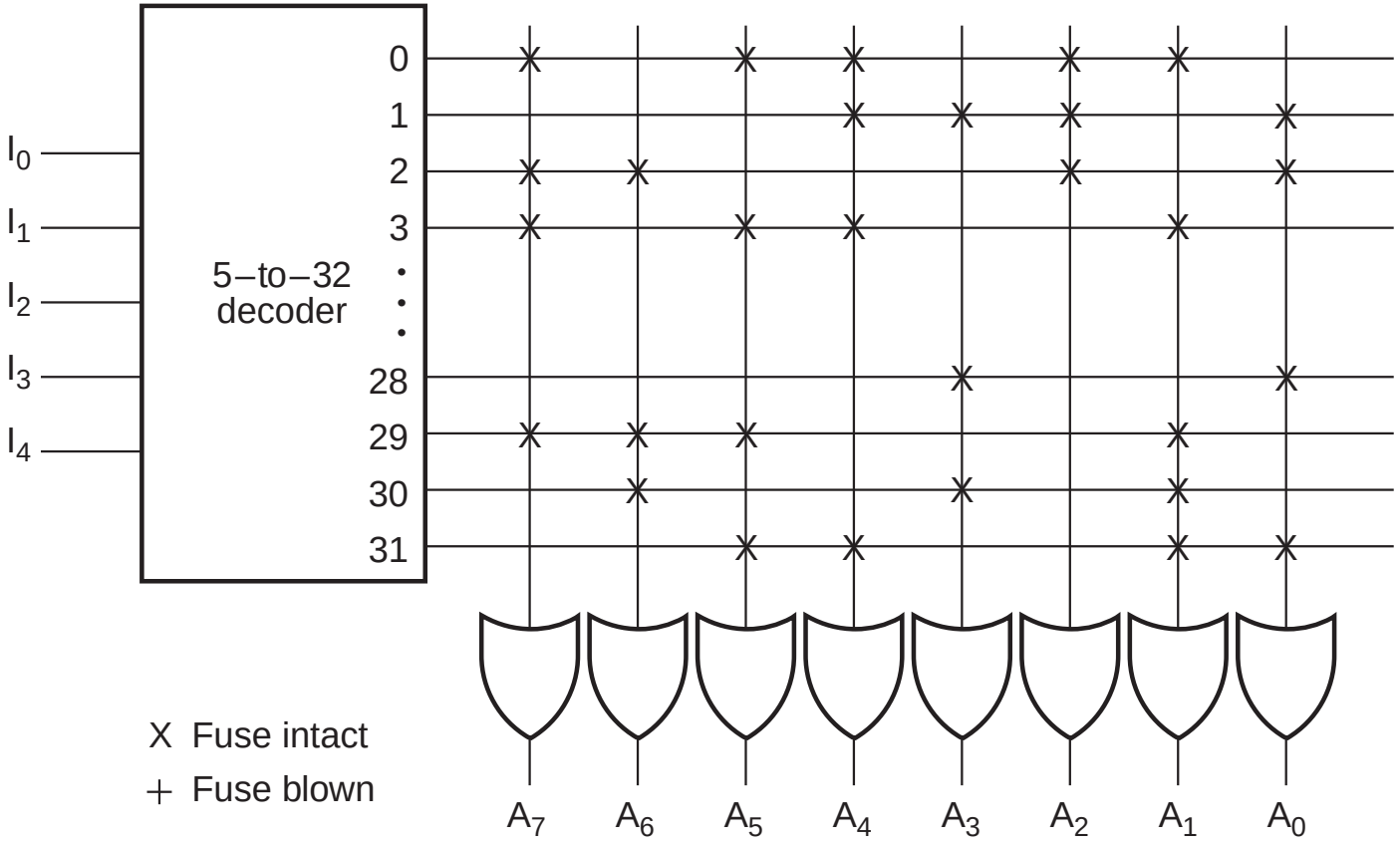
Block Diagram of a 64K x 16 RAM



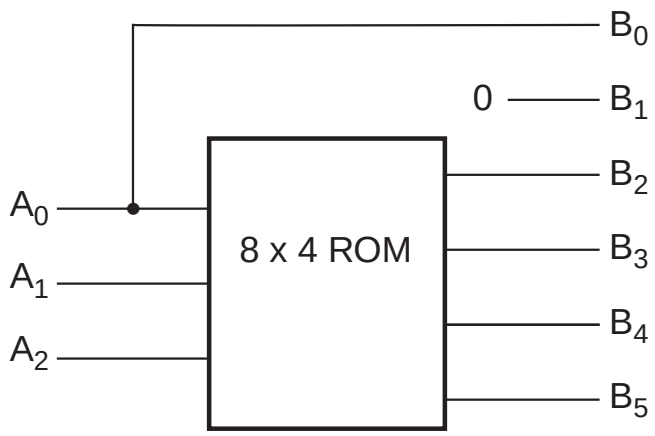
Internal Logic of a 32 x 8 ROM



Programming the ROM According to Table 6-2



ROM Implementation of Example 6-1

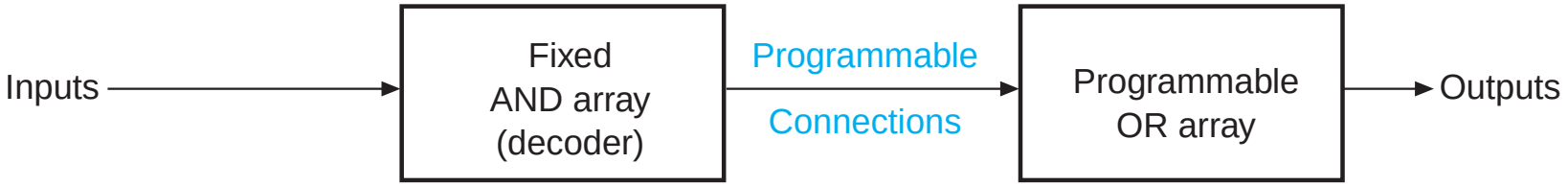


(a) Block diagram

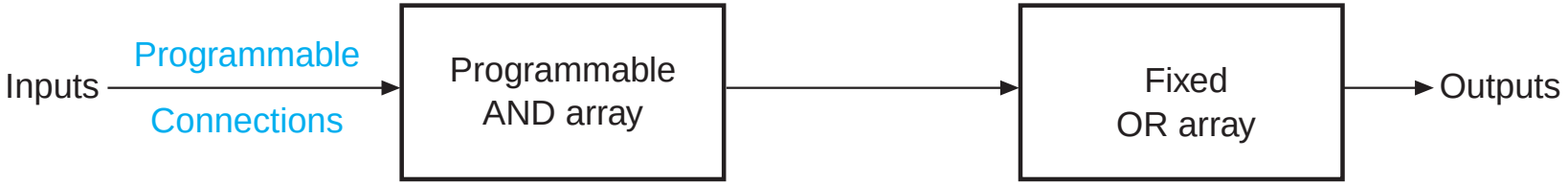
A_2	A_1	A_0	B_5	B_4	B_3	B_2
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

(b) ROM truth table

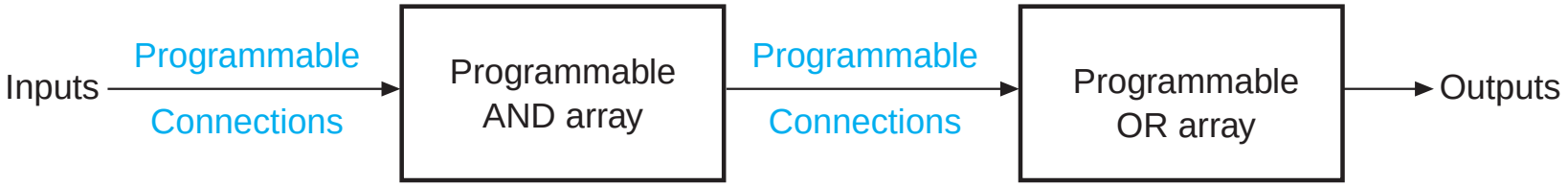
Basic Configuration of Three PLDs



(a) Programmable read-only memory (PROM)

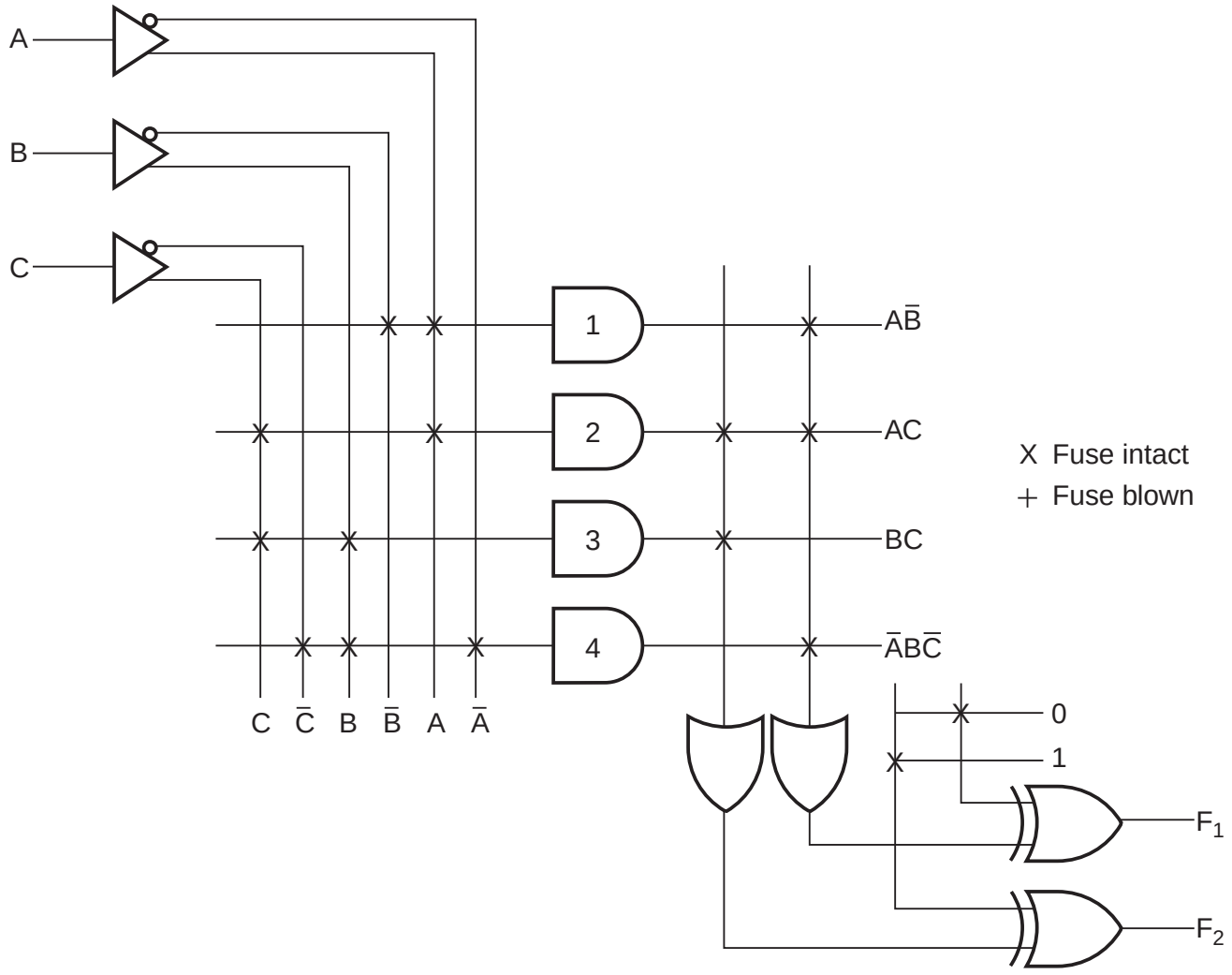


(b) Programmable array logic (PAL) device

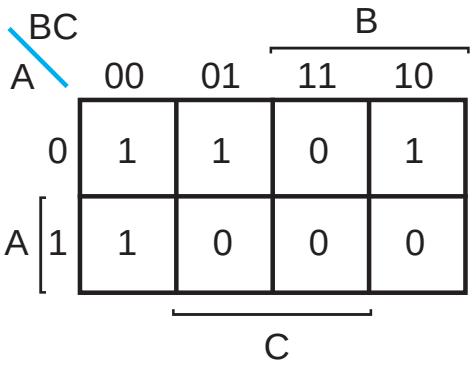


(c) Programmable logic array (PLA) device

T-146 PLA with Three Inputs, Four Product Terms, and Two Outputs

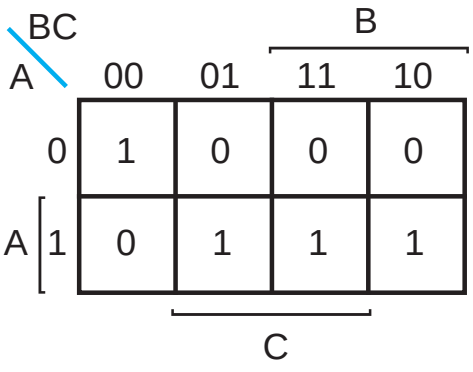


Solution to Example 6-2



$F_1 = \overline{A}\,\overline{B} + \overline{A}\,\overline{C} + \overline{B}\,\overline{C}$

$\overline{F}_1 = AB + AC + BC$



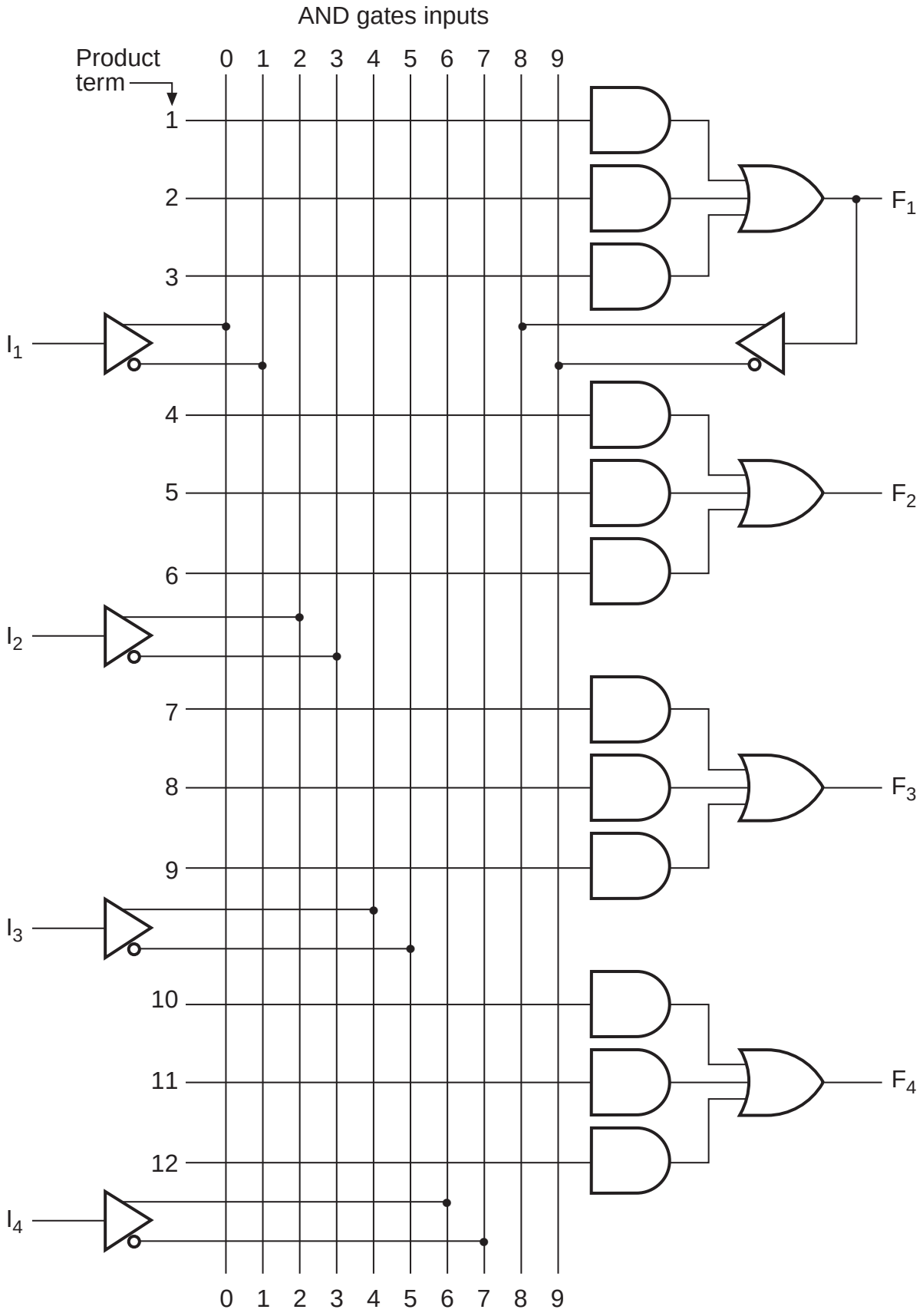
$F_2 = AB + AC + \overline{A}\,\overline{B}\,\overline{C}$

$\overline{F}_2 = \overline{A}C + \overline{A}B + A\overline{B}\,\overline{C}$

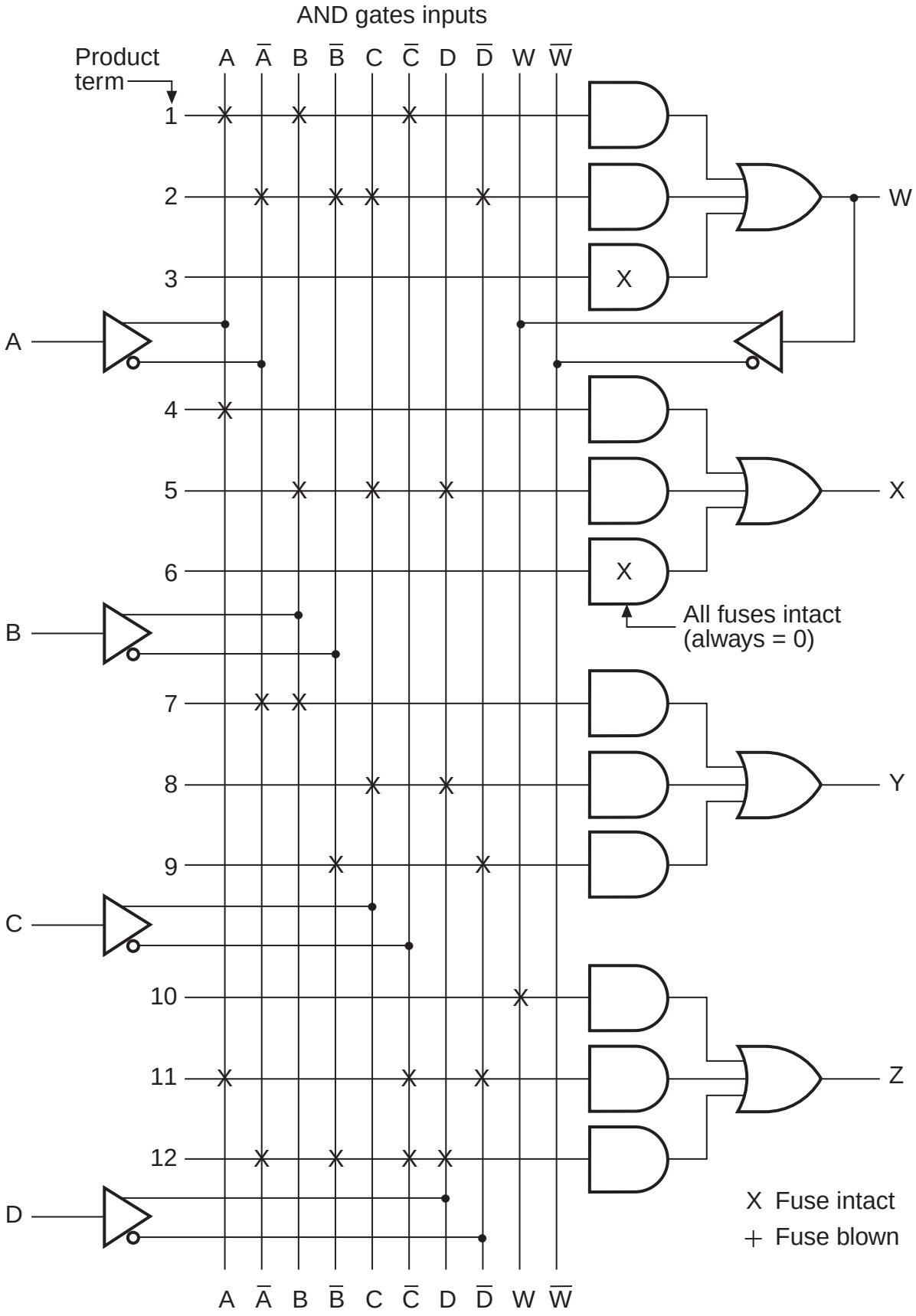
PLA programming table

	Product term	Inputs A B C	Outputs (C) F_1	Outputs (T) F_2
AB	1	1 1 –	1	1
AC	2	1 – 1	1	1
BC	3	– 1 1	1	–
$\overline{A}\,\overline{B}\,\overline{C}$	4	0 0 0	–	1

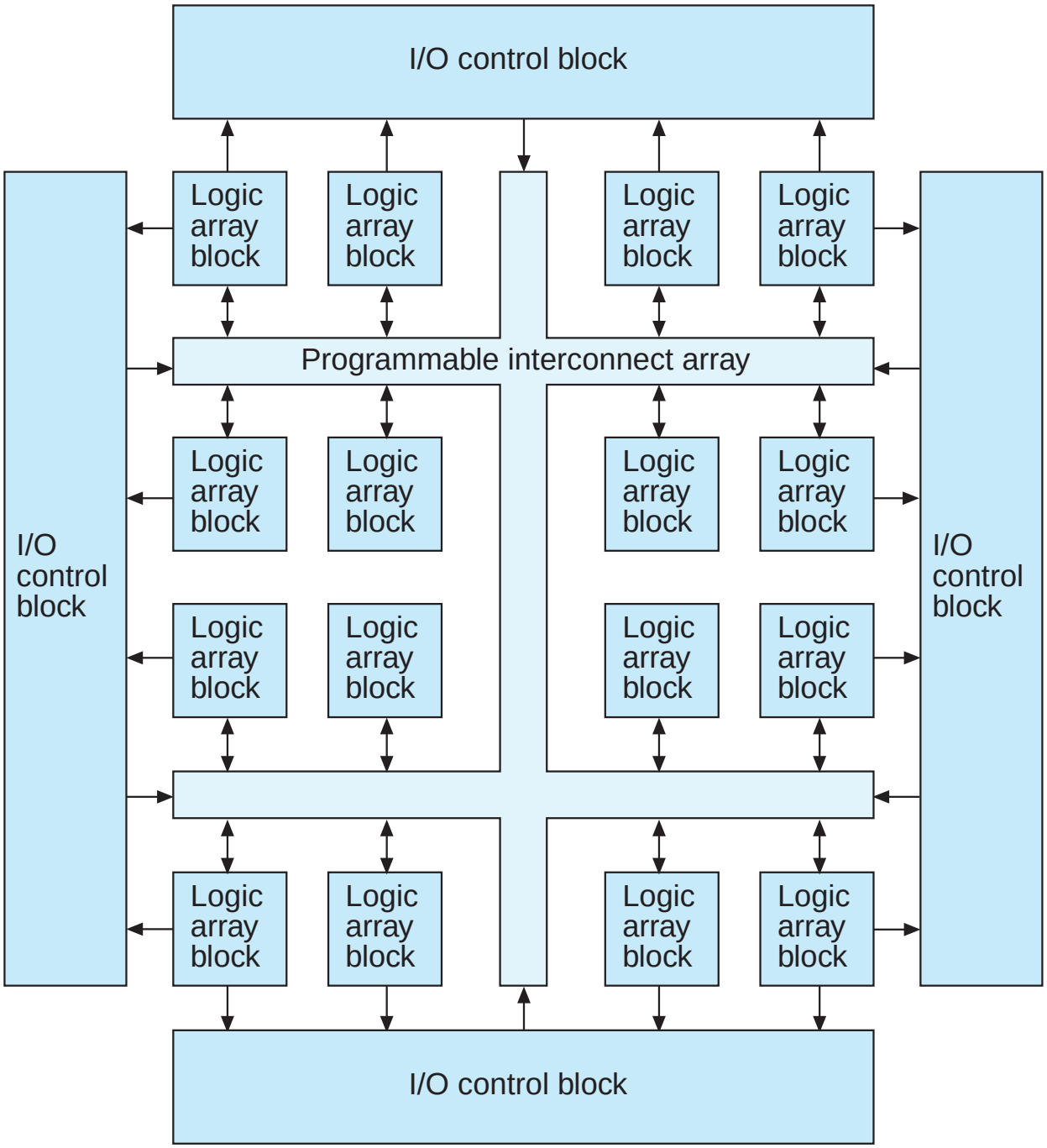
PAL® device with Four Inputs, Four Outputs, and a Three-wide AND-OR Structure



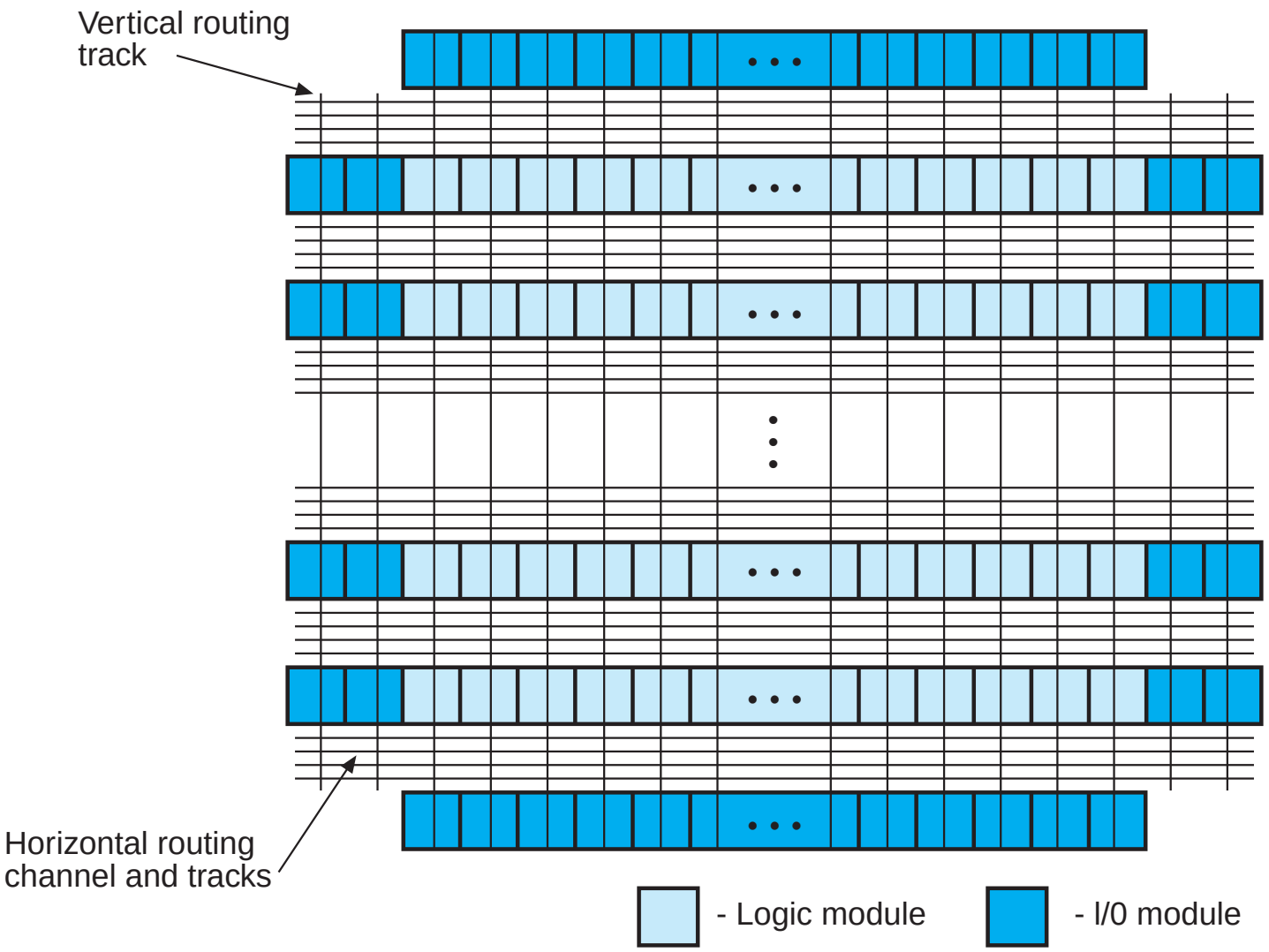
T-149 Connection Map for PAL® Device as Specified in Table 6-5



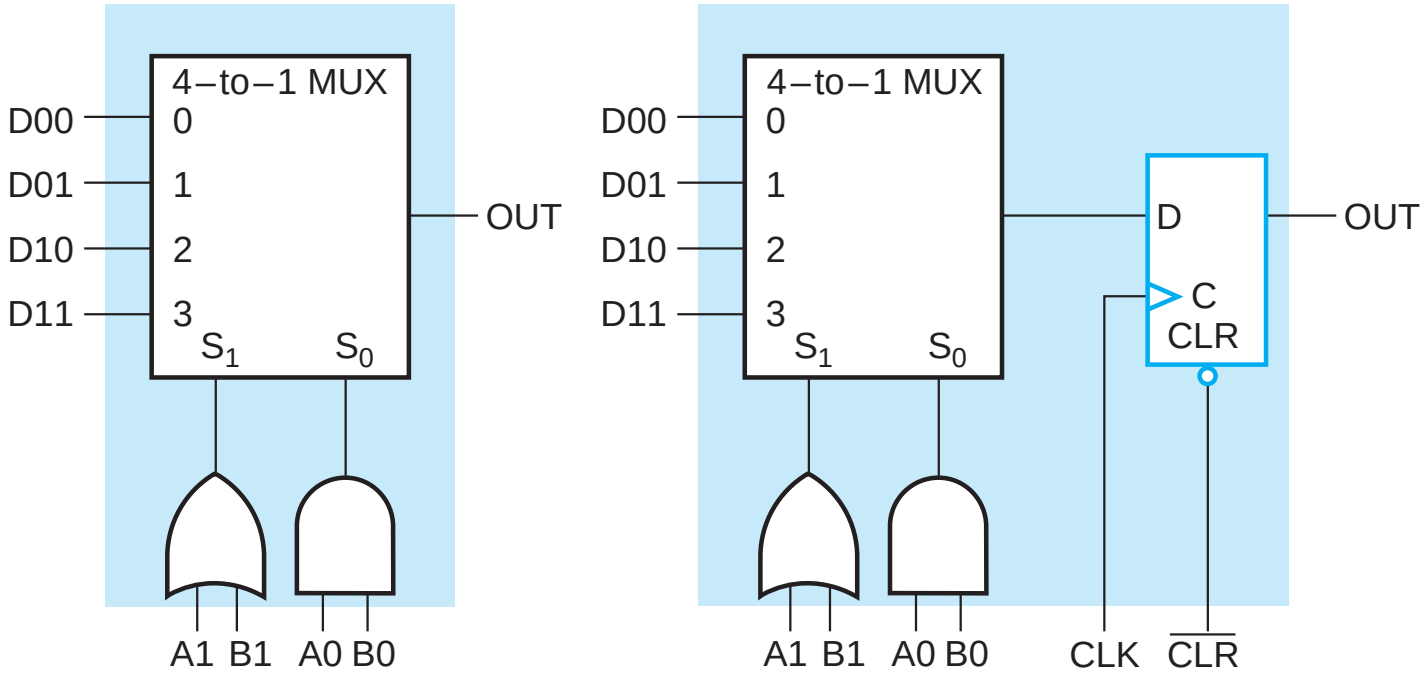
Altera® MAX 7000™ Structure (Reprinted with Permission of Altera Corporation,© Altera Corp., 1991)



T-151 **Actel® ACT 3 ® Structure (Reprinted Courtesy of Actel Corporation, © Actel Corp., 1993)**



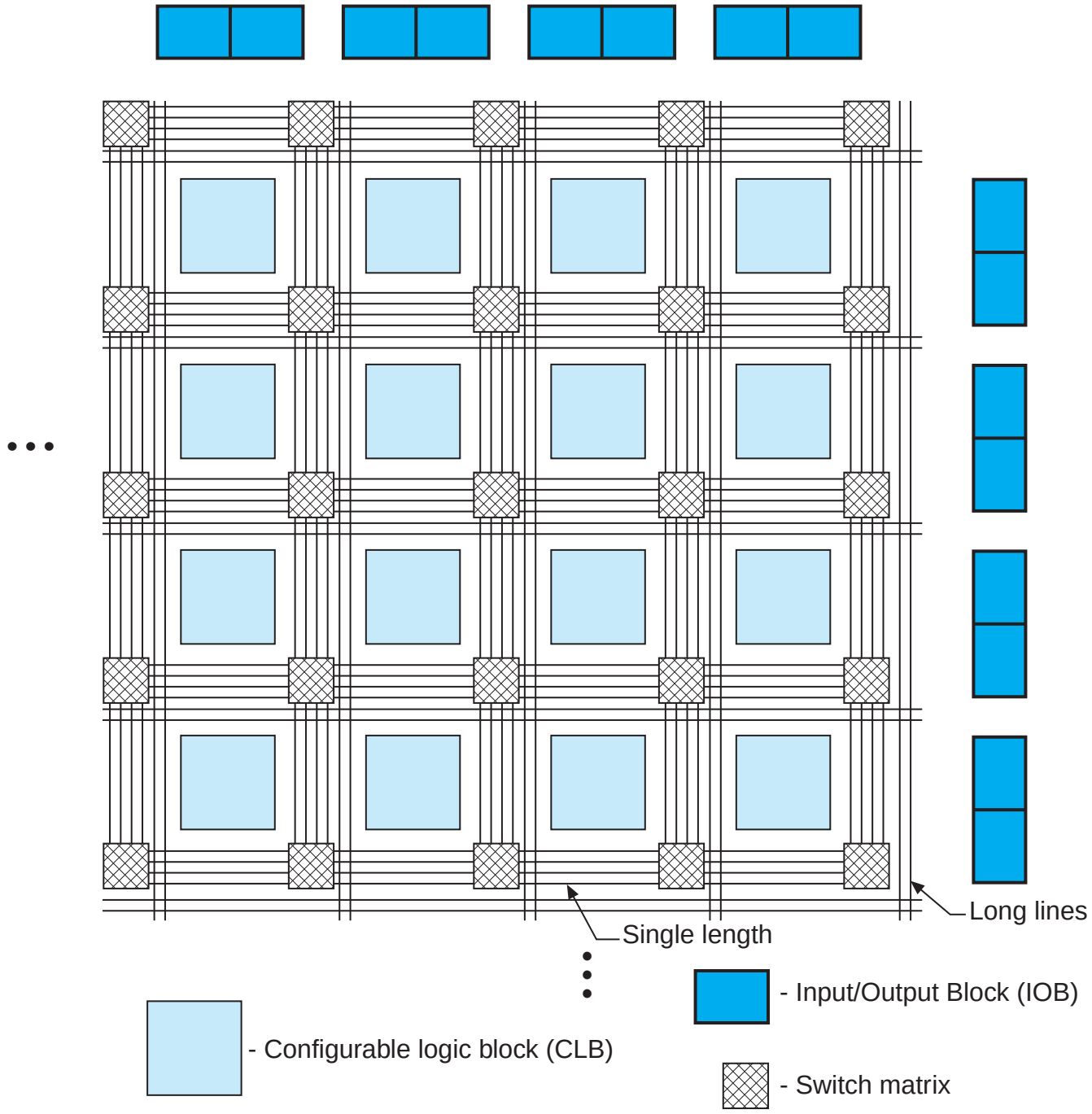
Actel® Logic Modules (Reprinted Courtesy of Actel Corporation, © Actel Corp., 1993)



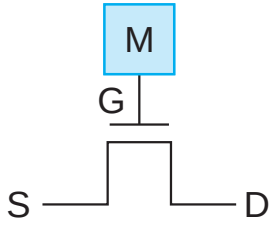
(a) C (combinational) module

(b) S (sequential) module

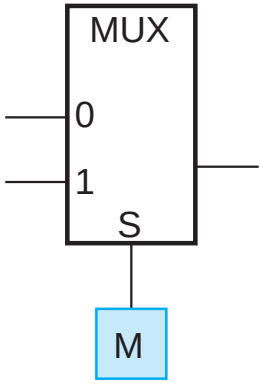
Xilinx® XC4000™ FPGA Structure (Adapted with Permission of Xilinx, Inc.)



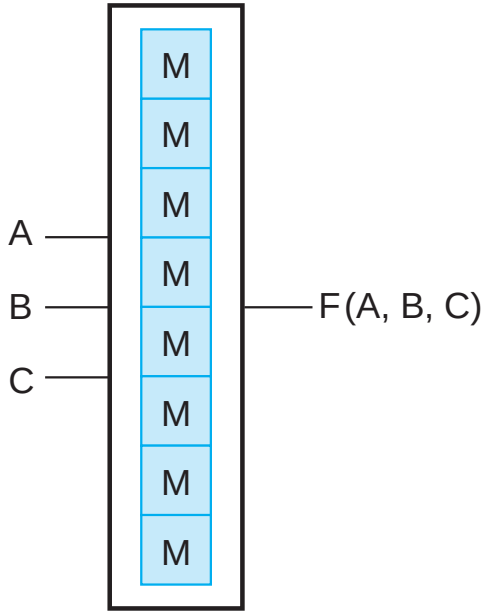
SRAM Bit Use in Xilinx® FPGAs



(a) Pass transistor control

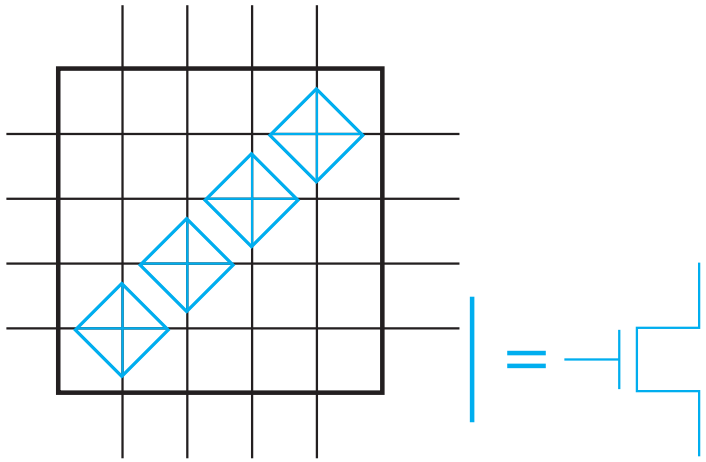


(b) Multiplexer control

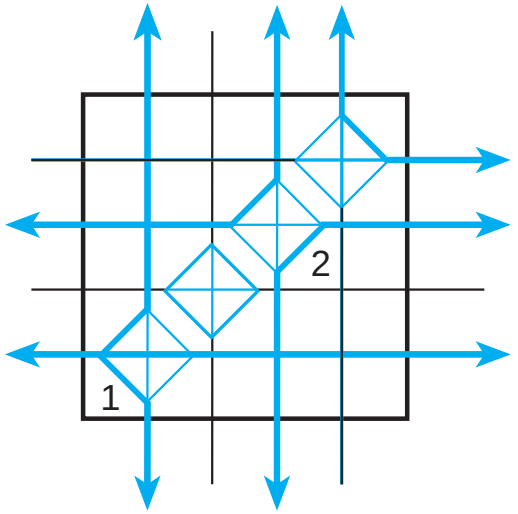


(c) Look up table implementation

Example of Xilinx® Switch Matrix (Adapted with Permission of Xilinx®, Inc.)

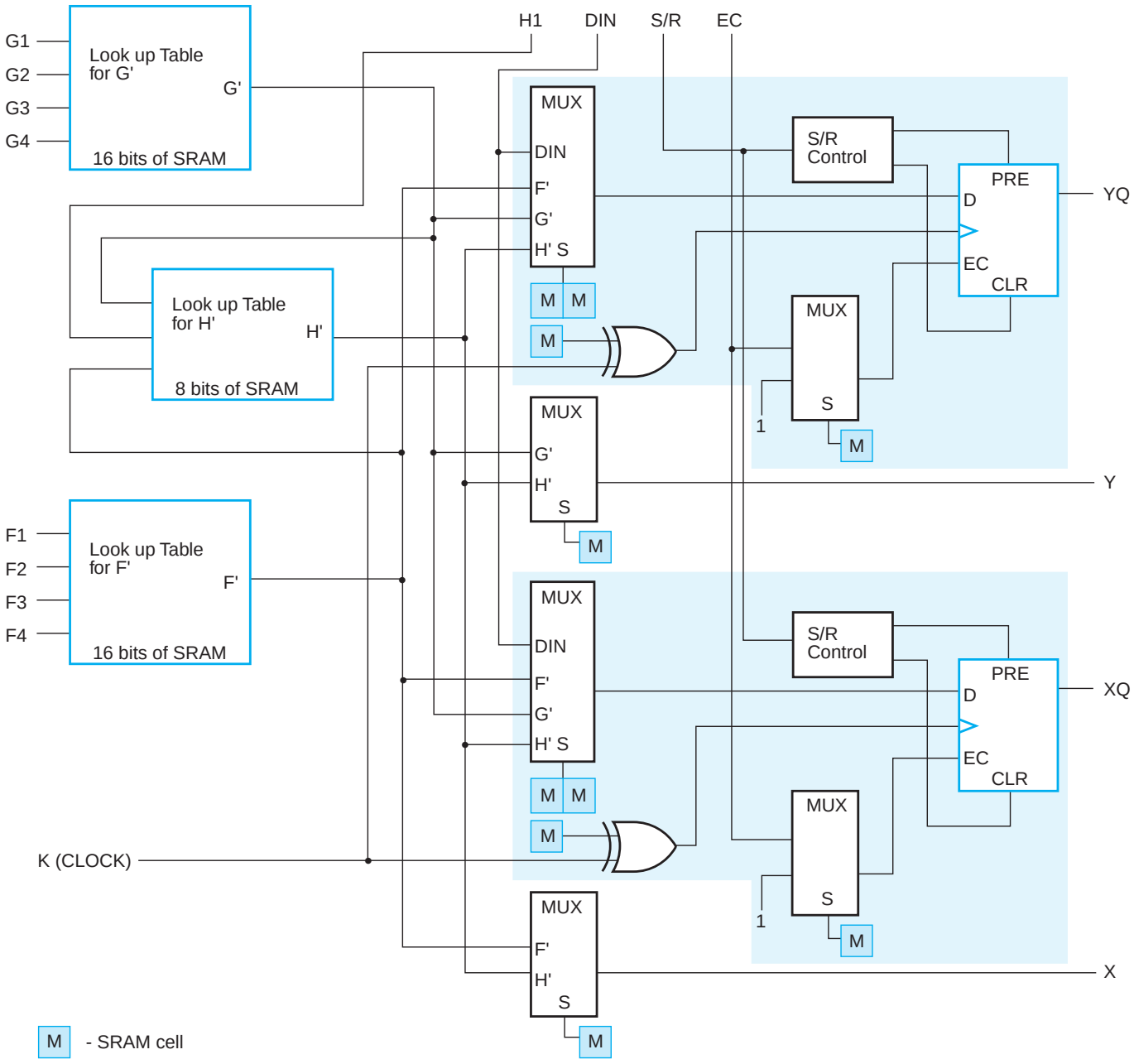


(a) Switch Matrix Transistors



(b) Examples of Connections

Simplified Diagram of a Xilinx® Configurable Logic Block (Adapted with permission of Xilinx®, Inc.)



Sketch of Xilinx® IOB Structure (Adapted with Permission of Xilinx®, Inc.)