



March 1998-3

#### FEATURES

- 8-Bit Resolution
- Sampling Rate to 30 MHz
- Low Power: 110 mW typ. (excluding reference)
- Power Down Mode: 100 $\mu$ A (typ)
- DNL =  $\pm 1/4$  LSB, INL =  $\pm 1/2$  LSB (typ)
- Internal S/H Function
- Single Supply: 5 V
- $V_{IN}$  Range: 0 V to  $V_{DD}$
- $V_{REF}$  Range: 1 V to  $V_{DD}$
- Latch-Up Free
- ESD Protection: 2000 V Minimum
- 3 State Digital Outputs

- Monotonic. No Missing Codes
- 20 Pin Package Available: MP8776
- 3 V Version: MP87L86
- Improved Version of MP8785

#### APPLICATIONS

- Wireless Communications
- Digital Cellular Telephones
- Telecommunications
- CCDs and Scanners
- Video Boards
- Digital Color Copiers
- Battery Powered Devices

#### GENERAL DESCRIPTION

The MP8786 is an 8-bit Analog-to-Digital Converter designed for high speed digitizing applications requiring low power. The MP8786 offers exceptional performance, flexible input architecture, low power consumption, power down capability, latch-up tolerant operation and is manufactured using an advanced 5 volt CMOS process.

This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8786 includes an on-chip S/H function which allows the user to digitize analog input signals between GND and  $V_{DD}$ . Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP8786.

The designer can choose the internally generated reference voltages by connecting  $V_{RB}$  to  $V_{RBS}$  and  $V_{RT}$  to

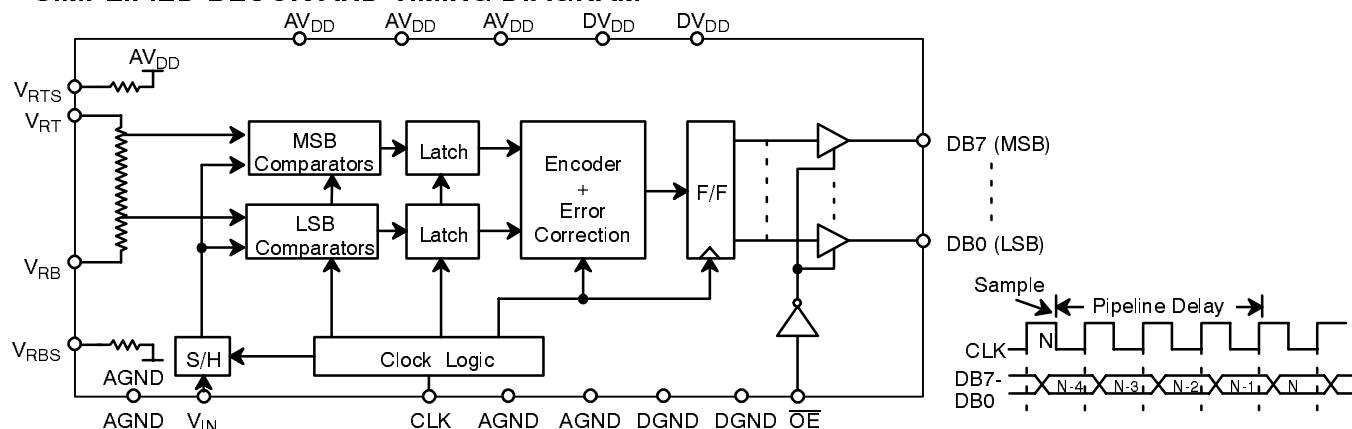
$V_{RTS}$ , or provide external reference voltages to the  $V_{RB}$  and  $V_{RT}$  pins. The internal reference generates 0.6 V at  $V_{RB}$  and 2.6 V at  $V_{RT}$ . Providing external reference voltages allows easy interface to any input signal range between GND and  $V_{DD}$ . This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

When board space is at a premium, designers may prefer to use the MP8776 which is available in a 20 pin package.

The device operates from a single +5 volt supply. Power consumption is 110 mW (typ) at  $F_s = 20$  MHz. Power down is accomplished by dropping  $V_{RT}$  below 0.55 V.

Specified for operation over the commercial / industrial ( $-40$  to  $+85^\circ\text{C}$ ) temperature range, the MP8786 is available in surface mount (SOIC) in Jedec and EIAJ, shrink small outline (SSOP) and plastic dual-in-line (PDIP) packages.

#### SIMPLIFIED BLOCK AND TIMING DIAGRAM

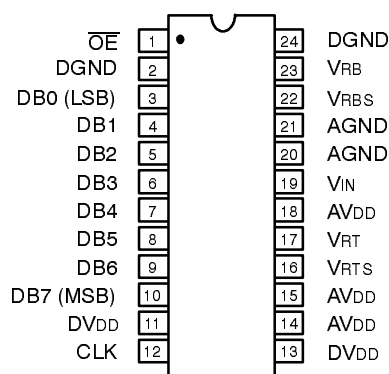


## ORDERING INFORMATION

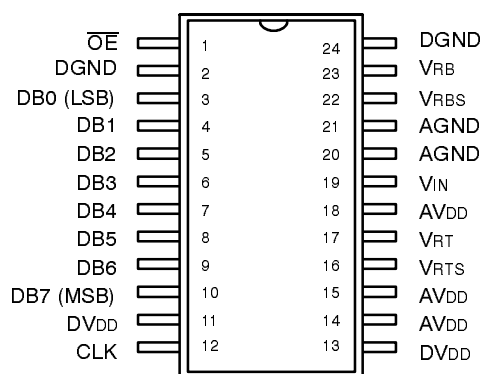
Package Type	Temperature Range	Part No.
SOIC (EIAJ)	-40 to +85°C	MP8786AR
SOIC (Jedec)	-40 to +85°C	MP8786AS
Plastic Dip	-40 to +85°C	MP8786AN
SSOP	-40 to +85°C	MP8786AQ

## PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")



24 Pin SOIC (EIAJ, 0.300")  
24 Pin SOIC (Jedec, 0.300")  
24 Pin SSOP

## PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DGND	Ground (outputs)
3	DB0	Data Output Bit 0 (LSB)
4	DB1	Data Output Bit 1
5	DB2	Data Output Bit 2
6	DB3	Data Output Bit 3
7	DB4	Data Output Bit 4
8	DB5	Data Output Bit 5
9	DB6	Data Output Bit 6
10	DB7	Data Output Bit 7 (MSB)
11	DVDD	Power Supply (outputs)
12	CLK	Sampling Clock Input

PIN NO.	NAME	DESCRIPTION
13	DVDD	Digital Power Supply
14	AVDD	Power Supply
15	AVDD	Power Supply
16	VRTS	Generates 2.6 V if tied to $V_{RT}$
17	VRT	Top Reference
18	AVDD	Power Supply
19	VIN	Analog Input
20	AGND	Ground
21	AGND	Ground
22	VRBS	Generates 0.6 V if tied to $V_{RB}$
23	VRB	Bottom Reference
24	DGND	Ground

## ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified:  $AV_{DD} = DV_{DD} = 5\text{ V}$ ,  $FS = 20\text{ MHz}$  (50% Duty Cycle),  
 $V_{RT} = 2.6\text{ V}$ ,  $V_{RB} = 0.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$

Parameter	Symbol	25°C			Units	Test Conditions/Comments
		Min	Typ	Max		
<b>KEY FEATURES</b>						
Resolution		8			Bits	
Maximum Sampling Rate	FS	20	30		MHz	
<b>ACCURACY<sup>1</sup></b>						
Differential Non-Linearity	DNL		$\pm 1/4$	$\pm 1/2$	LSB	Best Fit Line (Max INL - Min INL)/2
Integral Non-Linearity	INL		$\pm 1/2$	1	LSB	
Zero Scale Error	EZS		$\pm 3$		LSB	
Full Scale Error	EFS		$\pm 3$		LSB	
<b>REFERENCE VOLTAGES</b>						
Positive Ref. Voltage	$V_{RT}$		2.6	$AV_{DD}$	V	$V_{REF} = V_{RT} - V_{RB}$
Negative Ref. Voltage	$V_{RB}$	AGND	0.6		V	
Differential Ref. Voltage <sup>3</sup>	$V_{REF}$	1.0		$AV_{DD}$	V	
Ladder Resistance	$R_L$	245	350	455	$\Omega$	Short $V_{RB}$ to $V_{RBS}$ and $V_{RT}$ to $V_{RTS}$ Short $V_{RB}$ to $V_{RBS}$ and $V_{RT}$ to $V_{RTS}$ $V_{RB} = AGND$ , Short $V_{RT}$ and $V_{RTS}$
Ladder Temp. Coefficient	$R_{TCO}$		2000		ppm/°C	
Self Bias 1	$V_{RB}$		0.6		V	
	$V_{REF}$		2		V	
Self Bias 2	$V_{RT}$		2.3		V	
<b>ANALOG INPUT<sup>2</sup></b>						
Bandwidth (-1 dB) <sup>4</sup>	BW		14		MHz	Clock High Clock Low
Input Voltage Range	$V_{IN}$	0		$AV_{DD}$	V	
Input Capacitance Sample <sup>5</sup>	$C_{IN}$		22		pF	
Input Capacitance Convert <sup>5</sup>	$C_{IN}$		7		pF	
Aperture Delay	$t_{AP}$		10		ns	
Aperture Jitter	$t_{AJ}$		30		ps	
<b>DYNAMIC PERFORMANCE<sup>2</sup></b>						
Signal to Noise Ratio	SNR		46		dB	$F_{IN} = 1\text{ MHz}$
Signal to Noise plus Distortion	SINAD		42		dB	
Harmonic Distortion	THD		-46		dB	
Effective No. of Bits	ENOB		6.8		Bits	
<b>DIGITAL INPUTS</b>						
Logical "1" Voltage	$V_{IH}$	3.5			V	$V_{IN} = DGND$ to $DV_{DD}$
Logical "0" Voltage	$V_{IL}$			1.5	V	
DC Leakage Currents <sup>6</sup>	$I_{IN}$				$\mu\text{A}$	
CLK			5		$\mu\text{A}$	
OE			5		$\mu\text{A}$	
Input Capacitance			5		pF	
Clock Timing (See Figure 6.) <sup>7</sup>						For Specified Performance For Specified Performance For Specified Performance
Clock Period	1/FS	50			ns	
High Pulse Width	$t_{PWH}$	25			ns	
Low Pulse Width	$t_{PWL}$	25			ns	

## ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
<b>DIGITAL OUTPUTS</b>								
Logical "1" Voltage	$V_{OH}$	4.5					V	$C_{OUT}=15\text{ pF}$ $I_{LOAD} = 4\text{ mA}$
Logical "0" Voltage	$V_{OL}$			0.4			V	$I_{LOAD} = 4\text{ mA}$
3-state Leakage	$I_{OZ}$		10				$\mu\text{A}$	$V_{OUT}=GND\text{ to }DV_{DD}$
Data Valid Delay <sup>2, 8</sup>	$t_{DL}$		20				ns	
Data Enable Delay <sup>2, 8</sup>	$t_{DEN}$		20	25			ns	
Data 3-state Delay <sup>2, 8</sup>	$t_{DHZ}$		12	15			ns	
Pipeline Delay				3.5			clock cycles	Constant relationship between clock and output
<b>POWER SUPPLIES</b>								
Operating Voltage ( $AV_{DD}, DV_{DD}$ ) <sup>9</sup>	$V_{DD}$		5				V	
Current ( $AV_{DD} + DV_{DD}$ )	$I_{DD}$		22	35			mA	Does not include ref. current
<b>POWER DOWN</b>								
Power Down Point	$V_{RTPD}$	0.4	0.55				V	Chip goes to power down mode when $V_{RT} < 0.55\text{ V}$
Power Up Point				0.9			V	
Power Down Current	$I_{DDPD}$			100			$\mu\text{A}$	Does not include ref. current
Power Control Delay	PDD			200			ns	$V_{RT} @ 0.4 \rightarrow 0.9\text{ V}$

**Notes:**

- 1 Tester measures code transitions by dithering the voltage of the analog input ( $V_{IN}$ ). The difference between the measured and the ideal code width ( $V_{REF}/256$ ) is the DNL error (Figure 11.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 12.) Accuracy is a function of the sampling rate (FS).
- 2 Guaranteed. Not tested.
- 3 Specified values guarantee functionality. Refer to other parameters for accuracy.
- 4 The bandwidth represents the gain of the ADC and does not imply accuracy.
- 5 See  $V_{IN}$  input equivalent circuit (Figure 2.). Switched capacitor analog input requires driver with low output resistance.
- 6 All inputs have diodes to  $V_{DD}$  and GND. Input DC currents will not exceed specified limits for any input voltage between GND and  $V_{DD}$ .
- 7  $t_P, t_F$  should be limited to  $>5\text{ ns}$  for best results.
- 8 Depends on the RC load connected to the output pin.
- 9 AGND and DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted) 1, 2, 3

$V_{DD}$ to GND	7 V	Lead Temperature (Soldering 10 seconds)	300°C
$V_{RT}$ & $V_{RB}$	$V_{DD} + 0.5$ to GND - 0.5 V	Maximum Junction Temperature	150°C
$V_{IN}$	$V_{DD} + 0.5$ to GND - 0.5 V	Package Power Dissipation Rating @ 75°C	
All Inputs	$V_{DD} + 0.5$ to GND - 0.5 V	SOIC, PDIP, SSOP	750 mW
All Outputs	$V_{DD} + 0.5$ to GND - 0.5 V	Derates above 75°C	10 mW/°C
Storage Temperature	-65 to +150°C		

**Notes:**

- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100 $\mu\text{s}$ .
- 3  $V_{DD}$  refers to  $AV_{DD}$  and  $DV_{DD}$ . GND refers to AGND and DGND.

**THEORY OF OPERATION**

**Analog to Digital Conversion**

The MP8786 uses a two step, subranging architecture to convert analog voltages into 256 digital codes.

A full conversion (sampling  $V_{IN}$ , converting MSB & LSB, and performing any error correction) requires four clock cycles to complete (see Figure 6.) The pipelined architecture allows the chip to maintain a one conversion per cycle sample rate. Digital logic combines the MSB and LSB data and performs error correction to produce 8-bit output codes.

**Internal Reference Bias**

The MP8786 includes two on-chip resistors that can be used to bias the reference ladder without external circuitry. These two resistors are designed to track the reference ladder and are used to create a voltage divider between the supplies ( $AV_{DD}$  and AGND).

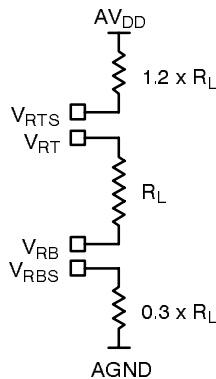
To use this feature simply connect  $V_{RT}$  to  $V_{RTS}$  and connect  $V_{RB}$  to  $V_{RBS}$ . This will nominally generate:

$$AV_{DD} \times (0.3/2.5) \text{ at } V_{RB}, \text{ and}$$

$$AV_{DD} \times (1.3/2.5) \text{ at } V_{RT}$$

This will generate 0.6 V at  $V_{RB}$  and 2.6 V at  $V_{RT}$  (Figure 1.) Bypass capacitors on  $V_{RT}$  and  $V_{RB}$  are suggested to stabilize the ladder.

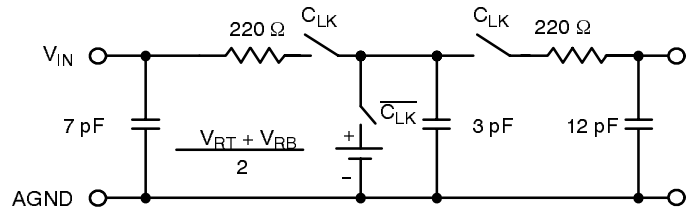
If the internal reference pins  $V_{RTS}$  and/or  $V_{RBS}$  are not used they should be left unconnected.



**Figure 1. Internal Reference Bias**

**Transfer Characteristics**

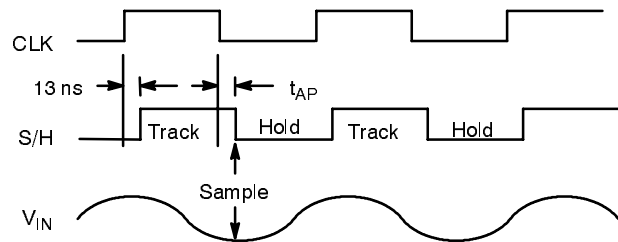
The ideal ADC is a linear building block that has infinite bandwidth and no phase distortion. A real ADC, however, exhibits finite bandwidth and non-constant group delay characteristics as well as non-linear behavior due to the non-zero INL characteristic. When modeling the ADC as a linear element and a quantizer, the circuit shown in Figure 2. can be used in order to represent the ADC's bandwidth.



**Figure 2. Input Equivalent Circuit**

**Sample and Hold Timing**

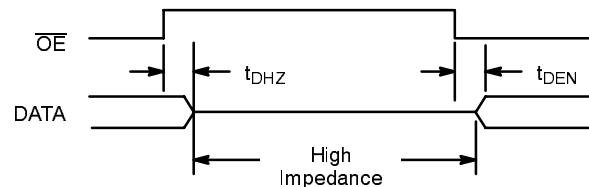
The ADC's internal sample and hold tracks the input signal when CLK is high. After a delay of  $t_{AP}$  from the falling clock edge, the analog signal is sampled and held for conversion as seen in Figure 3.



**Figure 3. Sample and Hold Timing**

**Output Enable ( $\overline{OE}$ )**

The  $\overline{OE}$  pin controls the state of the digital output drivers. When forced low, the drivers are active. When pulled high the drivers are 3-stated. Please note that the  $\overline{OE}$  pin only controls the output drivers, the rest of the chip is still active. Therefore if the clock is running, the internal registers are updated even if the digital outputs are 3-stated (Figure 4.).



**Figure 4. Output Enable/Disable Timing Diagram**

**Power Down Mode**

For systems that are battery powered, the MP8786 has a power down feature to help extend battery life. When the voltage at the  $V_{RT}$  pin drops below 0.4 V, the chip goes into power down mode. In this state, conversions are halted, the outputs are 3-stated and  $I_{DD}$  drops to less than 100  $\mu A$ . Then, when the voltage at the  $V_{RT}$  pin rises above 0.9 V, the chip will power up. Note that after power up, four clock cycles are required to get valid data at the digital outputs (see Figure 6.) One way to achieve power down is to disconnect or disable the buffer/amp driving  $V_{RT}$ , and let the internal reference resistance pull  $V_{RT}$  down. Remember, any bypass capacitors at  $V_{RT}$  will increase the time for  $V_{RT}$  to drop below 0.4 V.

## APPLICATION NOTES

### Power Supplies and Grounding

$AV_{DD}$  and  $DV_{DD}$  should be connected to the sample power supply source (Figure 5.). The power supply ( $AV_{DD}$  and  $DV_{DD}$ ) and reference voltage ( $V_{RT}$  &  $V_{RB}$ ) pins should be decoupled with  $0.1\mu\text{F}$  and  $10\mu\text{F}$  capacitors to GND, placed as close to the chip as possible.

AGND and DGND pins are connected internally through the P-substrate. AGND and DGND pins should be connected together as close to the chip as possible.

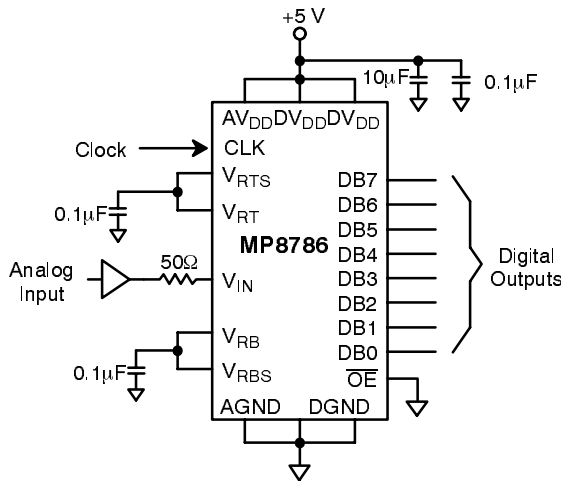


Figure 5. Typical Circuit Connections

### The Analog Input

When designing with the MP8786, the following points can help optimize performance.

1. Driving the analog input – The input impedance can be represented as a switched capacitor type input circuit, i.e. the input impedance changes with the phase of the input clock. Figure 2. shows an equivalent input circuit. In many applications, the input impedance can be treated as capacitive. For fast signals and a high driving impedance, a wide bandwidth op amp is recommended.
2. It is important to note that op amps have inductive output impedances at high frequencies which is a consequence of the emitter impedance of the typical push-pull output stage. The resulting transient ringing should be damped by inserting a resistor in series with the ADC input – typically about  $50\Omega$ . See Figure 6. The exact value may be obtained from the op amp manufacturer's data sheet.
3. Signals should not exceed  $V_{DD} + 0.5\text{V}$  or go below GND  $-0.5\text{V}$ . All pins have internal protection diodes that will protect them from short transients (See Note 2, Absolute Maximum Ratings) outside the supply range.

### Digital Outputs

Refer to Figure 6. for details on the data availability timing. The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion. The output enable pin ( $\overline{\text{OE}}$ ) should not be left unconnected. If it is not controlled by an active signal, it must be tied to ground.

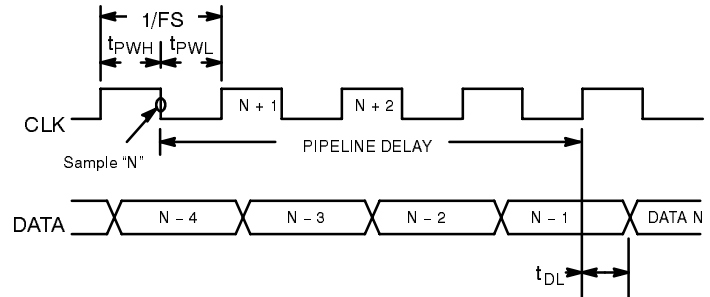


Figure 6. Data Available Timing

### Dynamic Reference Control

The MP8786 allows for dynamically adjusted  $V_{RT}$  and  $V_{RB}$ . When this is done,  $V_{RT}$  and  $V_{RB}$  have to be kept static during a certain period.

The A/D conversion is done in a two-step method. During the first clock period, the MSB comparator bank compares the  $V_{IN}$  with the reference voltage string in order to determine in which subrange the exact  $V_{IN}$  lies. During the subsequent clock period, an LSB comparator bank compares a subrange of the  $V_{REF}$  to the  $V_{IN}$ . Thus, the reference inputs have to be stable during two compare cycles. This implies that while the ADC is clocked with FS, the conversion only occurs at a rate of FS/2. Every second sample and resulting data must be discarded because the reference changes during its conversion.

The reference inputs  $V_{RT}$  and  $V_{RB}$  have to have settled to within 1 LSB, at least 50 ns before the rising edge which occurs after the sampling instant. The reference has to be kept constant until  $(t_{AP} + 10\text{ ns})$  after the second rising edge. See Figure 7. for timing details. The digital data of the  $N + 1$ ,  $N + 3$ ,  $N + 5$  etc. samples are invalid if the reference is changed every second clock cycle. The data for the  $N$ ,  $N + 2$ ,  $N + 4$  etc. samples are valid.

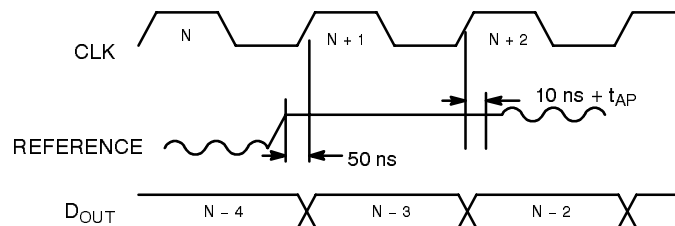
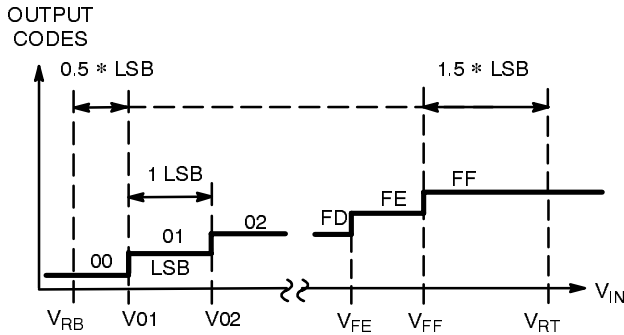


Figure 7. Dynamic Reference Control

**LINEARITY DEFINITION**

**The Ideal ADC**

The transfer function for an ideal A/D converter is shown in Figure 8.



**Figure 8. Ideal A/D Transfer Function**

The first transition for the data bits takes place when:

$$V_{IN} = V_{01} = V_{RB} + 0.5 * LSB$$

The last transition of the data bits takes place when:

$$V_{IN} = V_{FF} = V_{RT} - 1.5 * LSB$$

$$\text{where: } LSB = V_{REF} / 256 \\ = (V_{FF} - V_{01}) / 254$$

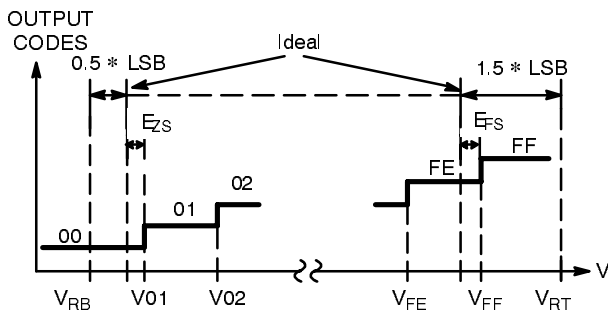
$$\text{and } V_{REF} = (V_{RT} - V_{RB})$$

**The Real ADC**

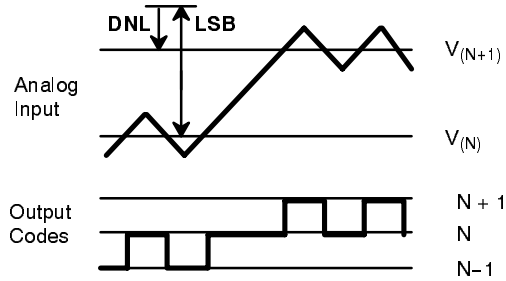
In a "real" converter, the code-to-code transitions do not fall exactly every  $V_{REF}/256$  volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A specification of Max DNL =  $\pm 0.5$  LSB means that all codes are within 0.5 LSB and 1.5 LSB. For example, if  $V_{REF} = 4.096$  V then 1 LSB = 16mV and every code width is between 8 and 24 mV.



**Figure 9. Real A/D Transfer Curve**



**Figure 10. DNL Measurement**

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) are:

$$DNL(01) = V_{02} - V_{01} - LSB$$

...

$$DNL(FE) = V_{FF} - V_{FE} - LSB$$

$$\text{Thus } DNL(N) = [V_{(N+1)} - V_{(N)}] - LSB$$

$$\text{Code Width (N)} = V_{(N+1)} - V_{(N)}$$

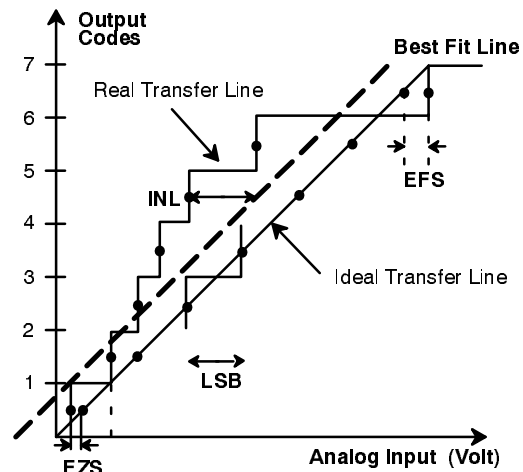
Similarly, the zero scale and full scale errors are defined as:

$$EFS \text{ (full scale error)} = V_{FF} - (V_{RT} - 1.5 * LSB)$$

$$E_ZS \text{ (zero scale error)} = V_{01} - (V_{RB} + 0.5 * LSB)$$

$$\text{where: } LSB = [V_{RT} - V_{RB}] / 256$$

Figure 10. shows the zero scale and full scale error terms while Figure 11. shows the definition of DNL.

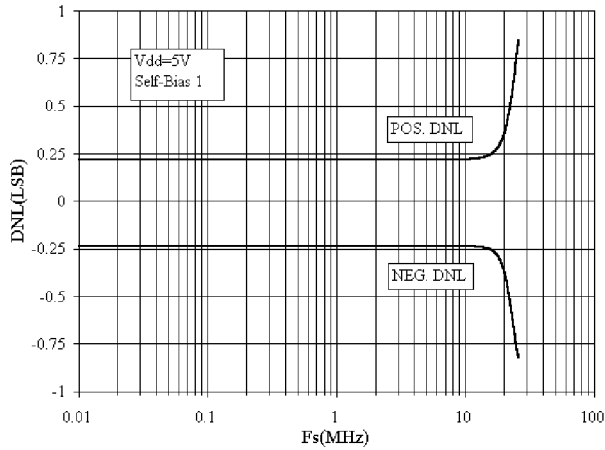


**Figure 11. INL Error Calculation (3-Bit)**

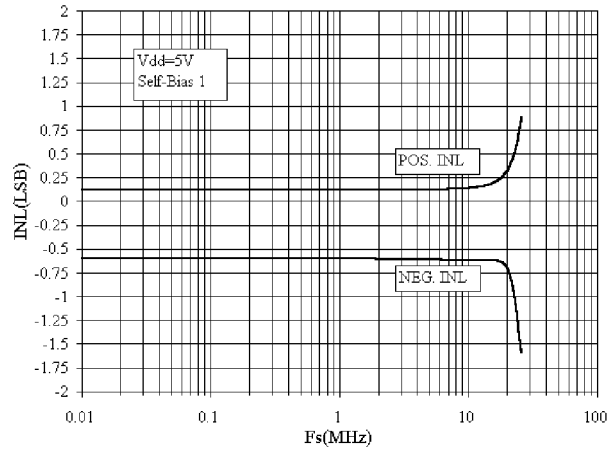
Figure 12. gives a visual definition of the INL error. The graph shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the best fit line makes equal the positive and the negative INL errors. This may change an INL of  $-1$  to  $+2$  LSBs relative to the ideal line into a  $\pm 1.5$  relative to the best fit line.

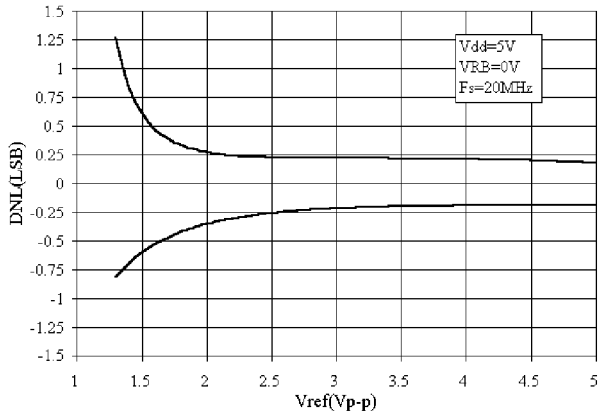
## PERFORMANCE CHARACTERISTICS



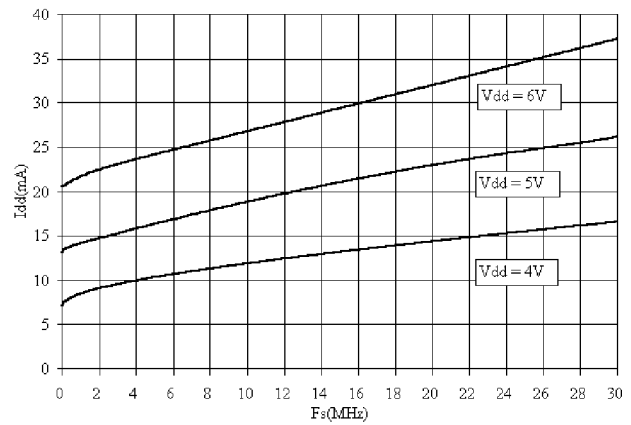
**Graph 1. DNL vs. Sampling Frequency**



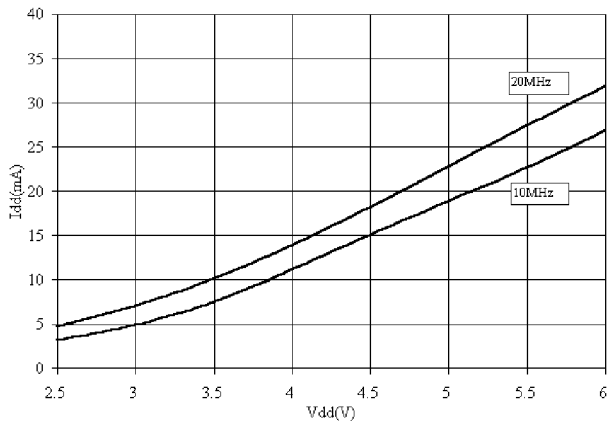
**Graph 2. INL vs. Sampling Frequency**



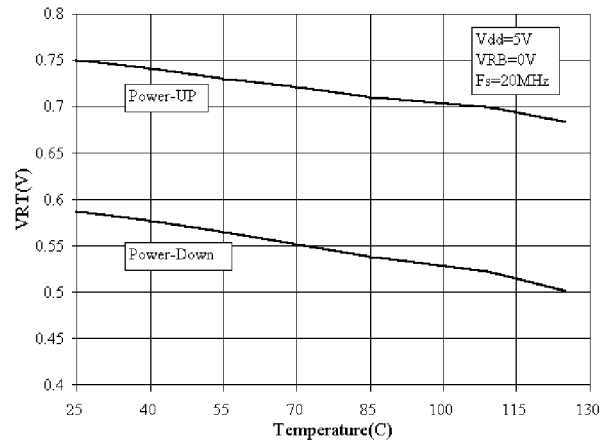
**Graph 3. DNL vs. Reference Voltage**



**Graph 4. Supply Current vs. Sampling Frequency**

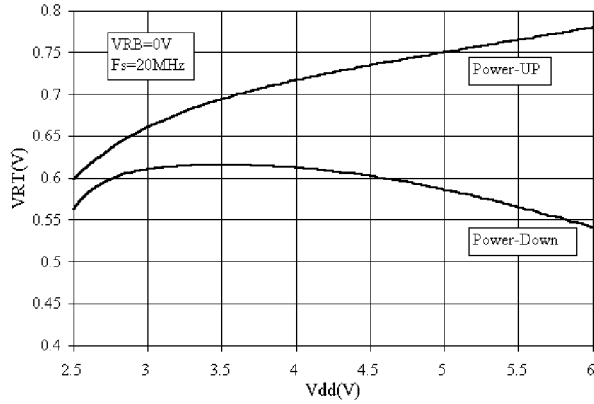


**Graph 5. Supply Current vs. Supply Voltage**

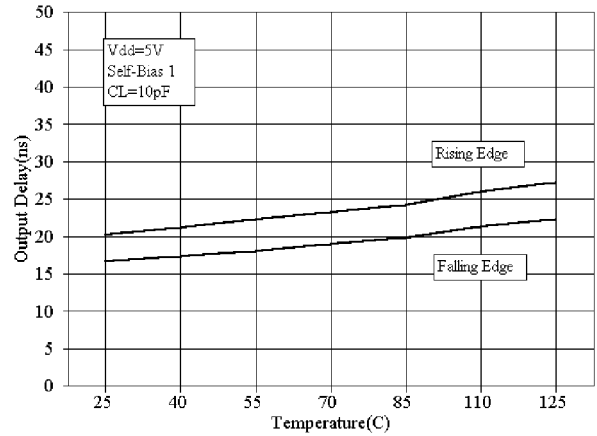


**Graph 6. Power Up/Down Voltage vs. Temperature**

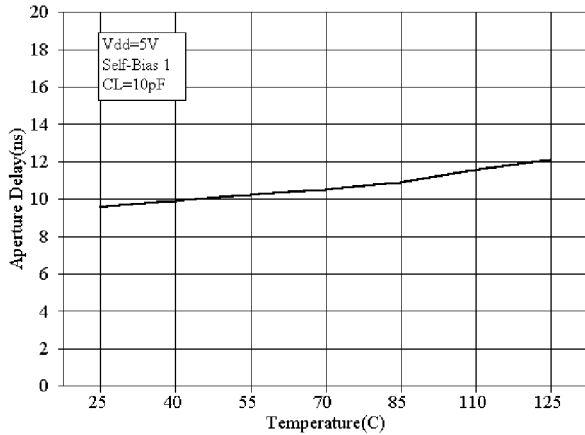




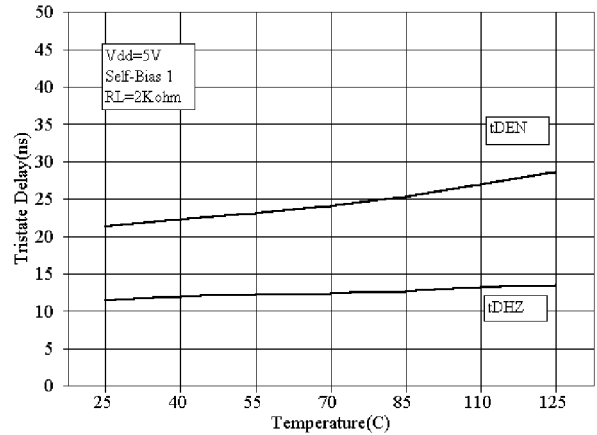
**Graph 7. Power Up/Down Voltage vs. Supply Voltage**



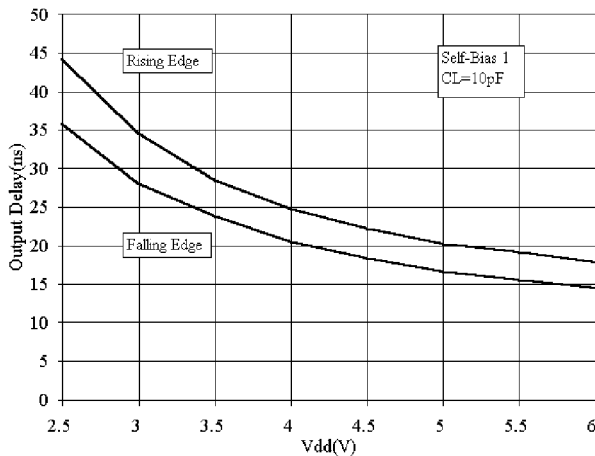
**Graph 8. Output Delay ( $t_{DL}$ ) vs. Temperature**



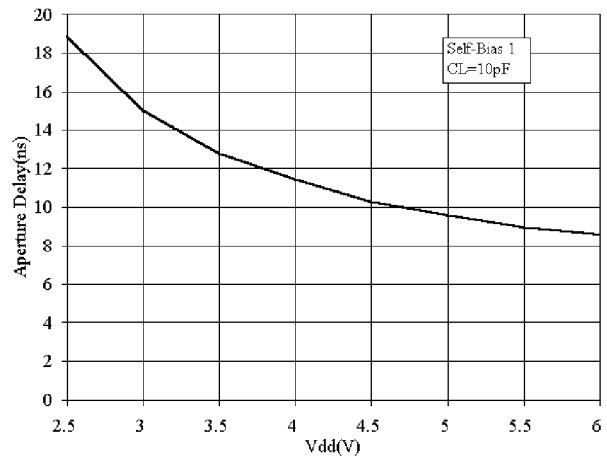
**Graph 9. Aperture Delay ( $t_{AP}$ ) vs. Temperature**



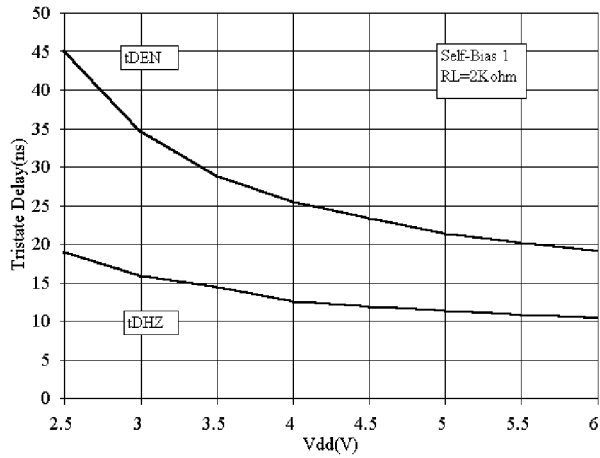
**Graph 10. 3-State/Enable Delay vs. Temperature**



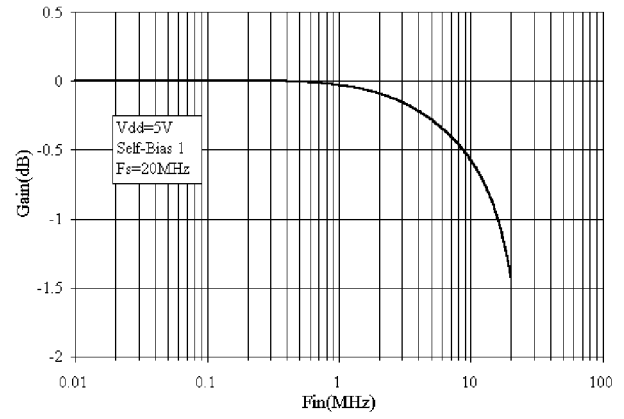
**Graph 11. Output Delay vs. Supply Voltage**



**Graph 12. Aperture Delay ( $t_{DL}$ ) vs. Supply Voltage**



**Graph 13. 3-State/Enable Delay vs. Supply Voltage**



**Graph 14. Gain vs. Input Frequency**