Amplifiers and Bits: An Introduction to Selecting Amplifiers for General-Purpose Data Converters

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ABSTRACT

This application report discusses various considerations that must be taken into account when interfacing general-purpose amplifiers and analog-to-digital converters. The report discusses bandwidth, resolution, analog ADC input drive, and power supply considerations for both parts.

Contents

List of Figures

1 Introduction

This application report discusses various considerations that must be taken into account when interfacing general-purpose amplifiers and analog-to-digital converters (ADC). As used here, *general-purpose* means voltage feedback (VFB) amplifiers of a bandwidth <10 MHz, and, typically, successive approximation ADCs between 8–12 bits with speeds <2 MSPS. Many of these same items can be applied to higher-speed or higher-resolution systems, but there are other design considerations specific to such systems that this report does not address.

This report discusses bandwidth, resolution, analog ADC input drive, and power supply considerations for both parts.

Figure 1 shows the amplifier – ADC interface.

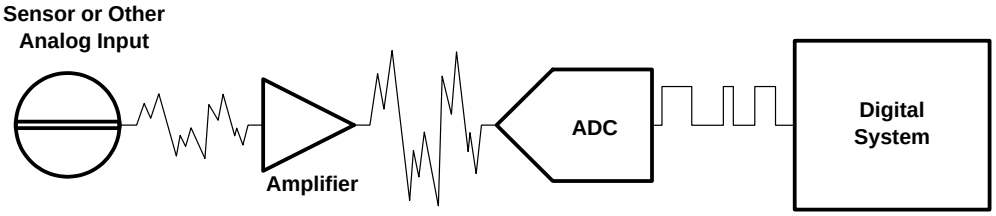


Figure 1. Amplifier and ADC

2 Bandwidth

Choosing an ADC that meets the system requirements for resolution and speed is the first priority. Other considerations such as power or interface will also come into play, but once the bandwidth of the ADC has been determined, an amplifier can be chosen to go with it. With regard to bandwidth, most applications using general-purpose ADCs will observe Nyquist and sample at greater than twice the highest frequency of interest to avoid aliasing.

With VFB amplifiers, gain bandwidth product (GBP) is the specification of interest when looking at small signal bandwidth. Because the VFB amplifier is dependent on the gain that is being employed, the frequency of the signal of interest multiplied by the gain must be less than the GBP for the amplifier.

$$\text{Frequency} \times \text{Gain} < \text{GBP} \tag{1}$$

It is good design practice to ensure the GBP of the amplifier has some amount of extra margin. This ensures that system variability does not press beyond the amplifier's capability.

When referring to GBP, use the graphs in the back of most amplifier datasheets, because GBP is often dependent on the supply voltage. As an example, Figure 2 shows that the TLV2460 has a delta of 40 kHz of GBP across the full Vcc range for the device.

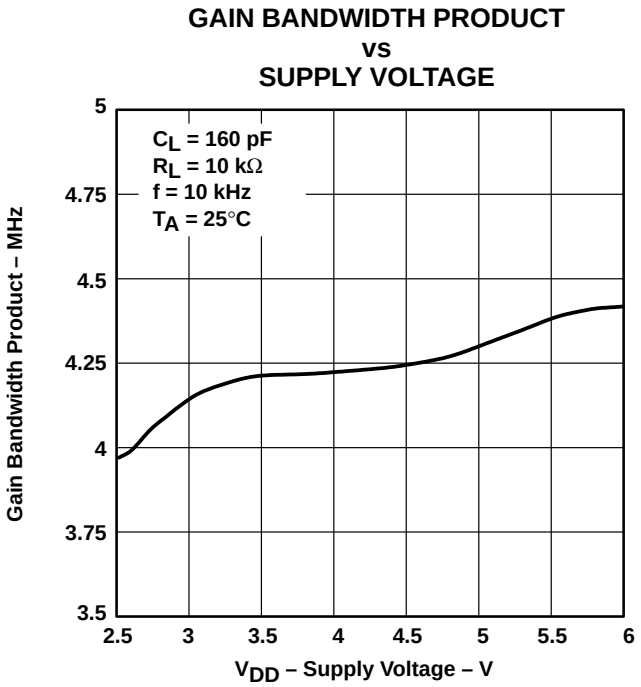


Figure 2. Typical Gain Bandwidth Product Graph (TLV2460)

The other specification that is of interest with respect to large signal bandwidth is slew rate. Denoted in volts per microsecond (V/μs), slew rate is the ability of the amplifier to react to step inputs and slew an output across the amplifier's dynamic range. To ensure an amplifier has sufficient slew rate for a given application, a rough calculation can be made.

For example, consider the TLV2460 again with a typical slew rate of 1.6 V/μs. The graph in the data sheet shows that using this part with a 3-V supply will result in roughly 1.6 V/μs or greater. Now, using a signal with frequency (f) equal to 2 MHz is well within the GBP of the amplifier at 3 V. Since f = 2 MHz, 1/f is then equal to 0.5 μs. The value of 1/f can be used to compare the amplifier's slew rate and what it can support in signal slew rate. Amplifier slew rate must be greater than or equal to the signal slew rate in this case:

$$\frac{1.6\ \text{V}}{1\ \mu\text{s}} > \frac{x}{0.5\ \mu\text{s}} \tag{2}$$

where solving shows that x is less than or equal to 0.8 V. Thus, the largest peak-to-peak voltage the TLV2460 can support at 2 MHz is 0.8 V. With respect to both GBP and slew rate, pushing the amplifier to its limit causes distortion. Ideally, an engineer wants 20% head room on both specifications to ensure correct operation.

3 Resolution and Amplifiers

Other product specifications are used to choose an amplifier that matches the resolution of the ADC. A familiar formula is:

$$\text{SNR dB} = 6.02 \times n - 1.76 \tag{3}$$

OR

$$n = \frac{(\text{SNR dB} + 1.76)}{6.02} \tag{4}$$

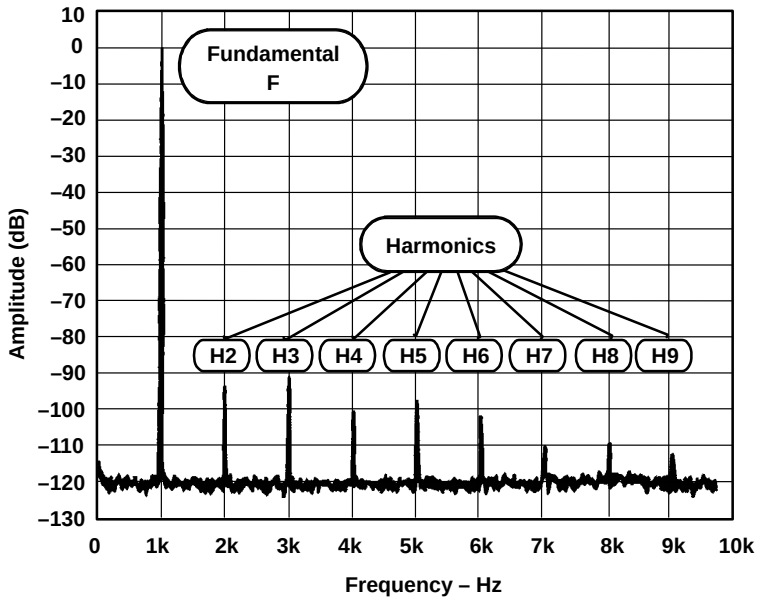
and is used to estimate the resolution needed in an application. In this equation, signal-to-noise ratio (SNR) is an ideal ratio in decibels, and n is an ideal number of bits. This equation offers a mathematical baseline, though *real* SNR must be used to match an amplifier with an ADC.

SINAD offers this real SNR, since it takes into account noise and distortion. SINAD is defined as:

$$\text{SINAD} = \text{SNR} + \text{D} = \frac{1}{\text{THD} + \text{N}} \tag{5}$$

NOTE: These numbers are scalar and not in dB.

SNR is the ratio of energy in the fundamental signal and the energy in noise. Total harmonic distortion (THD) is a similar ratio between the energy in the harmonics and the energy in the fundamental.



$$\text{SNR (dB)} = 20 \times \log \frac{E_F}{E_N}$$

$$\text{THD (dB)} = 20 \times \log \frac{\sqrt{E_{H2}{}^2 + \ldots + E_{H9}{}^2}}{E_F}$$

$$\text{THD+N (dB)} = 20 \times \log \frac{\sqrt{E_{H2}{}^2 + \ldots + E_{H9}{}^2 + E_N{}^2}}{E_F}$$

$$\text{SINAD} = \text{SNR} + \text{D} = \frac{1}{\text{THD} + \text{N}}$$

Figure 3. SNR and THD Pictorial

SINAD takes into account the harmonics and the noise energy, and thus produces a real SNR that can lead to the effective number of bits (ENOB) in ADCs and amplifiers. ENOB is defined as:

$$\text{ENOB} = \frac{[(\text{SINAD dB}) - 1.76]}{6.02} \tag{6}$$

Data converter specifications will offer either SNR + D or THD + N in dB; thus, this equation is easy to use. Conversely, amplifier specifications usually specify SNR + D or THD + N in percent instead of dB. This requires some mathematical manipulation to use the same equations.

Translating percent to dB is straightforward. For example, the following steps translate THD + N% to THD + N dB, but the same steps can be used to translate SNR + D or SINAD from percent to dB.

$$\frac{\text{THD} + \text{N}\%}{100} = \text{THD} + \text{N} \tag{7}$$

Then

$$20 \log (THD + N) = THD + N \text{ dB} \tag{8}$$

This can be put into one mathematical expression,

$$20 \log_{10} \left(\frac{THD + N\%}{100} \right) = THD + N \text{ dB} \tag{9}$$

but it is often useful to have the intermediate step of a scalar number, because equation (5) is also stated in scalar numbers. To use this equation in dB, remember:

$\log B^A = A \times \log B$ and thus, equation (5) in dB is :

$$SINAD \text{ dB} = SNR + D \text{ dB} = (THD + N \text{ dB})^{-1} = -(THD + N \text{ dB}) \tag{10}$$

The ability to convert between percent and dB simplifies matching the appropriate SINAD specifications between an amplifier and an ADC without. Ideally, choosing an amplifier and an ADC that have the same SINAD realizes the full potential of the signal chain. In practice, choosing an amplifier that has a slightly higher SINAD ensures that it does not degrade the system performance.

For example, the TLV1572 ADC has a typical SNR+D of 58 dB that equates to an ENOB of 9.35 bits. An amplifier like the TLV2770 is an excellent choice to drive this ADC. The TLV2770 has more than sufficient GBP (5.1 MHz typical) to place significant gain on the input signal. Also, the THD+N graphs in the back of the TLV2770 data sheet match the performance of the TLV1572 in nearly all cases, with the only exception being a relatively high supply voltage and high signal gain.

4 Analog-to-Digital Converter Analog Input

Figure 4 shows an example of driving the input of an ADC.

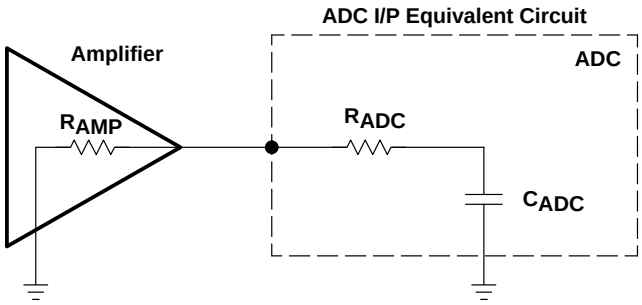


Figure 4. Amplifier–ADC Interface

Figure 5 shows the simplified equivalent RC circuit.

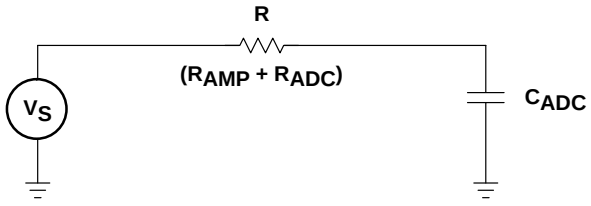


Figure 5. Amplifier–ADC Interface Equivalent Circuit

This assumes that R is the combination of the internal ADC equivalent resistance and the amplifier output resistance. If a significant external resistance were present in series between the two devices, such as PCB trace impedance, it would also need to be added. This gives a simple equivalent circuit model for the system. In this model, three items need to be accounted for with respect to the analog input of the ADC:

- The RC time constant created
- Having sufficient drive current
- Correctly biasing the input signal to the ADC

4.1 RC Time Constant

The following equation can be used to calculate the time constant for the circuit:

$$\tau = RC \tag{11}$$

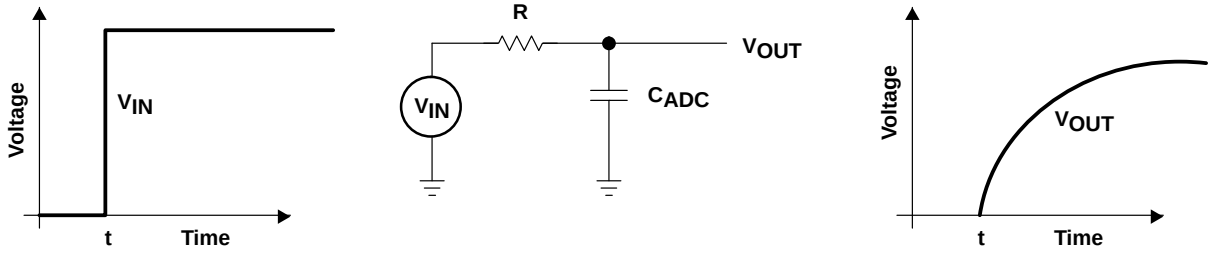


Figure 6. RC Pictorial

The optimal configuration is to have the amplifier drive directly into the ADC, as any additional external resistance will affect τ . If additional external resistance exceeding that specified in the ADC datasheet is necessary, it is extremely important to calculate τ and check it against the sample time of the ADC. This ensures the circuit has time to charge the input capacitor before the input signal is held by sample-and-hold circuitry, and the analog-to-digital conversion begins.

4.2 Drive Current

Drive current from the amplifier is another consideration in driving the analog input of an ADC. Without enough drive current, the same issue of not presenting the correct signal to the ADC occurs as mentioned previously with respect to τ**.** Looking again at the simplified circuit, there are many equations that govern what current is flowing at any given time.

Considering only the worst-case current demand ensures that the amplifier can help us get a rough idea of the appropriate amount of current needed. Using the simplified model circuit permits examining this circuit with a step function response between the two most extreme potentials.

For example, consider the case where the circuit is in steady state at the highest potential and immediately switches to the lowest.

This circuit is governed over time by the equation:

$$V(t) = V_o e^{\pm (t/RC)} \tag{12}$$

where V_0 is the steady state V on the capacitor. Assuming the input voltage at the voltage source (V_S) is steady from t = –∞ up until t= 0, it can be determined that $V_0 = V_S$. The simple explanation is that, in a dc steady state, the capacitor acts like an open circuit, thus having the same voltage as V_S.

To further simplify the analysis, assume that V_S switches from a known voltage to ground. Thus the circuit turns into a simple RC circuit.

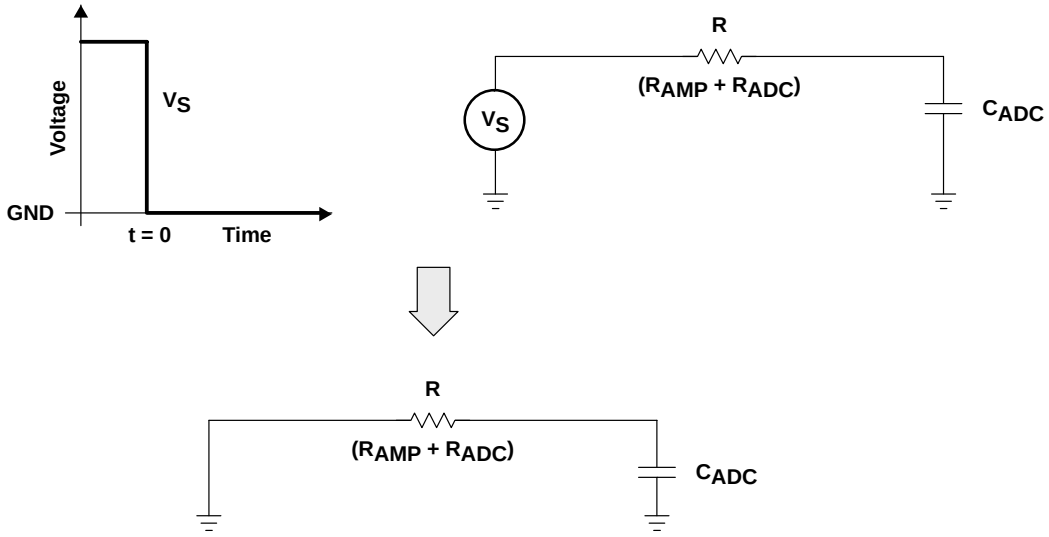


Figure 7. Circuit Simplification

It is intuitive that where t = 0, or right at the switch in potential, the current is the greatest while the voltage exponentially decays over time. The largest current the amplifier needs to handle can then be calculated roughly as:

$$I = \frac{V(t)}{R} \quad \text{Where } t = 0. \tag{13}$$

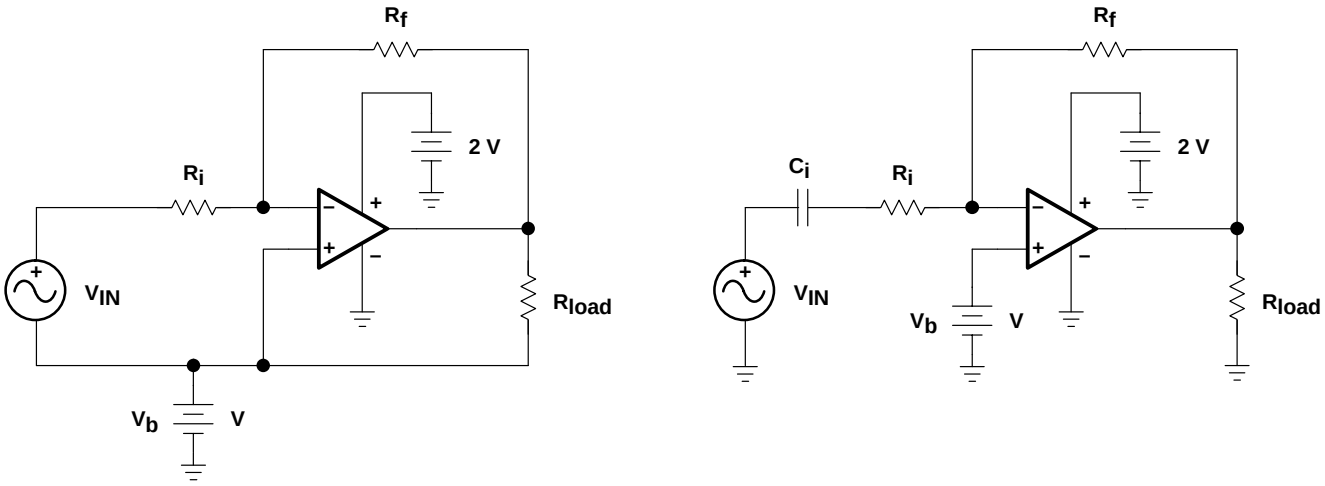
For example, using the TLV1544 ADC gives approximate values of R=1 kΩ and C=55 pF. The time constant τ can then be calculated as in the previous section, given the input resistance on a prospective amplifier. If the largest input voltage to the TLV1544 will be 3 V, the amplifier needs to source roughly 3 mA, again depending on the output resistance of the amplifier.

4.3 Signal Bias

Using the proper signal bias to the input waveform is another important consideration regarding the analog input of the ADC. Different ADCs have different analog input ranges.

For example, the TLV1572 has a single-ended analog input with a voltage range that extends 0.3 V beyond each rail. Conversely, the TLV1562 allows single-ended inputs similar to the TLV1572, and differential inputs (approximately 2 Vpp) operated in a different mode. Furthermore, some converters like the TLC320AD50 use a completely differential input structure. Understanding what the analog input voltage range looks like allows the designer to properly gain and bias an input signal and take advantage of the full dynamic range of the ADC.

Many circuits exist that properly bias an analog input signal. Two proven circuits for this function per the 1998 TI Analog Seminar are included below. Both circuits bias an ac input signal at mid-rail on a single supply amplifier.



Two examples for proper signal biasing fora single supply amplifier application

Figure 8. Input Signal Biasing Circuits

Input offset voltage (V_{IO}) is another parameter to consider on the amplifier. Even in a simple biasing or buffering application the amplifier introduces a dc error induced by the voltage difference inherent to the amplifier inputs and denoted in the data sheet by V_{IO}.

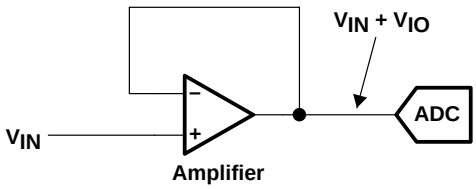


Figure 9. Input Offset Voltage (V_{IO})

The other important input error on the amplifier is input bias current, I_{IB}, which can be a very significant error if the signal on which the amplifier is working is represented by a relatively small current. As an example, some types of sensors can fall into this category. While V_{IO} is often easier to visualize, input current errors can also drastically affect resolution errors in an application. In general, it is good practice to keep the combination of both of these errors below 0.5 LSB in size, referenced to the size of one LSB on the data converter (see section 5.3).

5 Power Supply

Of course, devices used in the design must be able to withstand and function with the voltages used on a board. While this is obvious, there are other less obvious points that need to be explored, including power and ground planes, input/output voltage range, and the size of 1 LSB on the ADC.

5.1 Power and Ground Planes

Ideally, a board has both an analog and a digital ground plane. This helps isolate sensitive analog circuits—like an amplifier-from switching noise associated with the digital circuits. If a separate analog supply and ground plane are not possible, the power supply rejection ratio (PSRR) specification identifies problems that may be encountered from power supply noise. For newer amplifiers like the TLV2450, there is often a PSRR vs frequency graph in the back of the datasheet that can help if a designer understands the frequency characteristics of noise being encountered on the power rail.

5.2 Input/Output Voltage Range

Another effect of choosing any V_{CC} can be the input and output voltage range on the amplifier. Up until relatively recently, most amplifiers did not supply inputs and outputs that could swing to both rails. For example, the TLC2272 provides rail-to-rail outputs (RRO) but not rail-to-rail inputs (RRI). Instead, the TLC2272 has 1.5 V of headroom on the upper rail of the input. Thus, on a 10 V supply, the TLC2272 has an input range from GND to 8.5 V. Similarly, for a V_{CC} of 5 V, the TLC2272 still has 1.5 V of headroom and an input range from GND to 3.5 V.

The evolution of the amplifier has led to the innovation of rail-to-rail input and output (RRIO) amplifiers such as the TLV2462. RRIO amplifiers allow signals to swing between both rails, thus eliminating headroom on the inputs or outputs. This becomes increasingly important in low voltage applications, as a designer has a smaller input/output range with which to work. RRI comes at a price, however. Today, the construction of a rail-to-rail input stage introduces crossover distortion. For distortion-sensitive applications, the designer should consult both the op-amp vendor and the data sheet to determine the suitability of a particular amplifier.

5.3 LSB on the ADC

An ADC specification that varies with Vcc levels is the size of one least significant bit (LSB). This becomes clear with the following equation:

$$1\ \text{LSB} = \frac{\text{Vfullscale}}{2^N - 1} \tag{14}$$

Where n = resolution of the ADC

For the case of a 12-bit (ENOB) ADC, moving from a 5-V to 3-V full scale range results in a reduction in size of 1 LSB from 1.22 mV to 732 μV. For an ADC like the TLV1572 with a V_{CC} range of 2.7 to 5.5 V, this results in a range of LSB size (5.37 mV to 2.64 mV). The main concern is that, particularly in moving a system to a lower voltage, the LSB does not shrink to the point of being susceptible to system parasitics.

6 Summary

This report briefly covered various issues to consider when interfacing a general-purpose amplifier to a general-purpose ADC. With these things in mind, it should be straightforward to sift through many amplifier choices and find parts that interface nicely to an ADC and optimize system performance.

Summary Checklist

- Bandwidth – amplifier GBP vs ADC speed
- Resolution – amplifier SINAD vs ADC ENOB
- Analog Input – τ, drive current, and input signal vs ADC analog input range
- Power – amplifier PSRR, amplifier I/O voltage range, and ADC LSB

7 References

1. *Electric Circuit Analysis Second Edition*, by Johnson, Johnson, and Hilburn Copyright 1992, Prentice Hall, Englewood Cliffs NJ
2. *DSP/Analog Technologies 1998 Seminar Series*, by Texas Instruments Incorporated Copyright 1998

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