

A Next-Generation A/D Converter for Computer-Based Instrumentation

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Flexible A/D Converter Trades Speed for Resolution – Samples from 8 bits at 100 MHz to 21 bits at 10 kHz.

Test and measurement for the last decade has been undergoing a virtual instrumentation revolution. The paradigm shift of virtual instrumentation has empowered users to tailor generic inexpensive hardware to fit their specific needs with easy-to-use software.

Three key hardware technologies have been driving virtual instrumentation – PCs, signal processing, and data converters. Figure 1 illustrates the concept behind Virtual Instrumentation.

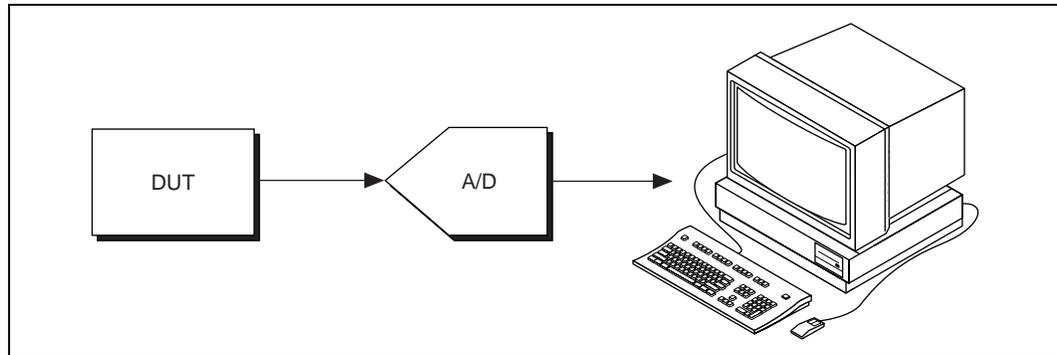


Figure 1. The Concept Behind Virtual Instrumentation

The device under test (DUT) is measured with an A/D converter (ADC). The ADC typically resides within the PC on its own plug-in board with associated programmable gain amplifiers and filters. The digital output of the ADC is connected to the computer through the PC bus.

Provided the ADC samples the signal from the DUT with sufficient speed and accuracy, virtually any measurement function can be performed in the computer by the execution of digital signal processing algorithms on the acquired data. Examples of measurement functions are DC and AC voltage, frequency counting, spectrum analysis, and amplitude distribution. With a programming language such as LabVIEW, these functions are very easily implemented in the computer.

There are several advantages of using virtual instrumentation compared to the more traditional approach of fixed-functionality instruments:

- You can perform any measurement function you desire.
- You can interpret measurement results very easily, for example, by performing statistical analysis on them.
- Your virtual instrument can be transformed into a completely different virtual instrument simply by changing its program, so you can reuse your hardware.
- Virtual instrumentation is more economical because it takes full advantage of the PC revolution.

In spite of the success of virtual instrumentation in many areas, ADC performance has been a limitation. Most ADCs are optimal only for certain applications. For example, a 16-bit 100 kHz ADC works fine for noise and vibration analysis, but does an insufficient job for many applications requiring higher bandwidth, such as oscilloscope functions.

On the other hand, an 8-bit 100 MHz ADC is normally excellent for most oscilloscope applications, but its dynamic range is insufficient for noise and vibration applications. For applications requiring both of these functions, the user has been forced to purchase two boards!

It would be a huge benefit to have an ADC that could operate both as a low-frequency, high-resolution converter and as a high-frequency, low-resolution converter – a flexible converter that could trade speed for accuracy.

Such a flexible converter could save money and ease the user's job in many ways. Not only are fewer input boards required, other associated costs could be reduced as well. It is easier to connect your DUT to one board instead of several; thus routing requirements via switches or relays are simpler and less expensive. A flexible converter system solution also requires fewer slots in a computer or in a PXI or VXI chassis.

The most important savings though, may be found in the simplified software development when control and acquisition of data from only one board is needed.

Flexible Resolution ADC

For these reasons, National Instruments has developed the proprietary Flexible Resolution ADC module. In addition to a high-speed ADC, the Flexible Resolution ADC contains a high-performance programmable gain instrumentation amplifier, a real-time digital signal processor (DSP) used for linearization and decimation of the digital output data, and a calibration circuit.

As illustrated in Figure 2, the converter samples at rates up to 100 MHz with 8-bit resolution and samples at lower frequencies with resolution that increases steadily to 21 bits at 10 kHz. Apart from offering flexible resolution over a wide range of sampling rates, the ADC offers unprecedented state-of-the-art performance at sampling rates below 5 MHz.

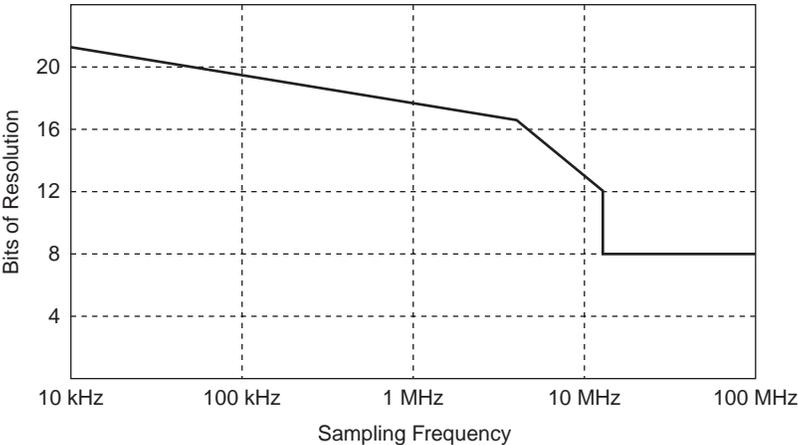


Figure 2. Resolution as a Function of Sampling Frequency for the National Instruments Flexible Resolution ADC Module

The ADC is based on a multibit delta-sigma converter topology, block diagrammed in Figure 3.

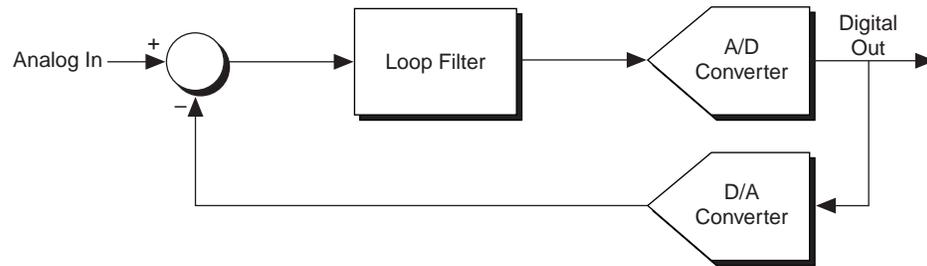


Figure 3. Block Diagram for a Multibit Delta-Sigma Converter

The Flexible Resolution ADC basically consists of a servo loop in which the analog input signal is fed through a subtraction node to a loop filter. The purely analog loop filter has high gain at low frequencies and, because of stability, low gain at higher frequencies. The filter output is digitized by an ADC sampling at a constant 100 MHz rate. The digital output is converted back to analog by a digital-to-analog converter (DAC) sampling at the same rate. The resultant analog signal is subtracted from the input signal in the subtraction node.

At low frequencies, where the loop has high gain, the output of the DAC is forced to be identical to the input. If any difference exists, it will be amplified, inverted, and subtracted until the DAC output is similar to the input.

Consider a multibit delta-sigma converter with a DC input voltage. The converter may be a first-order converter; that is, it contains one integrator as loop filter. Because the input voltage probably does not correspond to one of the discrete analog output values of the ADC, the result contains a small error. The error is detected in the loop filter and a persistent error will be accumulated until the loop filter has changed enough that a new code is obtained from the A/D converter. In this way the average value has to be exact. If it is not, it will be detected in the integrator and sequentially corrected until the error is zero.

From these considerations, it is evident that the conversion quality gets better at lower frequencies. It can also be seen that the output needs some processing. Oversampling and decimation will be described in the next section where the multibit delta-sigma converter is explained in a more analytical way.

An Analysis of the Multibit Delta-Sigma Converter

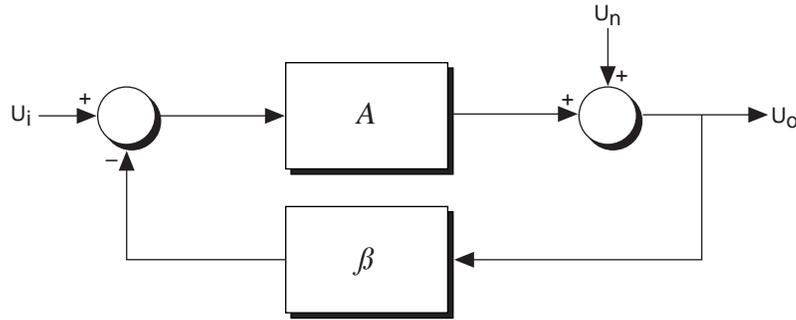


Figure 4. Block Diagram of a Servo Loop

The basic servo loop in Figure 4 consists of a gain block and a feedback with the respective gains of A and β .

The closed loop gain A_{cl} (from U_i to U_o) of the loop is:

$$A_{cl} = U_i/U_o = A/(1 + \beta A)$$

If A is sufficiently large,

$$A_{cl} \approx 1/\beta \quad \text{where } (\beta A \gg 1)$$

This means that when the loop gain βA is large, the transfer from input to output mainly depends on the feedback and is the inverse of β . In the case of the multibit delta-sigma converter, the feedback network is the DAC. The resultant transfer characteristic is the inverse of the DAC, which is an analog-to-digital transfer – exactly what we want.

An interesting property of the feedback loop is its ability to suppress signals added to the output of the loop. The gain from U_n to U_o (with reference to Figure 4) is:

$$A_n = U_n/U_o = 1/(1 + \beta A)$$

For the multibit delta-sigma converter, the quantization noise of the internal ADC is added to the output of the loop and is thus suppressed by the loop gain factor. The internal DAC does not add any quantization noise, because data coming out of the ADC is truncated and therefore can be converted without degradation by the DAC.

The Flexible Resolution ADC consists of an 8-bit ADC and an 8-bit DAC sampled at a constant rate of 100 MHz. The third-order loop filter basically consists of three cascaded integrators. The bandwidth of the loop filter, because of the stability of the loop, is limited to approximately 6 MHz. Figure 5 illustrates the resultant noise gain as a function of frequency. Noise gain is the gain the loop applies to the quantization noise from the internal ADC.

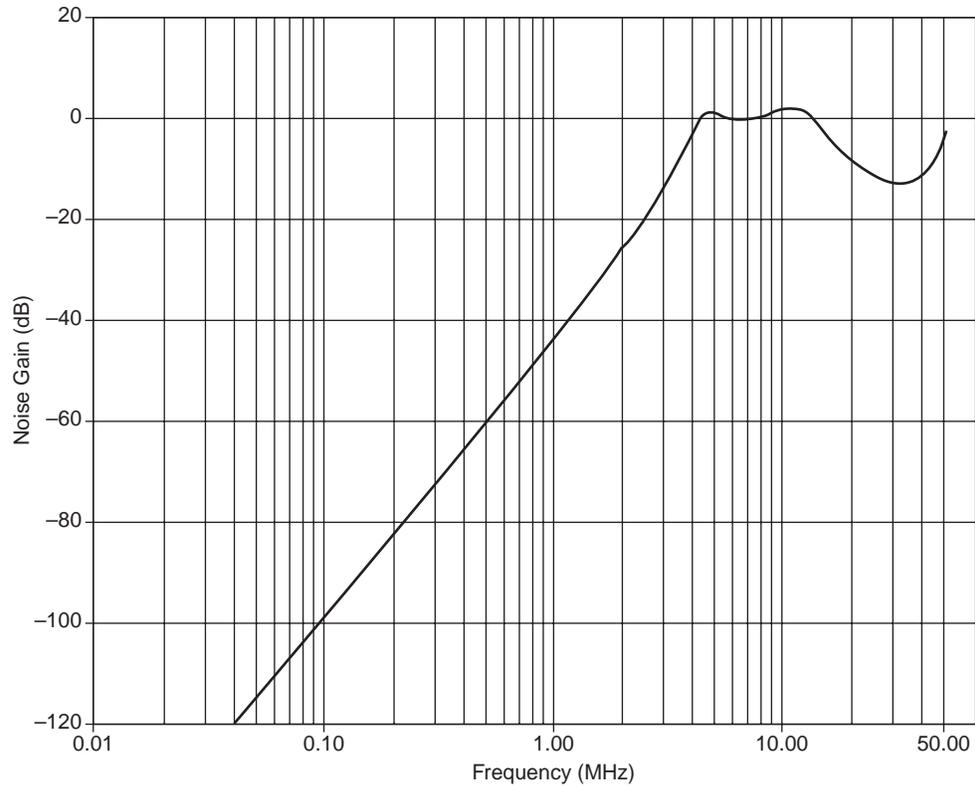


Figure 5. Noise Gain as a Function of Frequency

You can see from Figure 5 that the noise below 4 MHz is suppressed. This effect is referred to as noise shaping. The noise is shaped from low frequencies to high frequencies.

At 100 kHz, the suppression is approximately 100 dB, corresponding to an improvement of more than 16 bits of noise performance. Figure 5 also shows that noise actually is increased beyond 6 MHz. Analysis of the total noise in the system reveals that the total broadband noise energy is increased. However, the noise can be digitally filtered when high signal bandwidth is not needed. If higher bandwidth is needed, it is more advantageous instead to break the loop and send the analog signal directly to the internal 100 MHz ADC.

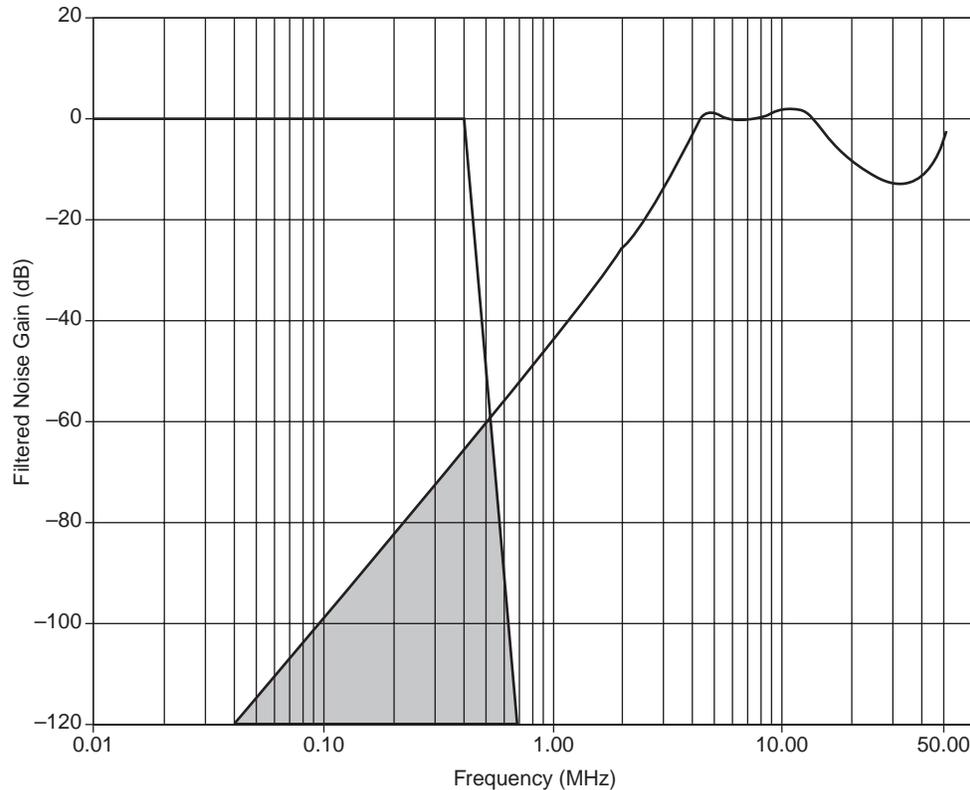


Figure 6. Applying a Lowpass Filter to the Converter

Figure 6 illustrates the results of applying a 400 kHz lowpass filter to the output of a multi-bit delta-sigma converter. After filtering, the only noise left is within the shaded area, which contains only a small residue of the original noise introduced by the 8-bit ADC.

Because the signal output from the digital filter is limited to 400 kHz, it is theoretically possible to represent the signal at a sampling rate of 800 kHz without any loss of information. However, because it is impossible to implement an ideal lowpass filter, resampling at 1 MHz is a more practical solution.

Digital Filtering

A significant advantage of digital decimation of oversampling converters is that antialiasing protection becomes very easy. You have to protect for aliasing within only a small span around the sampling frequency. The digital filtering in the decimation process takes care of the rest. In fact, the flexible converter theoretically does not need any antialiasing because the loop filter is analog and unsampled.

Assume a signal at a frequency greater than half the sampling rate is applied. After being filtered in the loop filter, the signal is converted and aliased to a low frequency at the output of the DAC in the loop. However, this spurious signal will be detected by the loop filter and suppressed by the loop gain of the filter, because the filter is purely analog and unsampled. Frequencies that alias to frequencies beyond the loop bandwidth are removed by the digital decimation filter.

Another significant advantage of digital filtering in conjunction with the multibit delta-sigma converter is the very low ripple and accurate phase response that can be obtained. The frequency response of the digital filter can be made arbitrarily accurate, provided sufficient computational power is available. The phase response of the digital filter can be made ideal. The frequency and phase response of the modulator are also very accurate for frequencies within the loop bandwidth, where high loop gain exists. At 100 kHz, for example, the ripple of the modulator is less than 0.00001 dB and the phase is within 0.0005 deg. This performance is conducive to very accurate multichannel applications.

Linearity

Theoretically, it is possible to digitally resample the output of the flexible converter to more than 24 bits resolution at a 1 MHz sampling rate. Practically, this is not possible because the architecture is based on 8-bit technology. An important design limitation to be considered is nonlinearity in the DAC internal to the loop.

Nonlinearity in the transfer affects the output in two ways:

1. It modulates the applied signal and creates nonlinear signal components. For example, a pure sine wave input will be modulated and harmonic components will appear at the output.
2. The frequency-shaped quantization noise modulates itself and creates a flat broadband noise floor, as illustrated in Figure 7.

For a conventional non-noise-shaped ADC, it is not necessary to take nonlinearity of noise signals into account, because the effect of the nonlinear modulation is less than the main noise signal. However, in the case of the frequency-shaped quantization noise signal, the nonlinear modulation signal will dominate at low frequencies where the quantization noise otherwise has been removed (see Figure 7).

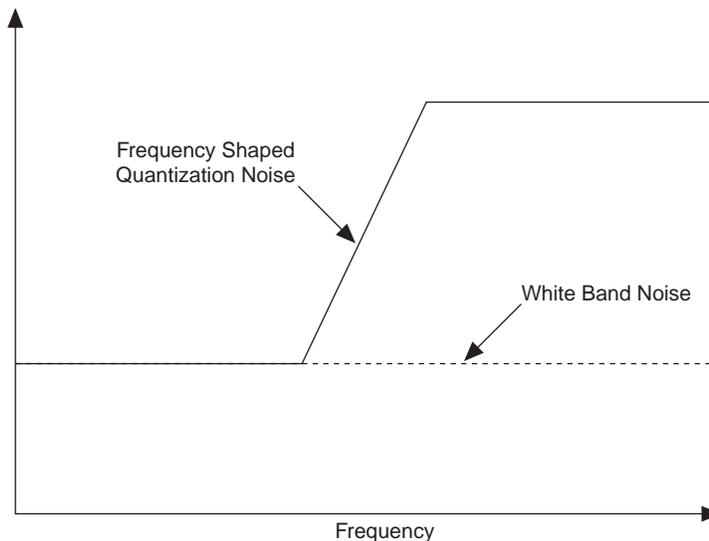


Figure 7. Broadband Noise Applied to the Noise-Shaped Output

For this reason, it is necessary to reduce the effects of nonlinearity before we can exploit the full potential of the multibit delta-sigma converter architecture.

Because linearity of the ADC in the loop is suppressed by the loop gain factor, only the DAC needs to be linearized. If the transfer function of the DAC is β , the resultant loop transfer is $1/\beta$. Hence, an ideal linear transfer from input to output can be obtained by digitally multiplying the output of the multibit delta-sigma converter by a transfer function similar to β .

The total signal chain from analog in to digital out is shown in Figure 8. An analog signal is input to the multibit delta-sigma modulator. The modulator outputs an 8-bit 100 MHz digitally sampled version of the input signal to a DSP.

This signal is corrected by applying a nonlinear transfer function similar to that of the DAC. The linearization takes every sample entered and translates it with 20 bits of accuracy before it is output to the decimation filter. This data is then entered in the decimation filter at the full rate of 100 MHz. The signal is filtered and digitally resampled to the desired sampling rate of 2.5 times the bandwidth.

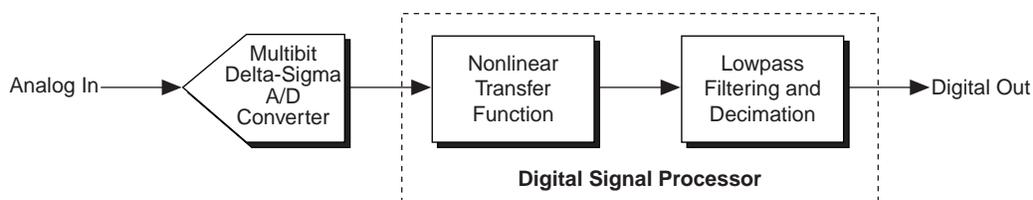


Figure 8. The Total Processing Chain from Input to Output

Digital Linearization of the Multibit Delta-Sigma Converter

The linearization process is essentially an emulation of the transfer function of the internal DAC. There are two main sources for erroneous conversion in a DAC:

- Static linearity error
- Glitch

The static linearity error is code dependent and is simply the deviation of the DAC output from the expected ideal output for a static input code. The error depends on only the input code and is easily compensated for in a simple look-up table.

The glitch correction is more complicated. Glitches occur when changing from one code to another in the DAC. Changing codes to a DAC, depending on the old and new code applied, may result in some current generators being turned on while other generators are turned off. If different delay paths between the current generators exist, glitches will occur.

The DAC used in the Flexible Resolution ADC is extremely fast, capable of converting at rates to 400 MHz. The time skew between internal current generators is accordingly low, typically some few picoseconds. Although glitch errors are small, it is desirable to compensate for them.

Because glitch compensation depends both on the current and the new code applied to the converter, the look-up table must be very large. However, the largest glitches depend mainly on the most significant bits applied to the converter; it is thus possible to significantly reduce the number of entries to the look-up table. In the Flexible Resolution ADC, we compensate for the six most significant bits.

Calibration of the ADC

Although it is possible to correct the internal DAC from 8-bit to more than 18-bit accuracy, temperature and time drift can easily change the behavior of the DAC so much that correction becomes virtually meaningless.

To calibrate the linearization circuitry within the DSP when required by time or temperature changes, the flexible ADC works in conjunction with a calibration generator and a thermometer. It is always possible on command to calibrate the Flexible Resolution ADC module to optimum performance.

The calibration generator contains a very low distortion sine wave generator. Using a National Instruments patented proprietary algorithm, the Flexible Resolution ADC derives the linearization coefficients from spectral analysis of the applied sine wave.

DSP Functionality Implemented in Reconfigurable Logic

Real-time decimation and linearization of a 20-bit wide 100 MHz digital signal is not a trivial task. General-purpose DSPs deliver only a fraction of the desired performance. Off-the-shelf hardware decimation processors are normally too slow and bit widths too shallow. If even possible, the off-the-shelf processor approach is expensive and lacks the necessary flexibility. To achieve the necessary computational power, the linearization and decimation algorithms are performed in dedicated hardware implemented in a reconfigurable field-programmable gate array (FPGA). A major advantage of using reconfigurable logic is that hardware resources can be shared for different decimation modes to minimize the hardware required.

Programmable Gain Instrumentation Amplifier

To maintain signal integrity from the device under test to the ADC, the Flexible Resolution ADC contains a high-precision programmable gain instrumentation amplifier. The amplifier, which has been optimized to match the performance of the ADC from DC to 100 MHz, has differential inputs for rejection of common-mode noise. The input stages are built with JFET transistors for low input bias currents and input impedance of 1 M Ω . Gains can be set to cover input ranges from 100 mV to 10 V in a 1-2-5 sequence. The programmable gain assures that all of the dynamic range of the ADC can be used for a wide range of input signals. The instrumentation amplifier also contains a new patented circuit that protects the amplifier from signals up to 42 V without degrading signal quality.

Performance Examples

This section shows some real measurements from the Flexible Resolution ADC. The first measurement illustrates noise performance. However, it is necessary to be cautious when dealing with noise in ADCs. Comparisons between noise performance in ADCs can be difficult if the converters are not sampled at the same frequency.

An ideal 14-bit, 10 MHz ADC has approximately -86 dB broadband noise while a 16-bit 100 kHz converter ideally has -98 dB broadband noise. But the noise output in the 10 MHz converter is distributed over a bandwidth 100 times greater. By decimating the output to the same rate as for the slower converter, the noise power is improved accordingly by a factor of 100, which is equivalent to 20 dB. This improvement makes the 14-bit converter the winner with -106 dB noise when compared over the same bandwidth.

For this reason, it is easier to compare between converters if the noise is specified by density. Density can be expressed as the noise amplitude at a given frequency measured through a 1 Hz bandpass filter. This way of noise specification is common for analog components such as op-amps.

For comparison, an ideal N-bit converter sampled at the frequency of F_s has the output density N_d measured in units of dB reference full scale per square root hertz (dB re $F_s/\text{SQRT}(\text{Hz})$):

$$N_d = N_x 6.02 \text{ dB} - 1.79 \text{ dB} - 10 \log((F_s)/(2 \text{ Hz}))$$

The first measurement shown (Figure 9) is a plot of noise density as function of frequency. No signal is applied to the converter and the only processing done by the DSP is linearization. A power FFT is performed on the data, and the magnitude of each of the FFT bins are rescaled to show the equivalent noise in 1 Hz of bandwidth.

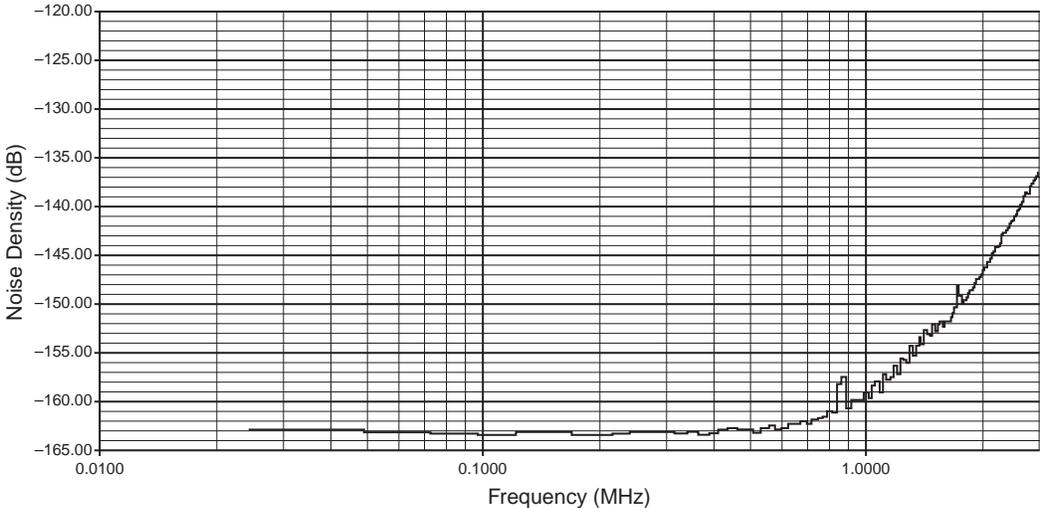


Figure 9. Noise Density as a Function of Frequency

The plot can be divided in two sections. The low band from DC to 1 MHz exhibits the very low noise performance of -160 dB re $F_s/\text{SQRT}(\text{Hz})$. This performance results from the instrumentation amplifier internal to the Flexible Resolution ADC. The noise level is equivalent to 17.5 bits at a sampling rate of 1 MHz.

The high-frequency band beyond 1 MHz shows rapidly increasing noise density as function of frequency due to decreased gain in the loop filters. Although it seems dramatic, the starting point is very low, and the performance is enhanced at frequencies below 6 MHz, compared to the performance in the non-noise-shaped mode.

Figure 10 displays a more traditional measurement of linearity in the converter. We applied a full-scale 3 kHz sine wave to the converter and the linearized and decimated the output to a 100 kHz sampling rate in the DSP.

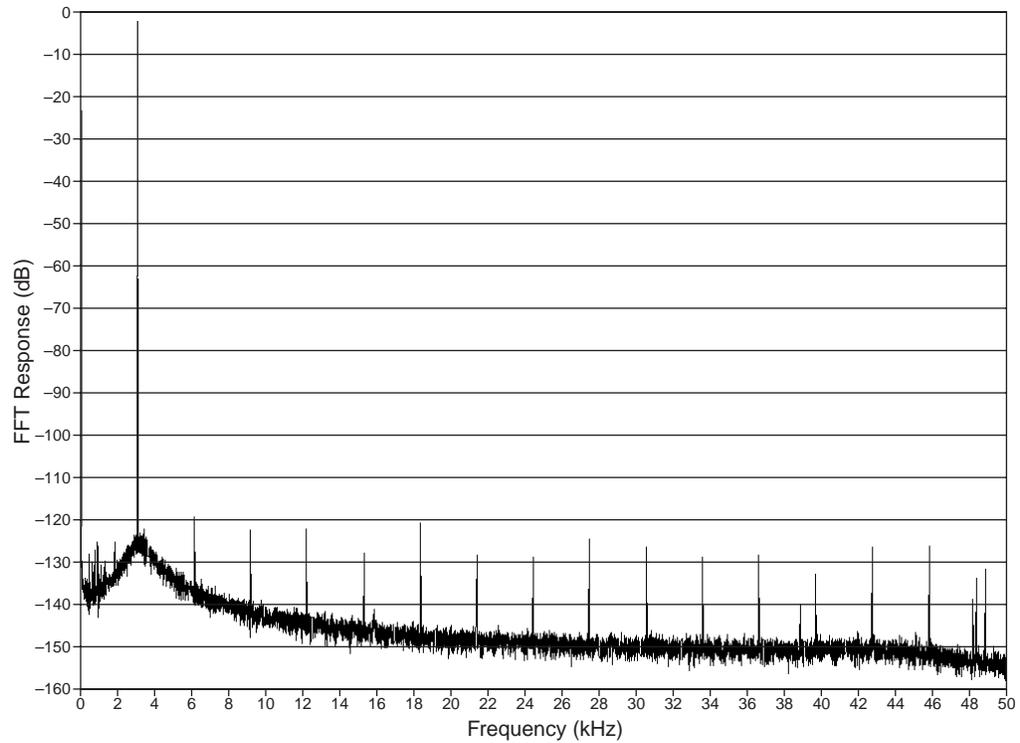


Figure 10. An FFT Plot of a 3 kHz Sine Wave 0 dB re Full Scale Measured with a Sampling Rate of 100 kHz

The spurious-signal-free dynamic range is approximately 120 dB. The noise floor, which is limited by the generator, is equivalent to 18.5 bits at the 100 kHz sampling rate. Figure 11 shows an FFT plot of the same signal attenuated to 60 dB below full scale. The plot exhibits a noise floor more than 150 dB below full scale.

Because the sine wave has been attenuated by a factor of 1000, it is no longer the dominant signal and the true noise performance of the ADC is revealed to be 19.5 bits at a 100 kHz sampling rate. The linearity performance at -60 dB is at or better than 25 bits.

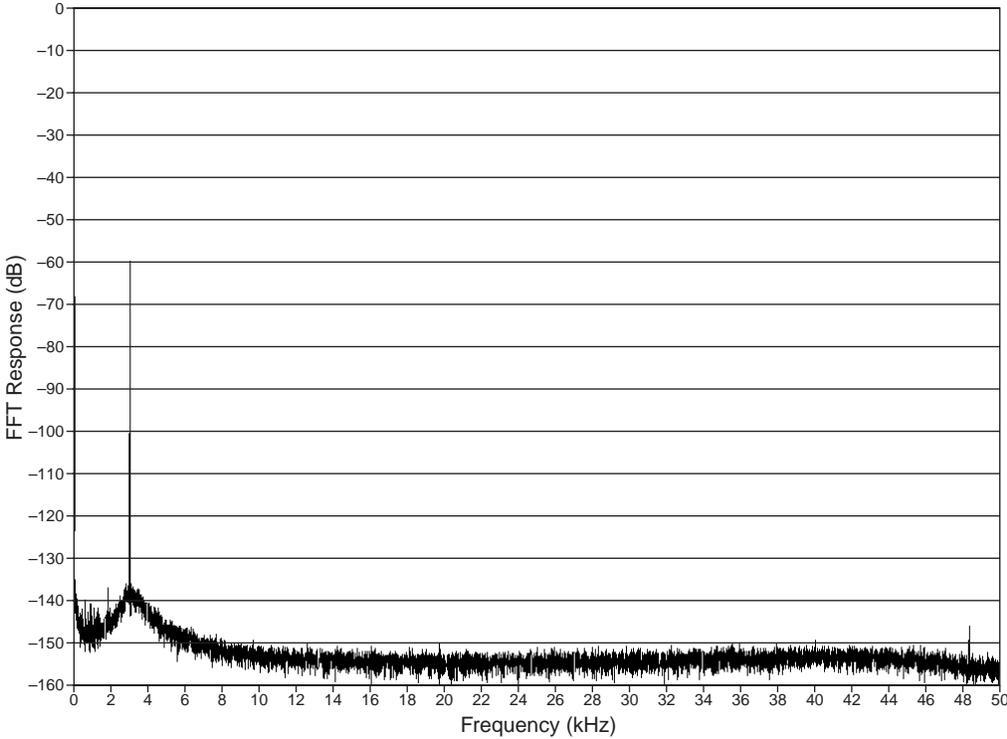


Figure 11. An FFT Plot of a 3 kHz Sine Wave at -60 dB re Full Scale Measured at a Sampling Rate of 100 kHz

Summary – A Next-Generation A/D Converter

A multibit delta-sigma converter, a powerful DSP, and a precision calibrator together form an ADC subsystem with a very important flexible characteristic – it can trade off speed for resolution. The Flexible Resolution ADC works in two modes – a fast 8-bit mode for transient and timing analysis and a slower increased-resolution mode, where resolution is dependent on sampling rate.

In the increased-resolution mode, the ADC exhibits near ideal performance – noise and linearity errors are small; frequency and phase response are good; and antialiasing is good.

This performance level is achieved by extensive use of an onboard DSP engine in conjunction with a self-calibration routine executed in the host computer. This scheme is an excellent example of how next-generation instrumentation performance is achieved by taking full advantage of the extensive capabilities made possible by the PC revolution.



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