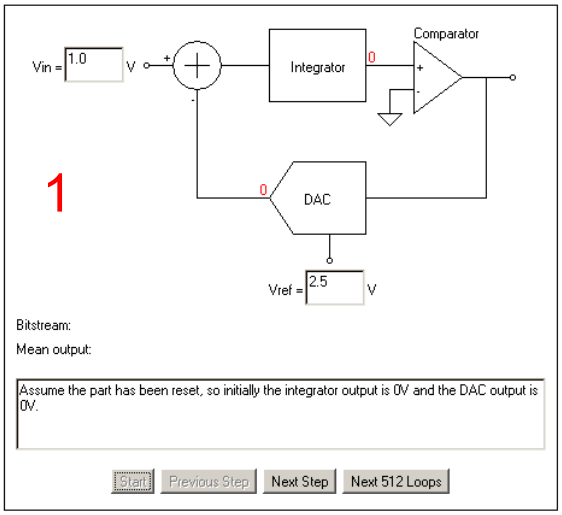
Interactive Design Tools

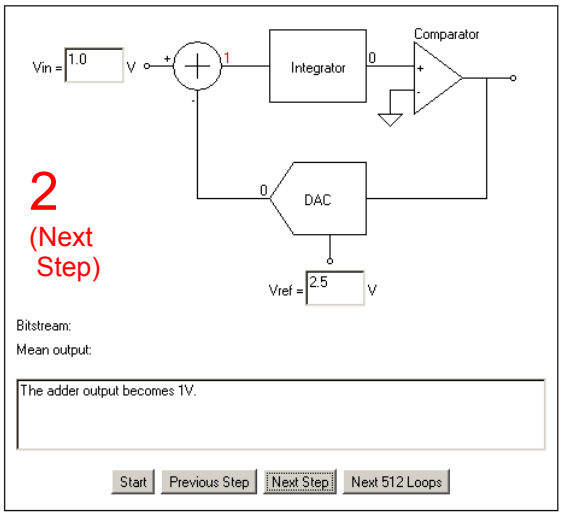
Analog-to-Digital Converters :

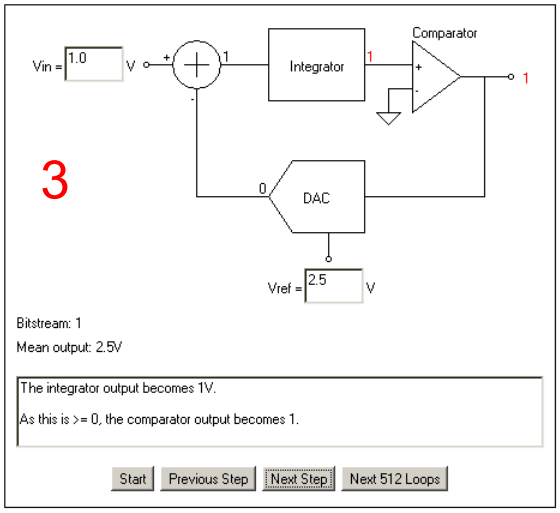
Sigma-Delta Analog-to-Digital Converters [1st order, bit-stream output] :

Sigma-Delta ADC Tutorial

An interactive **illustration** showing the behavior of an idealized sigma-delta A/D converter …







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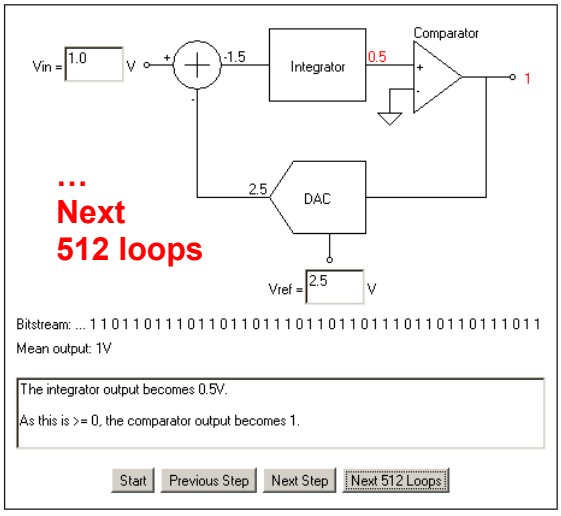

The **feedback** tries to keep the integrator output at zero by making the ones and zeros output of the comparator equal to the analog input.

The stream of 1's and 0's is subsequently digitally filtered (**not** shown) to produce a slower stream [word rate] of multi-bit samples.

The sigma-delta modulator loop typically runs at a **much higher** frequency than the final output rate of the digital filter. For example, a converter with a 2kHz output data rate may have a modulator loop frequency of over 2.5MHz.

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Instructions

The diagram inside the applet shows a basic first order sigma-delta modulator. More ophisticated parts may have multiple modulators and integrators however these tend to obscure the underlying sigma-delta principle.

Sigma-Delta Modulator Operation

The input voltage V_{IN} is first summed with the output of a **feedback** DAC. This summing can be accomplished by means of a switched capacitor circuit which accumulates charge onto a capacitor summing node. An **integrator** then adds the output of this summing node to a value it has stored from the previous integration step. A **comparator** outputs a logic 1 **if** the integrator output is greater than or equal to zero volts and a logic 0 otherwise. A **1-bit DAC** feeds the output of the comparator back to the summing node: $+V_{REF}$ for logic 1 and $-V_{REF}$ for logic 0. This feedback tries to keep the integrator output at zero by making the ones and zeros output of the comparator equal to the analog input.

The stream of 1's and 0's is subsequently digitally filtered (not shown) to produce a slower stream of multi-bit samples. The sigma-delta modulator loop typically runs at a much higher frequency than the final output rate of the digital filter. For example, a converter with a 2kHz output data rate may have a modulator loop frequency of over 2.5MHz.

How to use this tool

Enter an ADC **reference voltage** in the lower input field. The ADC will convert input voltages that fall between +/- V_{REF}. The demo will output all ones for a $+V_{REF}$ input and all zeros for a $-V_{REF}$. input. However a real ADC would use internal scaling to limit the allowed ones and zeroes density to around 10% minimum.

Enter the **voltage** to be converted in the V_{IN} field.

Note: V_{IN} and V_{REF} can only be changed at the start of the tutorial, so you may have to click the *Start* button to enter new values.

Click the *Next Step* button to move the tutorial forward a step. At each step the diagram is updated to show the current output of each block.

To see the outputs at the previous step of the tutorial, click the *Previous Step* button.

To advance the tutorial 512 complete loops of the modulator, click the *Next 512 Loops* button.

Example

Let V_{IN}=1.0V, V_{REF}=2.5V.

The outputs from the comparator will be: 1, 0, 1, 1, 1, 0, 1, 1.

This means 6 of the 8 outputs have been a 1; i.e. output is 75% of fullscale.

The allowed input range is -2.5 to +2.5 (+/-V_{REF}) so the span is -2.5 to +2.5.

With a 1.0V input the input is 3.5V above the bottom of the 5.0V span or 70% of fullscale.

If we continue looping, the ones density of the above output stream will get closer and closer to 70%.

The digital filter does a much better job at detecting this trend then our simple count ones method.