

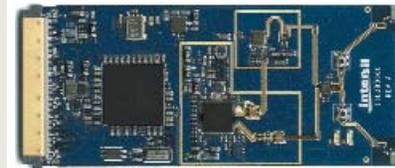
BY MANIWA

## LOW OR HIGH END, ADCs ARE UNDER PRESSURE TO PERFORM

The analog-to-digital converter (ADC) segment is closely aligned with the overall drive to perform as much signal processing in the digital domain. The drivers and trends are similar to the pressures that affect the logic areas. Converters are moving toward more bits and higher speeds. In these areas, the drivers are parallel to the digital world, and they look to smaller feature sizes for higher levels of integration.

Unfortunately, the bypass capacitors are getting larger than the IC packages, so reducing space becomes more difficult. The increases in speed and data word resolution force converter makers to pay extra attention to power consumption and packaging. A revolutionary change in architectures is being driven by requirements for smaller and lower power. Some of these new designs will be possible to embed in larger chips as further building blocks.

While the high-end products focus on performance, the low- and middle-range products must address both performance and cost. The mid-range converter space, with converters with a sampling rate of 1 to 10 Msamples/s, usually resides in the 8- to 16-bit resolution level.



The cost of this

mid- or low-range converter is just as significant a parameter as its monotonicity or linearity.

Precision is adequate in the low-cost areas. To address the ever-changing needs of converter users, vendors are expanding their converter product portfolio. Their focus is on low power, smaller packages, and integrated references. ADCs need to convert as fast as possible, but faster converters are typically only necessary for the lower latency, not the higher speed. Most users want to complete the conversion and power the converter down to achieve an overall lower-power consumption figure.

For example, many users employ 200-ksample/s converters but only require 10-ksample/s data rates. Therefore, they can get a 98% reduction in operating power, compared to other “low-power” converters, by powering down between conversions. An addendum to the “sampled” samples is a growing need to perform data reduction or averaging before sending the data out.

Other important ADCs beyond just voltage inputs include voltage to frequency, frequency to voltage, and rms-dc.

The lower sophistication and experience of users means that vendors must do a better job of design and support. The customer is easily responsible for the system, but not expert in enough facets of the design to be good in everything. Smarter customers will rely on their semiconductor vendor(s) to take responsibility for the analog and special-purpose mixed-signal portions. **ED**



TOP TEN

**>FULLY DIFFERENTIAL OUTPUTS** will find greater use in high-performance and low-voltage converters for better dynamic range or higher data rates.

**>POWER-SUPPLY VOLTAGES** track the digital components. Lower supplies help the power consumption in the digital sections but make the analog sections more difficult.

**>MORE "EXOTIC" SEMICONDUCTOR** processes will be used in the search for higher speeds and lower power.

**>ANALOG FRONT-END COMPONENTS** will see increased integration. Putting analog-signal-processing components on-chip reduces the design effort and also improves signal quality.

**>MORE INTEGRATION IS EXPECTED** with digital post-processing functions. This level of integration reduces the processing load on the system processor or DSP, which also limits power consumption in the logic section of the system.

**>SPEEDS ARE RISING.** First, higher conversion rates reduce data latency and, with a gated sampling scheme, can reduce system power consumption. Plus, higher analog bandwidths let the system capture faster signals.

**>SENSOR-SPECIFIC CONVERTER SUBSYSTEMS** will become more popular. As analog knowledge slowly slips away from systems design groups, more of the analog subsystem will be integrated into a single package.

**>OUTPUTS ARE MIGRATING** from the parallel outputs to I<sup>2</sup>C and SPI (serial packet interface), as well as other serial interface structures. This change simplifies the design interfaces.

**>INTEGRATED AVERAGING AND DATA REDUCTION FUNCTIONS** will limit the loading of DSPs in a system. Processing in the analog domain helps slash latency and power consumption.

**>LOWER POWER** is becoming a necessity. While most analog subsystems aren't battery-powered, system power consumption is a serious design issue, particularly as the analog subsystems integrate more functions into a single chip and the packages shrink.

**MORE-INTEGRATED ADCs WORK ON LESS POWER**

**ELECTRONIC DESIGN (ED):** Is there a clear direction for power supplies for converters?

**Osgood:** Analog functions are having to address the different voltage standards, dropping from 5 to 3 V and lower. People using DSP and other high-speed digital functions are moving to below 2 V to try to keep the number of supplies low. Everyone is moving down in supply voltage. For the high-speed converters, when people can use the parts at a lower voltage, they will. It's hard to get full accuracy (and your money's worth of bits) when the converter works on less than 1-V swing. At the same time, many systems use multiple supplies—one for the analog and one for the digital parts. The precision parts are going off of the digital board. However, some of the industrial controls still use ±15-V supplies for everything.

**ED:** Do you expect to see more converter variations?

**Osgood:** Certainly, the increase of other functions will be integrated with the converter. For example, adding the amplifiers and buffers to make the complete analog-signal-processing chain makes it easier for the end users to configure the system, and it reduces some of the data processing in the DSP. We're going for targeted applications that address specific signal and data requirements at the high end. At the same time, precision converters are mostly standard catalog items. People just look up their speed and precision requirements and buy something to meet them. When they look at spinning variations, it is in vertical equipment markets. The focus on the end equipment leads to higher levels of integration.

**ED:** Is there a practical upper limit on analog and mixed-

signal circuit integration?

**Osgood:** Not really. Higher levels of integration provide multiple benefits, including higher reliability, lower total cost, higher performance, and shorter time-to-design completion. The design is finished sooner because the analog signal chain is no longer a lot of discrete components, but a single part. For example, they have a 24-bit analog-to-digital converter (ADC) with a microcontroller and a 16-bit DAC in a single package. Another highly integrated function is a multi-channel ADC and digital-to-analog converter (DAC) on one chip, with both types of converter in the same package. The increased level of integration is just a grouping of standard building blocks used in fairly standard configurations.

**ED:** What do you expect to see in processes than other standard CMOS?

**Osgood:** ADCs are process-limited. The analog and digital resolution is a function of the device characteristics. A fast 14-bit ADC needs a sample-and-hold with precision capacitor ratios and values. The larger the cap, the better the accuracy (up to a point). But the high-value capacitors slow the response. So the only way to get a higher resolution is to get faster parts to charge the capacitors quicker. If the latest CMOS process cannot provide the necessary speed, we will move to other processes to achieve higher speeds and accuracies in our converters.  [www.ti.com](http://www.ti.com)



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BY MANIWA

## DACs: BRIDGES FROM THE COMPUTER TO THE REST OF THE WORLD

Like their analog-to-digital converter (ADC) counterparts, digital-to-analog converters (DACs) are moving toward higher speeds and resolutions at a lower operating power. The primary drivers are higher speed, greater resolution, and lower power. Moreover, higher integration is taking place among DACs, with digital error correction and post processing now included.

Bit resolution is increasing from a median of 8 bits to higher bit counts, reaching a plateau at about 14 bits. Most users don't go above 14 bits because the board layout is more critical and because the system can't use any additional bits. The noise floor and dynamic range of the converter dominate bit resolution. Thus a drop in supplies, caused by digital parts moving to smaller process geometries, reduces the possible dynamic range and increases the sensitivity to noise.

Resolution increases require more internal devices, but the higher speeds tend to force reductions in bit counts due to internal capacitance. For very high speeds, amplifiers and other internal components will need to go to an SOI-type process to minimize device parasitic elements.

Converters are moving toward more bits and higher speeds. In these areas, the drivers parallel the digital world by going to smaller feature sizes for higher levels of integration. Yet unlike their ADC cousins, the D/A parts are already in the best technology. The processes don't stand in the way of better performance, but the devices won't lead the move into the next smaller process generation. The parts aren't process-limited, although the output voltage must be within less than 1-LSB accuracy of an absolute value on the output. ADCs can scale the input voltage for any reasonable range either internal or external to the chip.

Precision is adequate in the low-cost areas. The string DAC architecture is now available in single, dual, and quad configurations, and they ship for less than \$2 in quantity. The architecture sacrifices internal linearity, but this is acceptable in the common control loop or calibrated sensor applications. Usually the sensor has a greater error budget than the converter, so the converter need only be monotonic.

A smaller die tends to imply lower power, but the form factor also is shrinking. The challenge is to make the design faster with lower power at the same time, so the thermal resistance isn't an issue in use.

Even though the shift is on to smaller packages, DAC functions are becoming more highly integrated. DACs are moving toward maximizing the number of parts in the package. Whole subsystems can include buffers and may even incorporate other types of converters and interfaces into the rest of the system. One ongoing change is to have differential signal paths for a higher dynamic range and higher speeds in the signal chain. **ED**

### TOP TEN

**>HIGH-RESOLUTION DACs** will go to 18 bits, which is already common for the analog-to-digital converter (ADC). The digital-to-analog converter (DAC) must move up to continue as part of a matched set. Further increases in resolution beyond 18 bits will take much greater effort in system-level design, which may not be worth the additional effort in the pc-board and interconnect designs.

**>THE COST OF THE HIGH-VOLTAGE ( $\pm 10$ -V)** parts will track the rest of the products, so higher supply voltage won't cost a premium. The continuing existence of separate, high-voltage analog sections will continue to drive the bifurcation of supplies, as the designers start to look for better system performance as compared to power-supply compatibility.

Look for some very high supply voltage parts for 42-V automotive applications. The auto market is already moving the system supply from 12 to 42 V in some of the high-end vehicles. The auto makers are reluctant to add one more power supply to their systems, but they still need high accuracy and high noise rejection in the components they use for systems.

**>THE NUMBER OF CONVERTER TYPES** and capabilities will continue to increase, with the set of all possible parts numbers significantly growing. Just as in the amplifier area, application-specific converters will proliferate with many variations within a set of speeds and bit resolutions. The wide range of applications means that the "best" converter will always contain specifications that don't exist within a single IC.

Multichannel ADC and DAC reside on a single chip, with both types of converter in the same package. The need for matching and minimal data skew requires that the parts of an analog subsystem be in the same package. The challenge is in managing the differences between the processes for ADCs and DACs, which are optimized for disparate parameters.

**>COMMUNICATIONS CIRCUITS need high-linearity and low-distortion specifications. The move to digital modulation adds very high requirements for linearity, settling time, and distortion in a digital transmitter. The challenge is to improve speed and linearity while simultaneously reducing power consumption.**

**>PACKAGE SIZE continues to decrease, from surface-mount packages, to SOT, and even to chip-scale packages, which are really just encapsulated dies with a set of external connections. The smaller packages allow for minimal footprint and also simplify signal routing on the pc board.**

**>DATA CONVERTERS FOR IF APPLICATIONS are coming online. The zero-IF transmitters are still a few years away, so intermediate architectures are going to prevail for a while. These parts must have a large dynamic range and low noise and distortion to minimize the processing load at the DSP, allowing the DSP to perform all demodulation.**

**TOP TEN**

>**EXPECT MORE DACs IN SOI (silicon on insulator) as frequencies go up to 1.8 GHz to also meet the requirements for low noise. The existing silicon processes are not able to meet all of the device specifications for speed and noise. The costs of the exotic processes, however, may become a hurdle, as the higher-performance parts cannot maintain too much of a premium over the lower-performance parts.**

>**THE TREND TO SMALLER PROCESS GEOMETRIES** in the digital sections of the systems forces lower supply voltages. The converters will have to track the rest of the system, or it will necessitate adding level translation functions on the digital inputs. The overall system compatibility is an issue if the system designers are going to get their money's worth from the high-bit-count converters without having to add more parts just to interface the low-voltage digital logic to the high-voltage analog.

>**INTELLIGENT CONVERTERS** will take advantage of the logic process scaling to add functions that will provide local data processing before transferring the data to the outputs. The converters will become more power-aware. They will use the local built-in intelligence to limit power consumption to only those intervals that require operations.

>**REDUCTION IN PERIPHERAL COMPONENTS:** The inclusion of local intelligence in conjunction with the increases in integration levels means that more converters will have self-calibration and linearity and offset compensation on-chip. This signals the early ending of the "binary" voltage references and tighter closed-loop control of the external transducers without much intervention from the digital controllers.

**MODELING HOLDS KEY FOR CONVERTER ADVANCES**

**ELECTRONIC DESIGN (ED): What is your focus at Linear?**

**Gross:** Function is key for our customers. We provide a set of very high-quality intellectual property functions for our customers. By focusing on the performance, they can create the specific circuits that fit the design requirements of the most critical systems. Manufacturing and the ability to perform specific functions are important to us and our customers.

**ED: How do you go about improving performance?**

**Gross:** Transistor count is not the key motive for changes in designs. The technologies and architectures continue to advance in all directions. Converters are moving toward more bits and higher speeds. In these areas, the drivers for change are parallel to the digital world and continue to move toward the smaller feature sizes that enable higher levels of integration.

**ED: How do you manage the changes in technologies?**

**Gross:** One key is the ability to get accurate device modeling for the designs. The smaller devices don't model well with the simple models. They used to employ a level 2 MOS model with about 10 parameters. Now they use a BSIM 3 or 4 with over 80 parameters. One problem is that the short channel effects don't correspond as well in the older models. Out of necessity, the foundries have good modeling people on staff. They understand the tools and methodologies needed to extract models that have high correlation to the physical devices in the ICs.

In addition to the manufacturing models, we also need specialized models for our special devices, and the special

functions in the chips. These are unique capabilities that enable breakthrough architectures.

One challenge is to get some correlation between the smaller line sizes and the disturbing trend toward lower levels of robustness. For example, electrostatic discharge (ESD) protection is down in the smaller processes. Analog structures need to have ESD protection and low load and parasitic characteristics. We cannot use a digital ESD structure with leakage current of 10 nA in a 25-pA input device. New processes require an empirical process to get the appropriate level of ESD protection, because the protection circuits need to be bulk and not surface conduction devices.

**How do your designs affect the manufacturing?**

**Gross:** Testing is another challenge. We have to test all parts to guarantee all parameters. This challenges the testing capabilities and test equipment, because the tester has to be much better than the state-of-the-art ICs. In addition, the test engineers have to resolve diametrically opposed characteristics: shortest test time possible and as accurate and complete as possible. A low-noise amplifier is best checked for noise by averaging over a fairly long time, milliseconds or seconds. But the tester needs to be finished with its testing in under 10 ms. **ED**



William Gross/  
**VICE PRESIDENT & GENERAL MANAGER, SIGNAL CONDITIONING**  
Linear Technology Corp.

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