Analog-to-Digital Converter Survey & Analysis

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References:

1. R.H. Walden, "Analog-to-digital converter survey and analysis," IEEE Journal on Selected Areas in Communications, vol. 17, no. 4, pp. 539-550, April 1999.

2. R.H. Walden, "Performance trends for analog-to-digital converters," IEEE Communications Magazine, vol. 37, no. 2, pp. 96-101, February 1999.

Outline

- Introduction
- ADC survey
- Characterization
- Performance Limits
- Architectures
- Trends
- Conclusions

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What Does an Analog-to-digital Converter Do?

- **It converts continuous-time signals to discrete-time binary-coded form. Two purposes are (1) to enable computer analysis of the signal, and, (2) to enable digital transmission of the signal.**
  - **Some examples of continuous-time signals:**
    - **speech, medical imaging, sonar, radar, electronic warfare, instrumentation, consumer electronics, telecommunications,…**
  - **The conversion can be thought of as a two-step process:**
    - **sampling the input signal in time, usually at regularly-spaced intervals; f_{samp} = 1/T, where T = sampling interval**
      - Example, for f_{samp} = 1 gigasample per second, T = 1 ns.
    - **quantizing (or digitizing) the samples in amplitude, usually voltage. The full-scale input voltage is divided into 2^N sub-ranges where N = the ADC's resolution (number of output leads).**
      - Example, for N = 12 bits, a 1-Volt full-scale range is divided into 2^N = 4096 levels. The size of the least-significant bit (LSB) is 1 V / 2^N = 244 μV.

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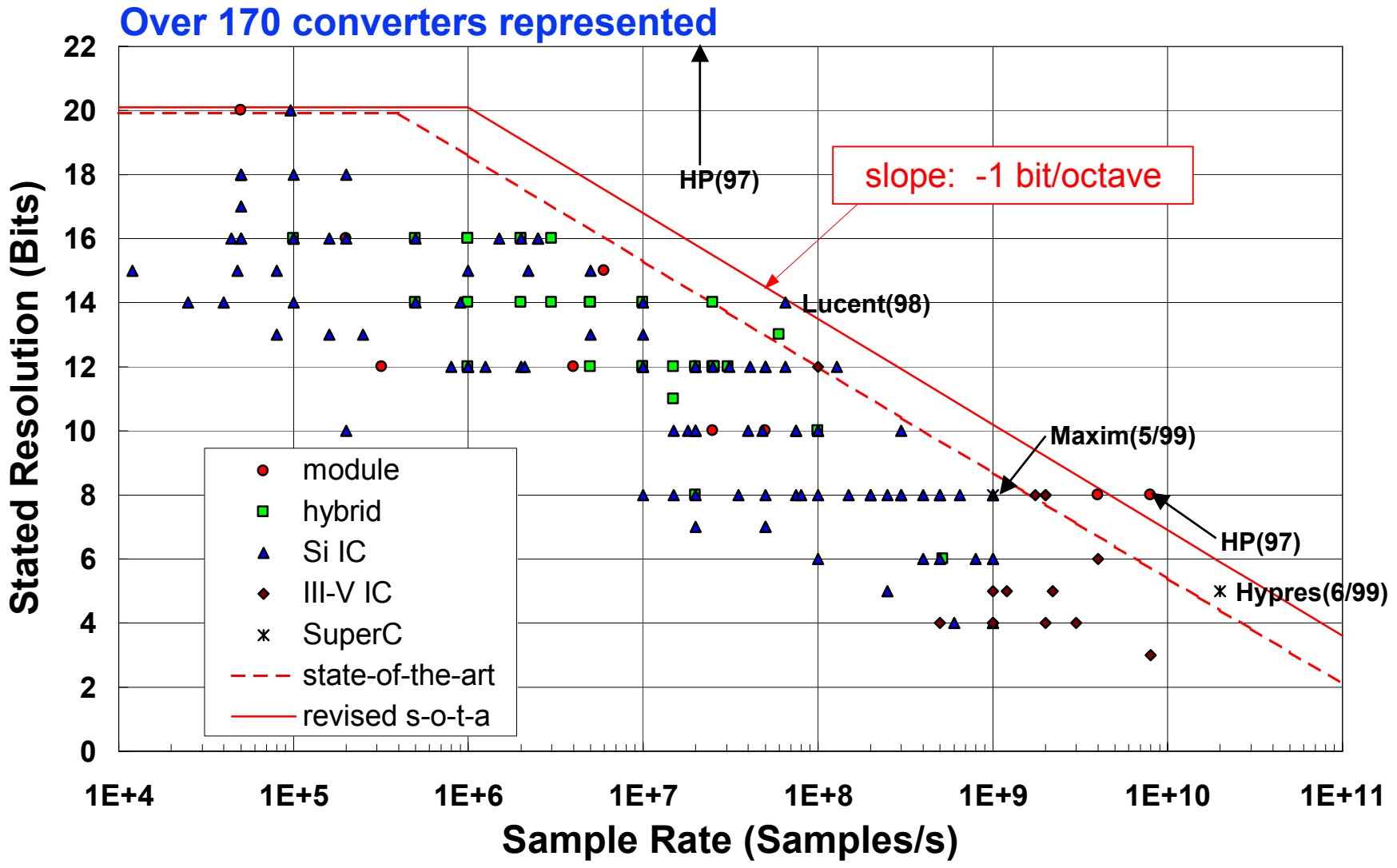
Analog-to-Digital Converter Data: Stated Resolution



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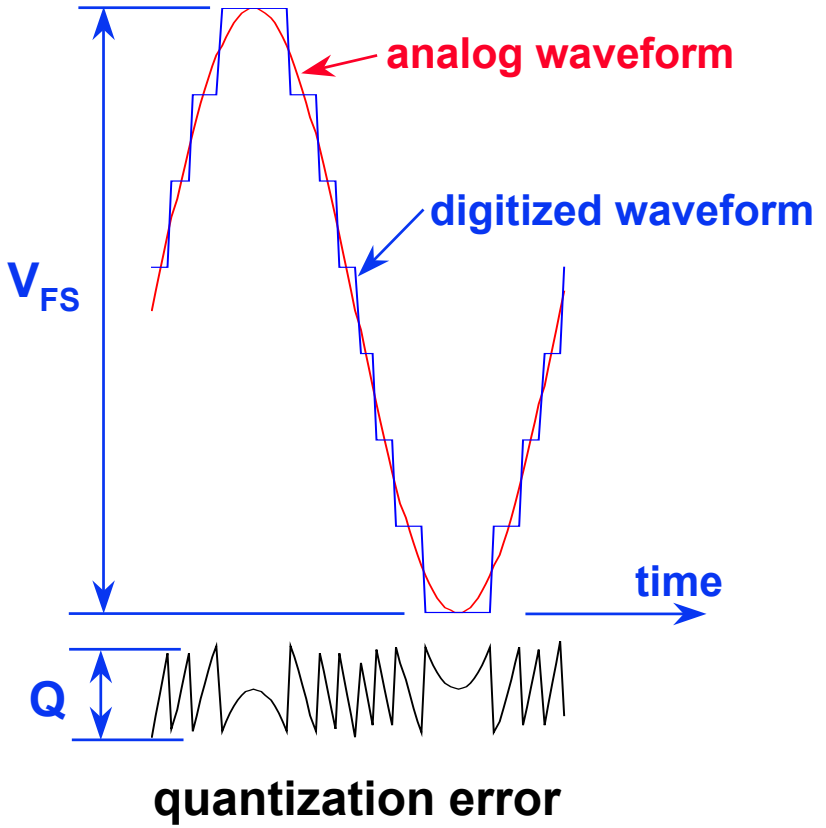
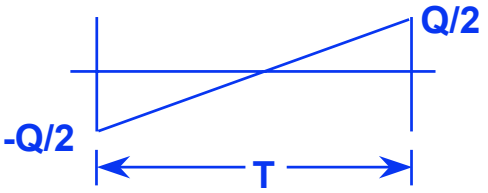
ADC Basics: Quantization Noise

Sinusoidal Signal



Randomized Signal



Q = LSB
= $V_{FS}/2^N$
N = ADC Resolution
T = sampling interval

$$e(t) = Q \cdot (\frac{t}{T} - \frac{1}{2})$$

$$NP_0(rms) = \sqrt{\frac{1}{T}\int_0^T [Q \cdot (\frac{t}{T} - \frac{1}{2})]^2 dt} = \frac{Q}{\sqrt{12}}$$

$$SNR(dB) = 20 \cdot \log_{10}(\frac{V_{FS}(rms)}{NP_0(rms)})$$

$$= 20 \cdot \log_{10}(\frac{V_{FS}}{2\sqrt{2}} \frac{1}{\frac{V_{FS}}{2^N\sqrt{12}}}) = 6.02 \cdot N + 1.76$$

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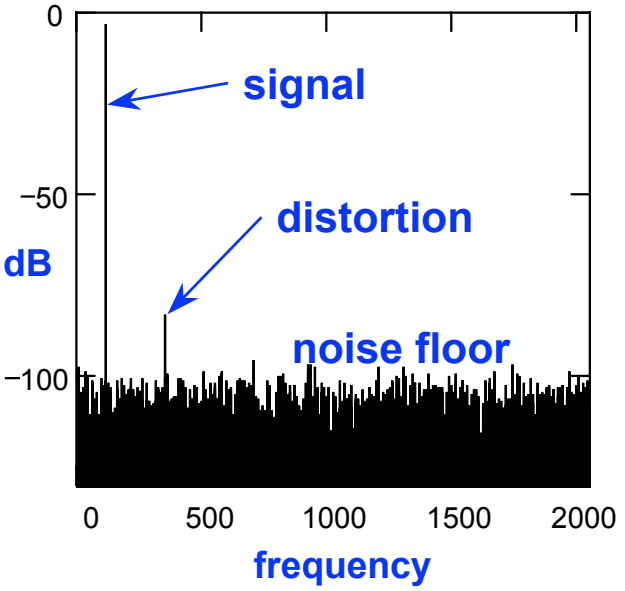
ADC Characterization

- **Quasi-static tests**
  - Differential nonlinearity, DNL
  - Integral nonlinearity, INL
- **Dynamic tests**
  - Collect 2^{bits} samples "at speed" and compute fast Fourier transform (FFT)
  - Determine signal-to-noise ratio, spurious-free dynamic range, noise power ratio
- **How do we count bits?**
  - Stated resolution = physical number of output leads (bits)
  - Signal-to-noise ratio, SNR(dB) = $6.02b_{eff} + 1.76$
    - b_{eff} = SNR bits = (SNR(dB)-1.76)/6.02
    - determined for $f_{sig} < f_{samp}/2$
  - Spurious-free dynamic range, SFDR(dBc)
    - SFDR bits = SFDR(dBc)/6



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Effective Resolution Bandwidth (ERBW)

- **Measure SNR vs f_{sig}, f_{samp}**
- **ERBW is the signal frequency where the SNR is 3 dB below the low frequency value**
- **If the ERBW is $\geq f_{samp}/2$, then we have a Nyquist converter**
- **In this presentation:**
  - quoted SNR values correspond to $f_{sig} << f_{samp}/2$
  - ADCs in this survey have $0.25f_{samp}$ <~ ERBW <~ $0.5f_{samp}$

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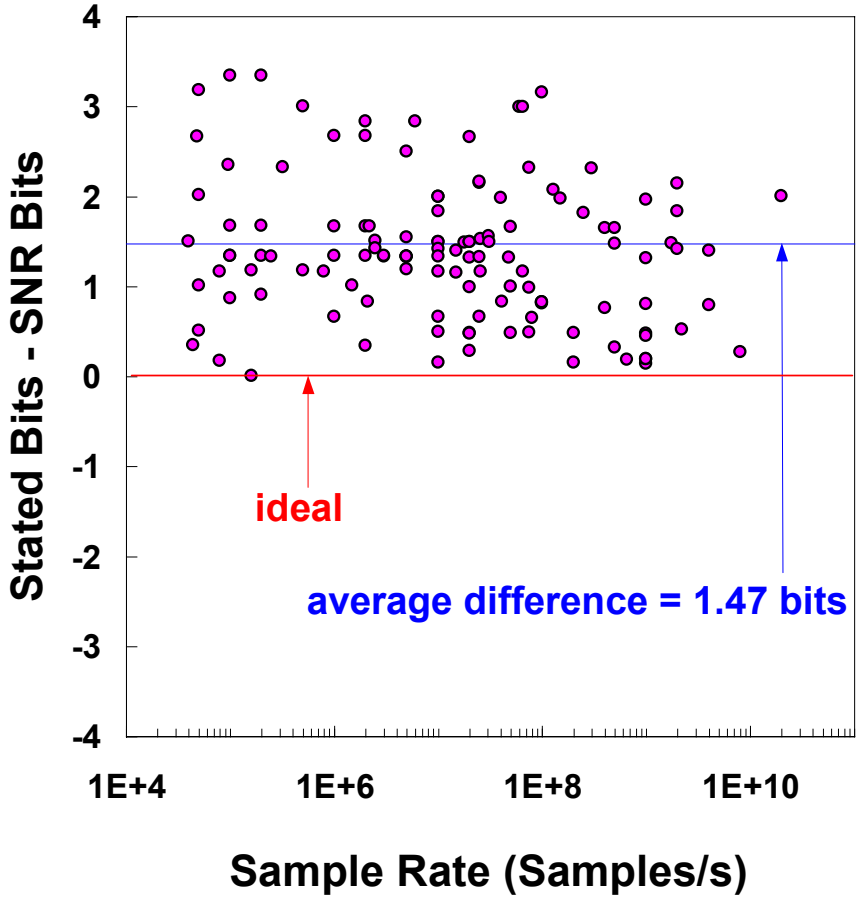
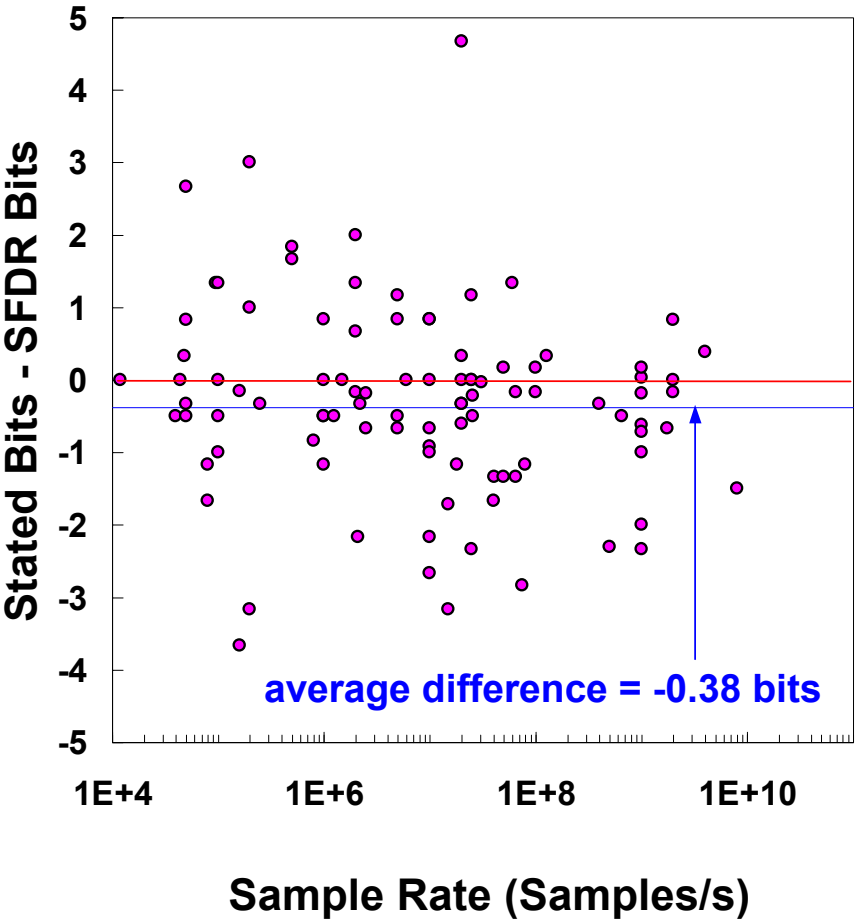
Stated Resolution Contrasted with SNR and SFDR





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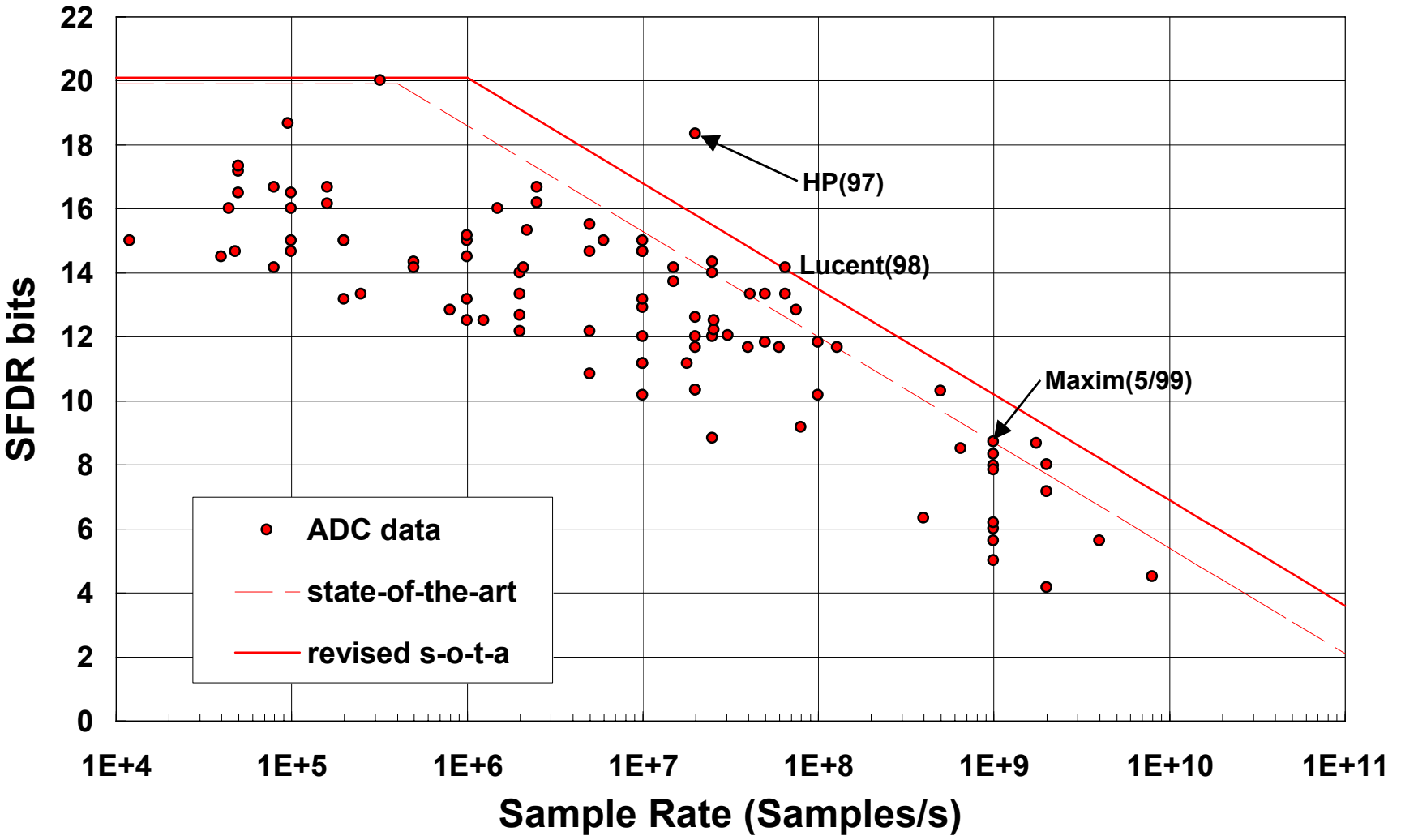
Spurious-Free Dynamic Range Data
SFDR-bits = SFDR(dBc) / 6.02



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ADC Performance Limitations: Circuit Noise

Equivalent input-referred thermal noise

- $\langle v_n^2 \rangle = 4kTR_{eff}f_{samp}/2$
- R_{eff} includes contributions due to thermal noise, shot noise, flicker noise, and input-referred noise terms
- thermal noise contribution includes the signal source resistance
- maximum resolution (+/- .5 LSB)

$$B_{max} = \log_2\left(\frac{V_{pp}^{\,2}}{6kTR_{eff}f_{samp}}\right)^{1/2} - 1$$

- in this presentation, V_{pp} = 1 V

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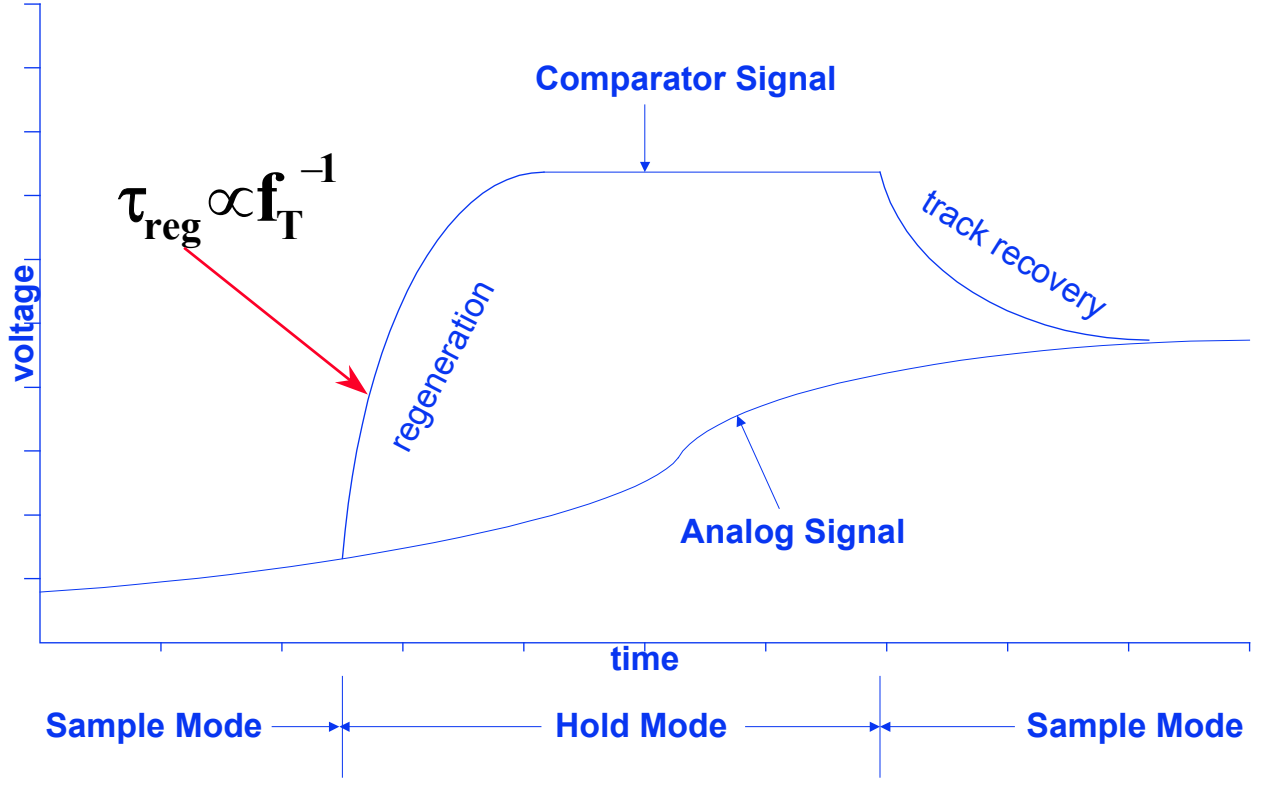
ADC Performance Limitations: Comparator Ambiguity



$$B_{ambiguity} = \frac{\pi f_T}{6.9 f_{samp}} - 1.1$$

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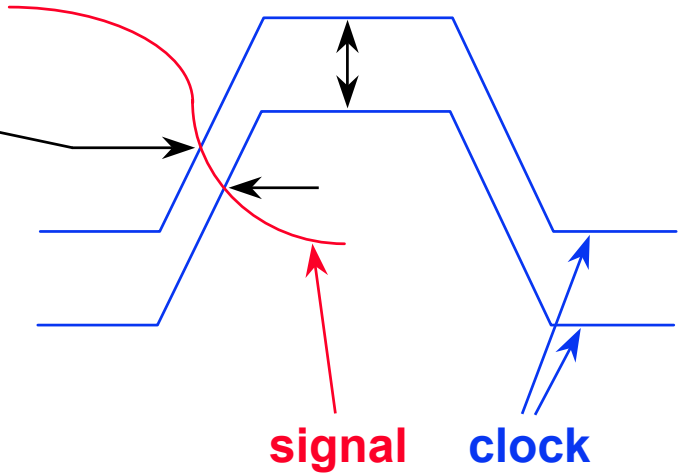
ADC Performance Limitations: Aperture Uncertainty

Aperture jitter τ_a

- uncertainty in sampling time
- varies from sample-to-sample
- broadband noise on sampling clock
  - circuit noise
  - power-line noise
  - digital feedthrough noise
- phase noise on sampling clock
- phase noise on input signal
- system problem: on-chip & off-chip noise sources (having a clean, stable clock may not be enough)
- maximum resolution (+/- .5 LSB):



$$B_{aperture} = \log_2\left(\frac{2}{\sqrt{3}\,\pi f_{samp}\,\tau_a}\right) - 1$$

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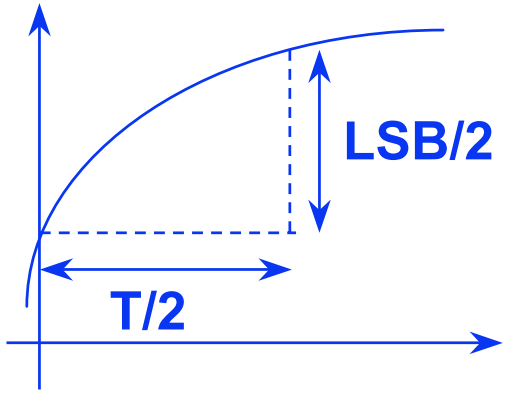
ADC Performance Limitations: Heisenberg Uncertainty Principal



$$\Delta E = \frac{\left(\frac{LSB}{2}\right)^2}{R}\frac{T}{2}, \quad \Delta t = \frac{T}{2}$$

$$\Delta E \cdot \Delta t = \frac{1}{R}\left(\frac{LSB \cdot T}{4}\right)^2 \geq \hbar$$

$$f_{samp} = \frac{1}{T}$$

$$LSB = V_{FS} 2^{-N}$$

$$V_{FS} = 1\,V$$

$$R = 50\Omega$$

$$\sqrt{\hbar R} = 7.26 \cdot 10^{-17}$$

$$2^N \cdot f_{samp} \leq \frac{V_{FS}/2}{\sqrt{\hbar R}} = 3.44 \cdot 10^{15}$$

$$e.g., 12\ bits\ @\ 840\ GSPS$$

$$\tau_{a,H} = \frac{1}{\pi \cdot 2^N \cdot f_{samp}} = .093\ fs$$

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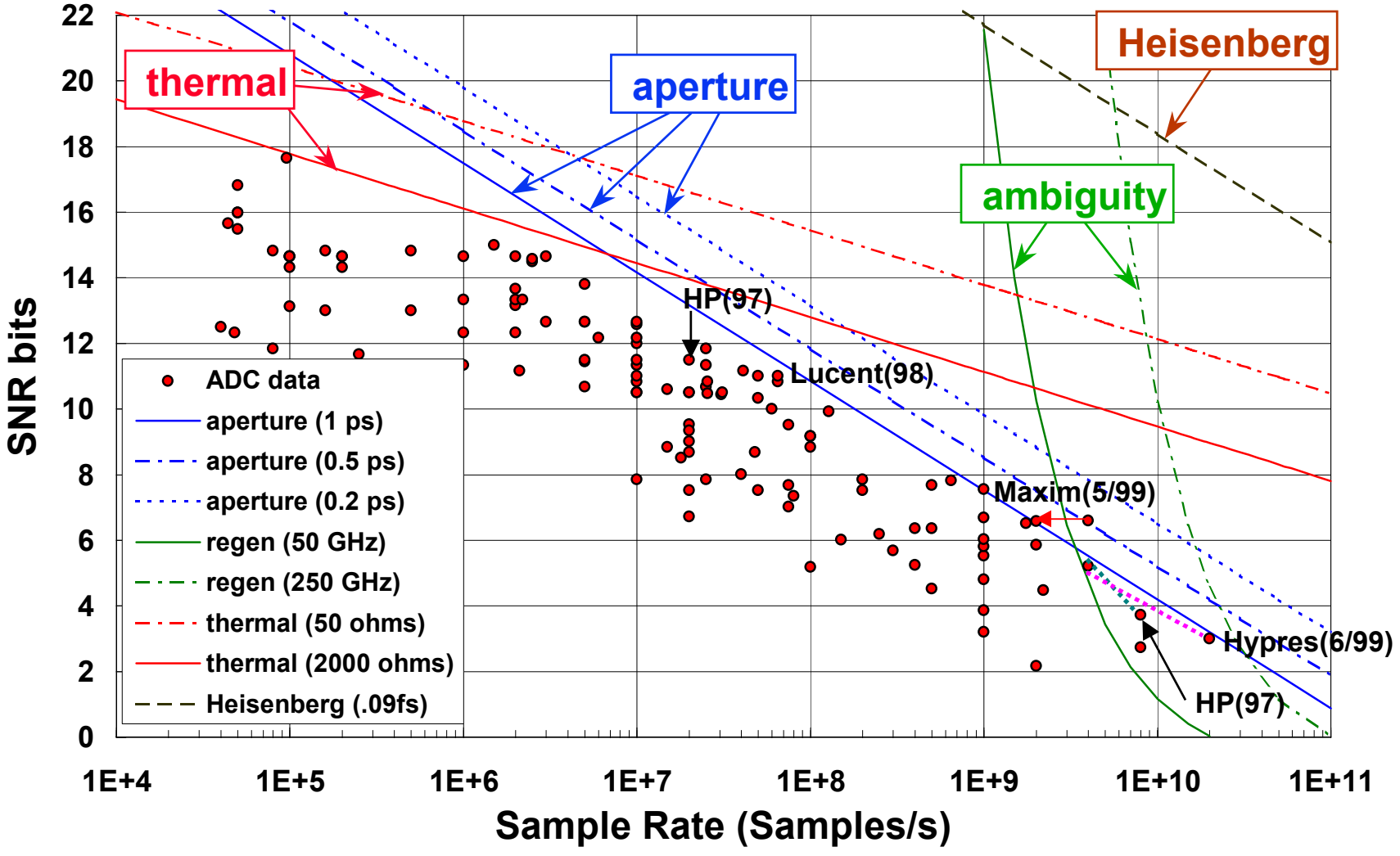
ADC Performance Limitations (updated 7/16/99)

Basis: Signal-to-Noise Ratio



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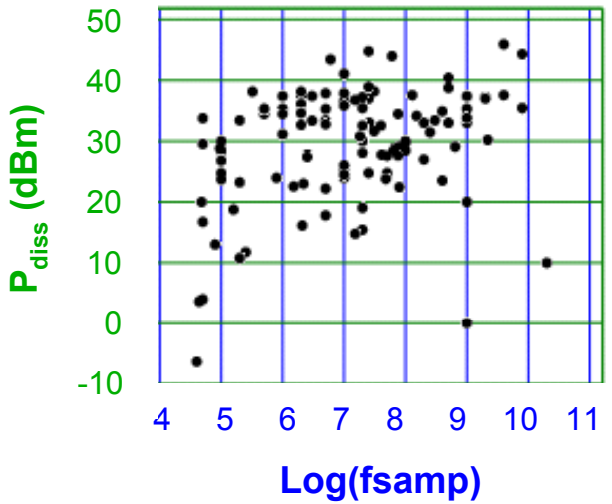
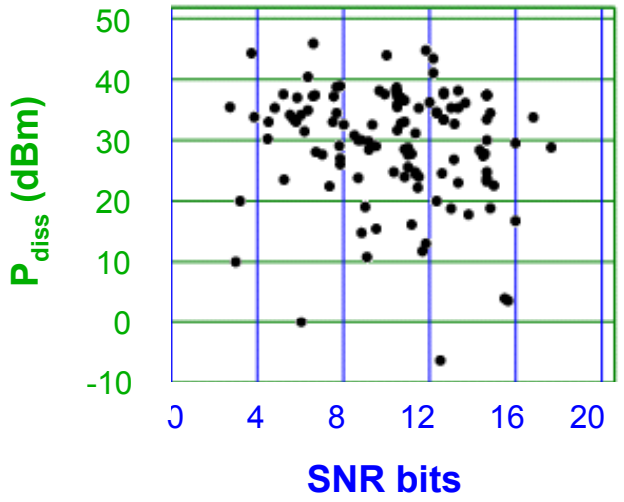
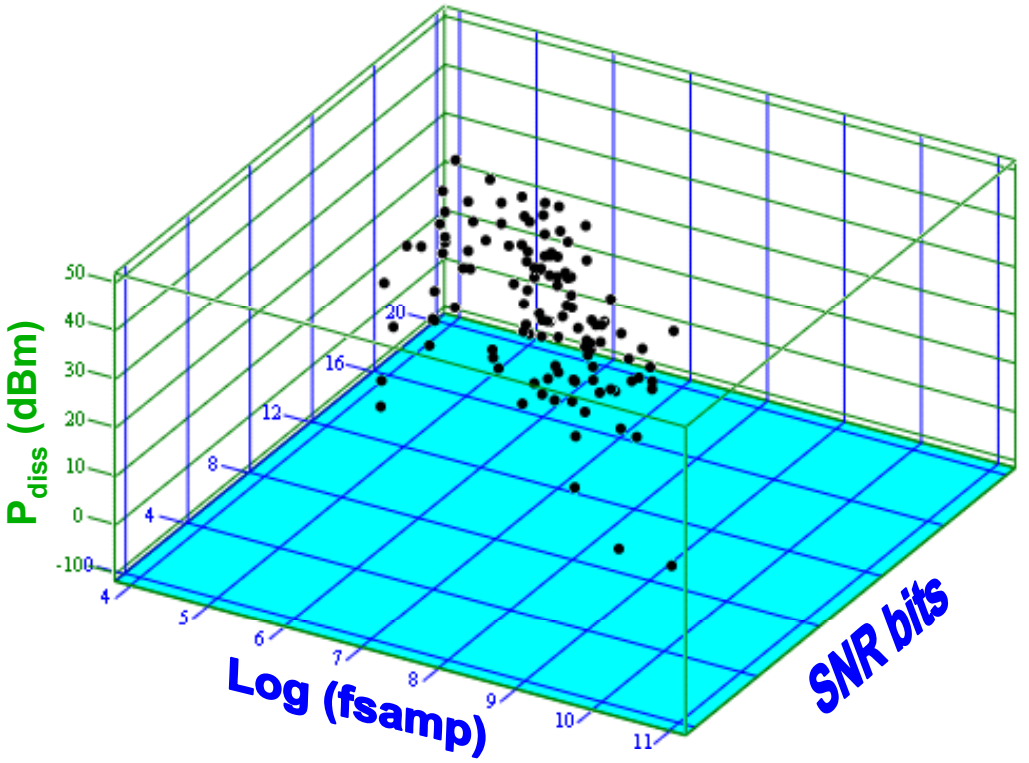
ADC Power Dissipation

Power consumption varies by roughly six orders of magnitude.







Average ~ 30 dBm

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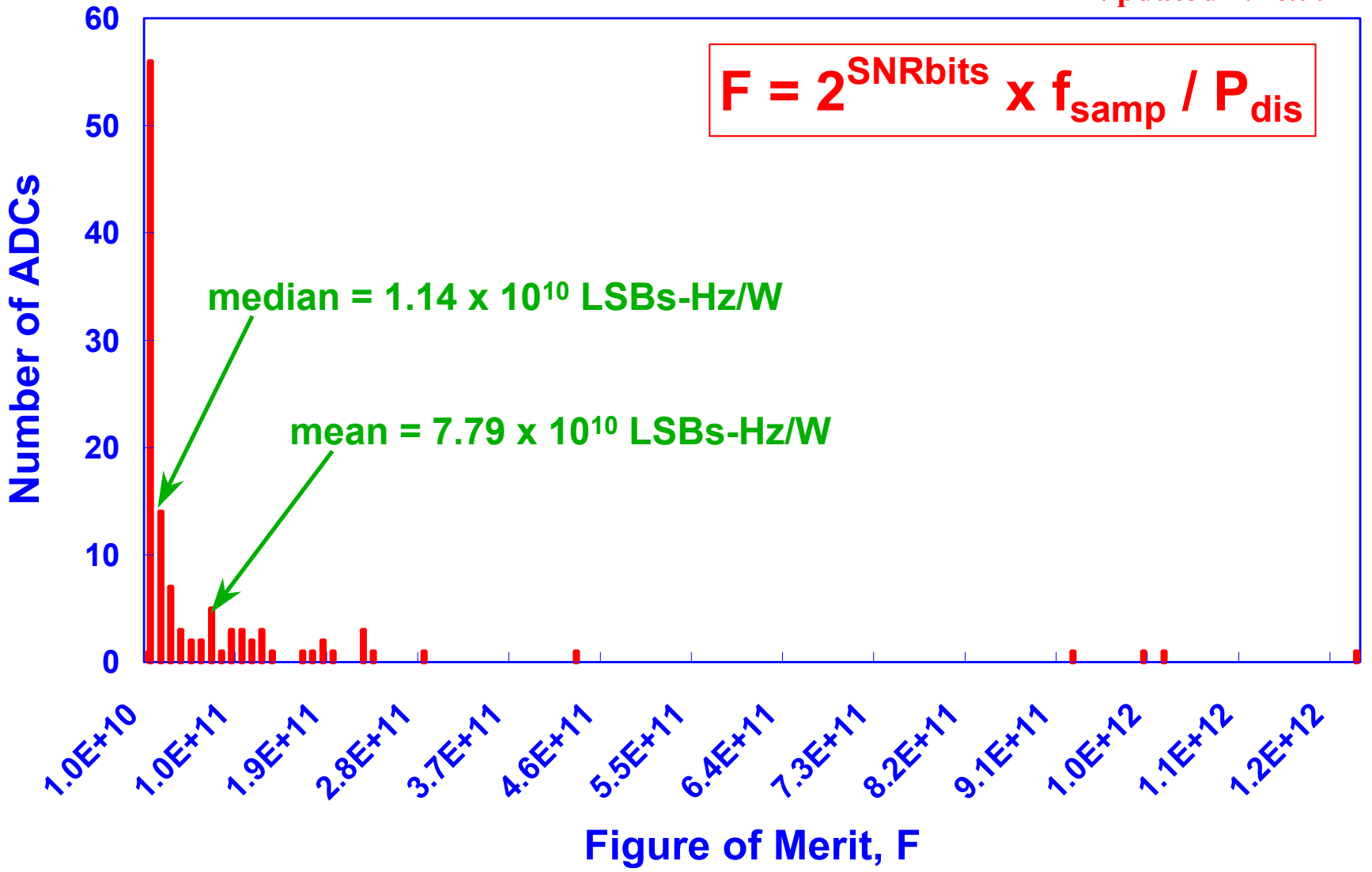
ADC Figure of Merit - 1

updated 7/16/99



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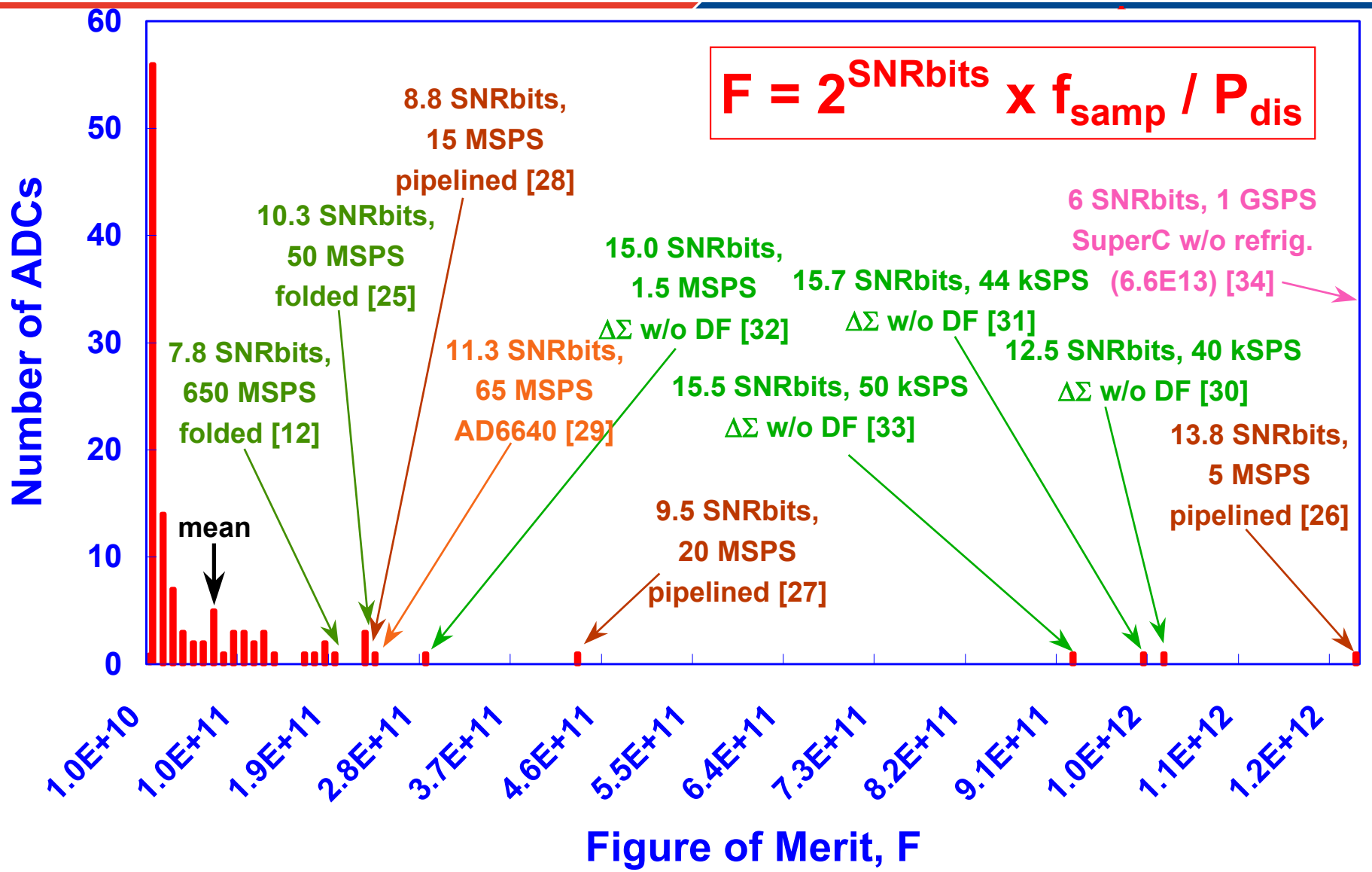
ADC Figure of Merit - 2



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High Performance ADCs

High Figure of Merit:

- 13.8 SNRbits, 5.0 MSPS; 4-stage, calibrating; Kwak et al., et al., '97
- 12.5 SNRbits, 40 kSPS; $\Delta\Sigma$, OSR = 250; Chen & Leung, '97
- 9.5 SNRbits, 20 MSPS; pipelined, digital correction; Cho & Gray, '95
- 8.8 SNRbits, 15 MSPS; pipelined, interpolating; Kusumoto et al., '93
- 10.3 SNRbits, 50 MSPS; folded flash , interpolating; Vorenkamp et al., '97

State-of the Art Performances ($P = 2^{SNRbits} \times f_{samp}$):

- 6.6 SNRbits, 4.0 GSPS; time interleaved, 40W; Schiller & Byrne, '91
- 6.6 SNRbits, 2.0 GSPS; folded flash; Nary et al., '95
- 7.5 SNRbits, 1.0 GSPS; flash; Maxim Max104, '99
- 6.5 SNRbits, 1.8 GSPS; flash; Wong et al., '96
- 3.0 SNRbits, 20.0 GSPS; superconducting folded-flash; Hypres, '99

High Spur-Free Dynamic Range

- 18.3 SFDRbits, 20 MSPS; dithered, HP E1437A, '97
- 14.2 SFDRbits, 65 MSPS; dithered, Lucent CSP1152A, '98

Flexible:

- 60 MHz IF, 4 GHz clock, 2nd order bandpass $\Delta\Sigma$, Raghavan, et al., '97
  - 7.0 SNR bits @ 63 MHz bw
  - 14.9 SNR bits @ 366 kHz bw

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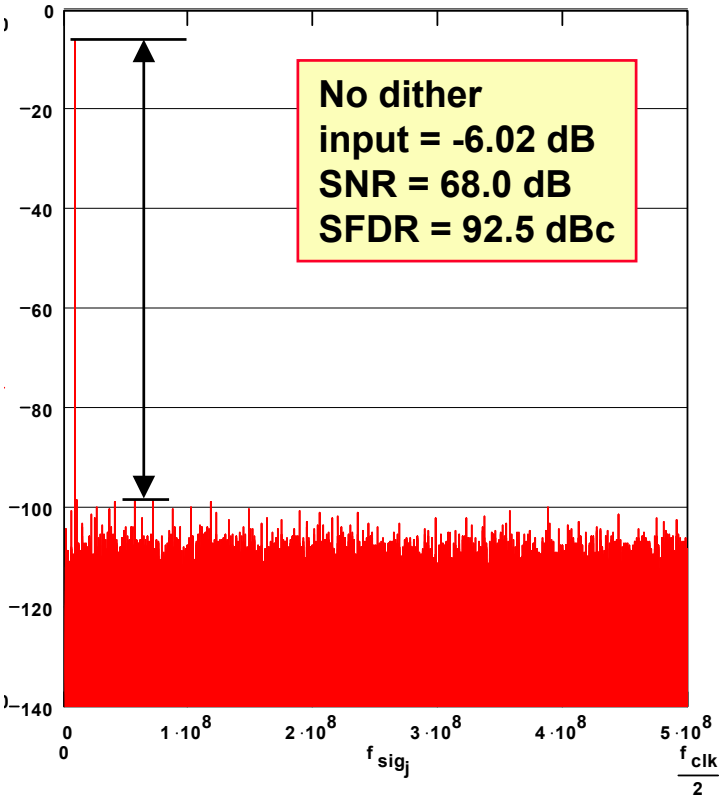
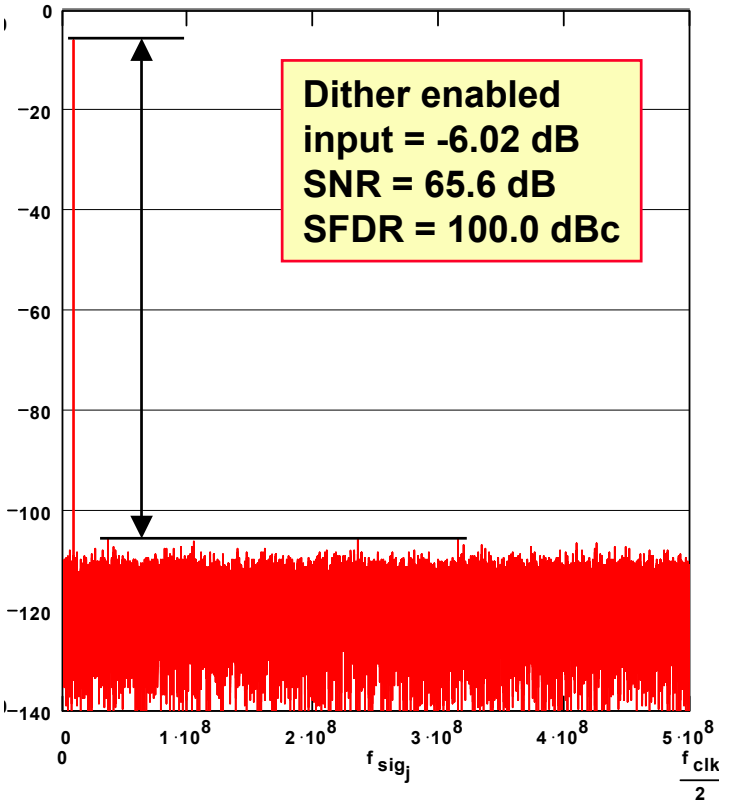
High Performance ADC Architectures
dithering improves SFDR

Example: introduce dithering by addition of pseudorandom noise to an ideal 11-bit ADC

- SFDR increases
- SNR decreases
- optimum PRN level ~ 1/2 LSB





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High Performance ADC Architectures
moderate sample-rate, high resolution

Delta sigma ($\Delta\Sigma$): a combination of oversampling and feedback leads to suppression of quantization noise at low-frequency end of spectrum.

- analog front-end contains a small number of low-precision components
- digital back-end contains most of the complexity
- most popular configuration is a cascade of first and/or second order modulators
- requires ultra high speed IC technology for RF applications
- bandpass modulators add new dimensions
  - tunable center frequency
  - tunable bandwidth
  - reduce number of downconversions
  - bandpass digital filtering replaces analog filtering functions (better blocking of interferers)

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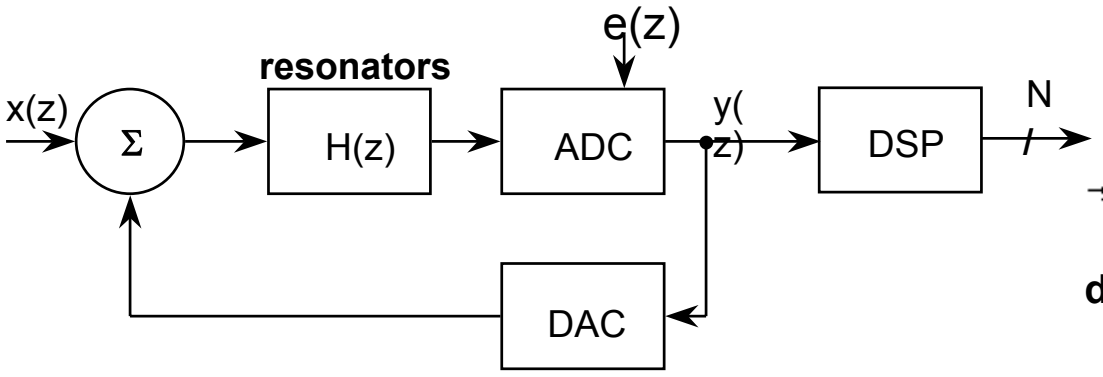
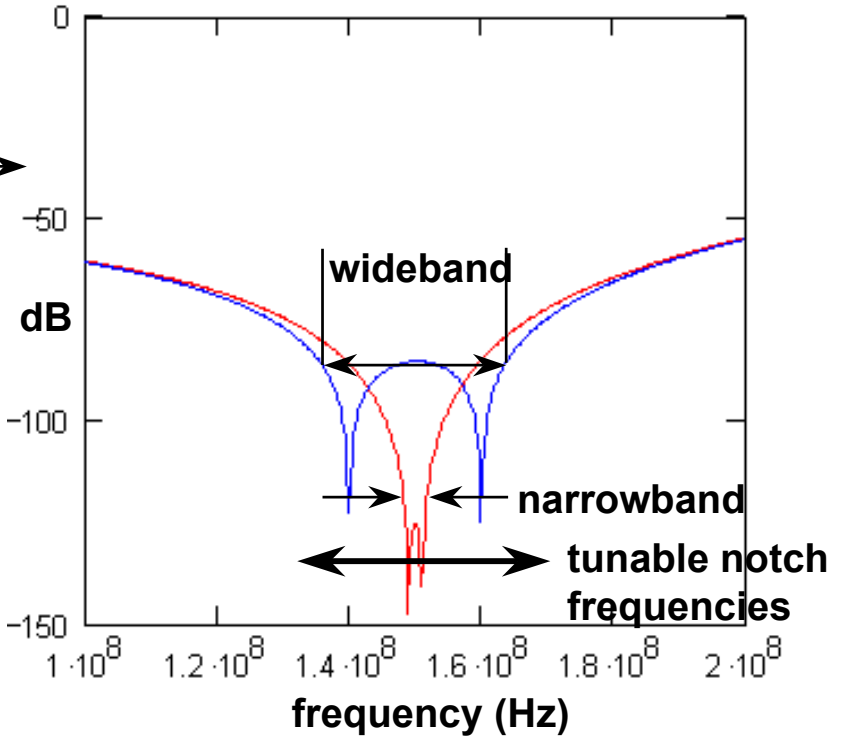
Bandpass Delta Sigma Converters



$$y(z) = \{z^{-1}H(z)x(z) + e(z)\} / \{1 + z^{-1}H(z)\}$$



- Resonators determine modulator frequency response and are tunable
- Sample rate of modulator is sample rate of the quantizer (ADC)
- DSP is a complex digital circuit and performs bandpass filtering and downconversion
- Sample (Nyquist) rate of ADC is set by DSP
- Number, N, of output leads limits ADC resolution

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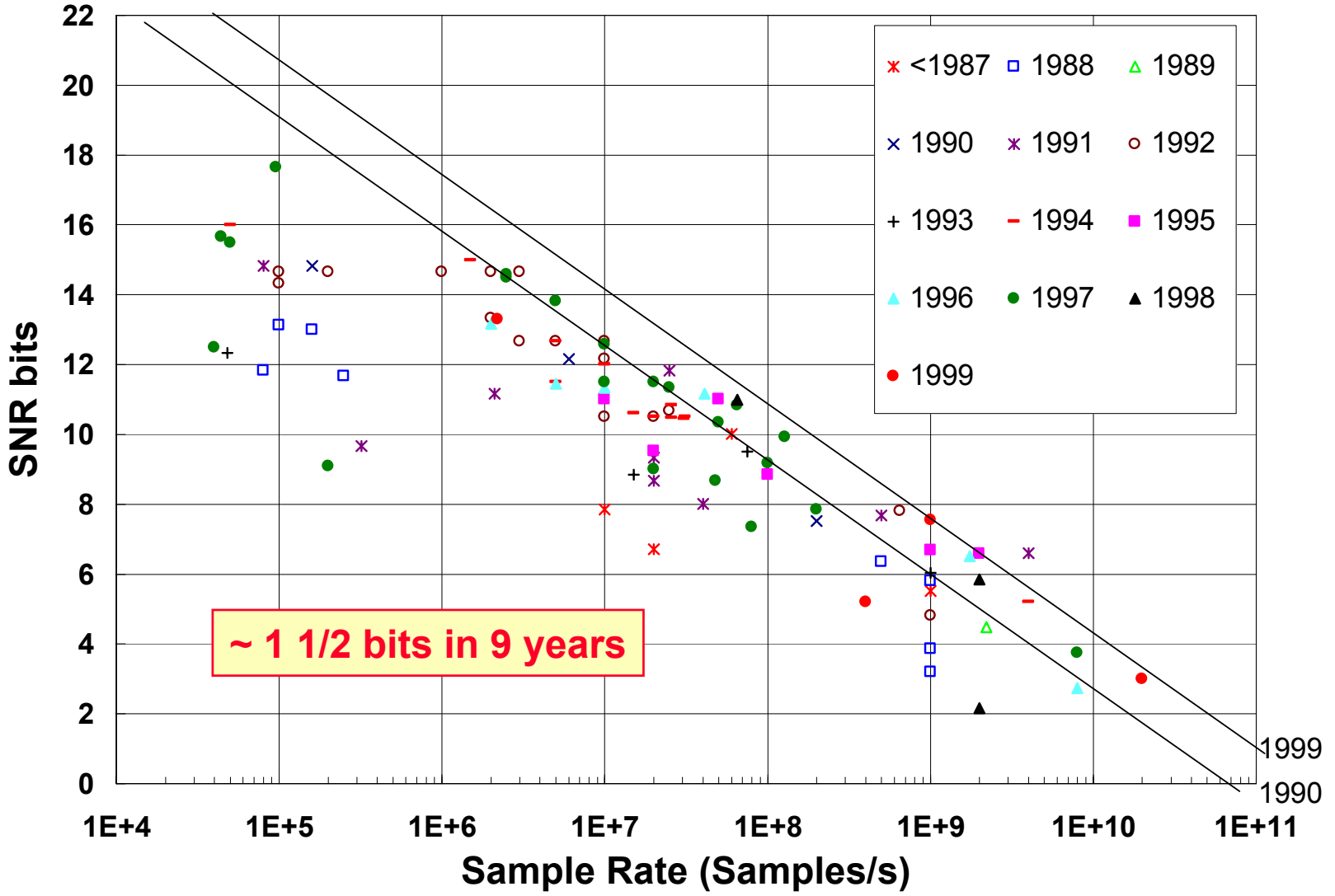
Progress in Performance Improvement Over Time: SNR



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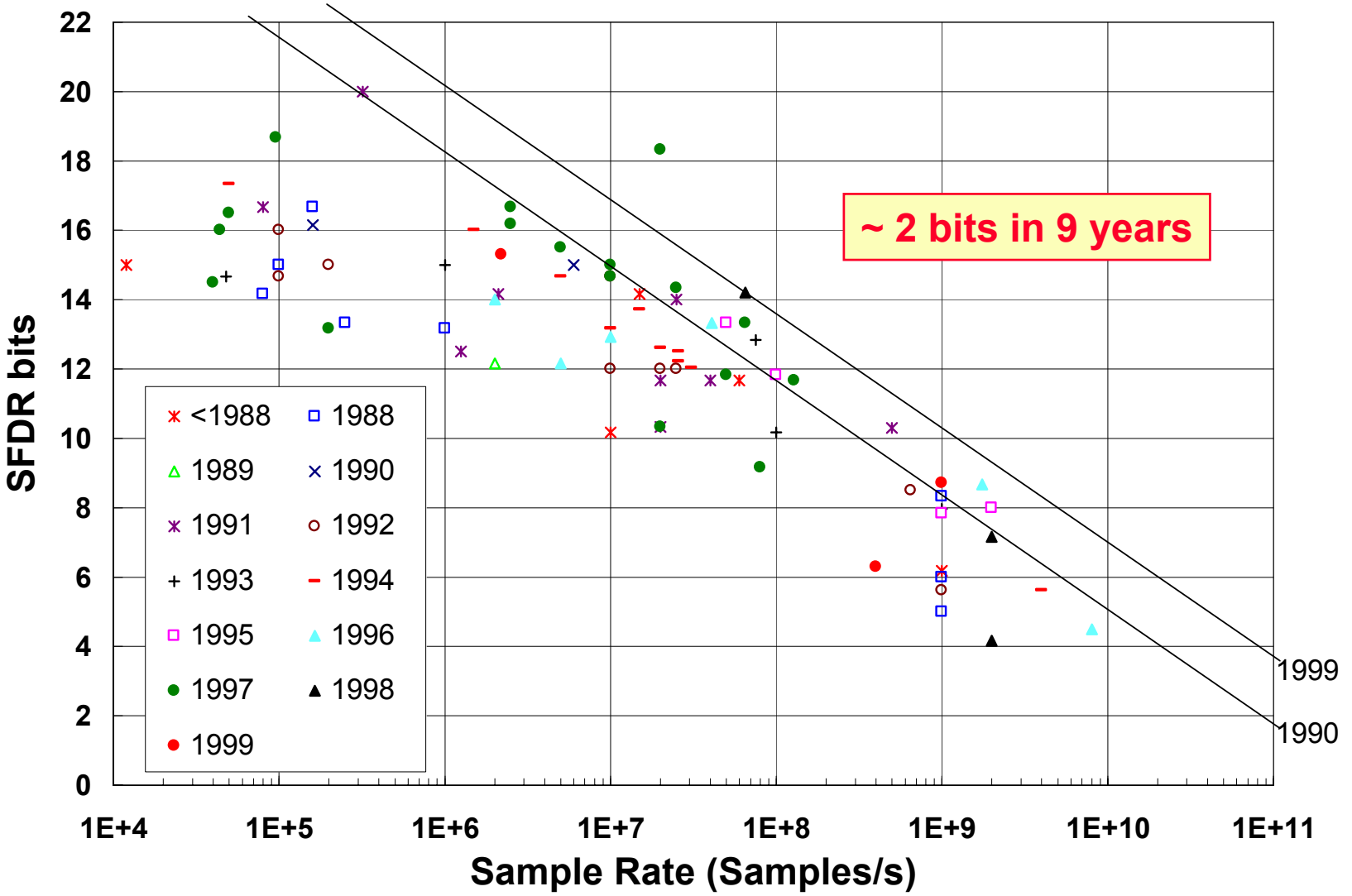
Progress in Performance Improvement Over Time: SFDR



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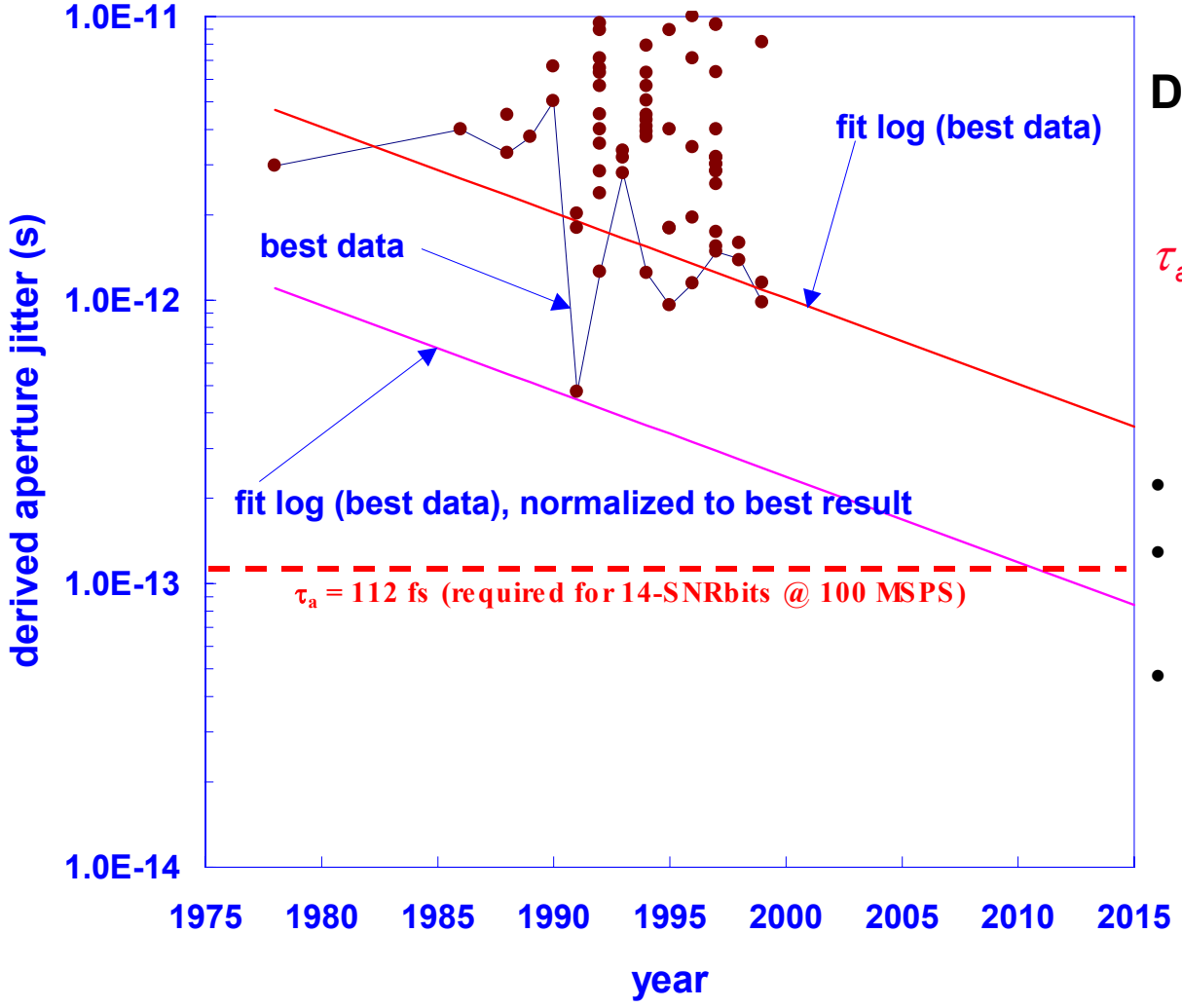
ADC Performance Trend using Derived Aperture Jitter



Derive τ_a values from SNR data:

$$\tau_a = \frac{1}{\sqrt{3} \cdot \pi \cdot P} = \frac{2^{-SNRbits}}{\sqrt{3} \cdot \pi \cdot f_{samp}}$$

- current best ~ 0.5 ps
- trend shows very gradual improvement
- actual progress is sporadic

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ADC Technology Comparison Conclusions

- ADC Survey
  - Over 170 converters: experimental and commercial
  - SNR bits: ranged from 0 to 3.5 bits below stated resolution
  - SFDR bits: ranged from 4 bits below to 4.5 bits above stated resolution
  - Performance limitations: aperture uncertainty (?) (~ 1 ps), IC technology speed (~ 50 - 80 GHz)
  - Figure of merit: $F = 2^{(\text{SNR bits})} \times f_{samp} / P_{diss}$ (mean = 7.8×10^{10} LSBs-Hz/W)
- High performance architectures
  - Time interleaved
  - Folded, interpolating
  - Pipelined
  - Dithered (high SFDR)
  - Delta sigma (including bandpass)
- Relatively little improvement in ADC performance during recent years ($P = 2^{(\text{SNR bits})} \times f_{samp} < 4.096 \times 10^{11}$ LSBs - Hz)

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