

Comparing the High Speed Comparators

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Comparing the High Speed Comparators

INTRODUCTION

Several integrated circuit voltage comparators exist which were designed with high speed and complementary TTL outputs as the main objectives. The more common applications for these devices are high speed analog to digital (A to D) converters, tape and disk-file read channels, fast zero-crossing detectors, and high speed differential line receivers. This note compares the National Semiconductor devices to similar devices from other manufacturers.

The product philosophy at National was to create pin-for-pin replacement circuits that could be considered as second-sources to the other comparators, while simultaneously containing the improvements necessary to make a more op-

timum device for the intended usage. Optimized parameters include speed, input accuracy and impedance, supply voltage range, fanout, and reliability. The LM160/LM260/LM360 are replacement devices for the μ A760, while the LM161/LM261/LM361 replace the SE/NE529. Tables I and II compare the critical parameters of the National commercial range devices to their respective counterparts.

SPEED

Throughout the universe the subject of speed must be approached with caution; the same holds true here. Speed (propagation delay time) is a function of the measurement

TABLE I. LM360/ μ A760C Comparison $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $V^+ = +5.0\text{V}$, $V^- = -5.0\text{V}$

Parameter	LM360	μ A760C	Units
Input Offset Voltage	5.0	6.0	mV max
Input Offset Current	3.0	7.5	μ A max
Input Bias Current	20	60	μ A max
Input Capacitance	4.0	8.0	pF typ
Input Impedance	17	5.0	k Ω typ @ 1 MHz 25°C
Differential Voltage Range	± 5.0	± 5.0	V typ
Common Mode Voltage Range	± 4.0	± 4.0	V typ
Gain	3.0	3.0	V/mV typ 25°
Fanout	4.0	2.0	74 Series TTL Loads
Propagation Delays:			
(1) 30 mVp-p 10 MHz Sinewave in	25	30	ns max 25°
(2) 2.0 Vp-p 10 MHz Sinewave in	20	25	ns max 25°
(3) 100 mV Step + 5.0 mV Overdrive	14	22	ns typ 25°

TABLE II. LM261/NE529 Comparison $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $V^+ = +10\text{V}$, $V^- = -10\text{V}$, $V_{CC} = +5.0\text{V}$

Parameter	LM261	NE529	Units
Input Offset Voltage	3.0	10	mV max
Input Offset Current	3.0	15	μ A max
Input Bias Current	20	50	μ A max
Input Impedance	17	5.0	k Ω typ @ 1 MHz 25°C
Differential Voltage Range	± 5.0	± 5.0	V typ
Common Mode Voltage Range	± 6.0	± 6.0	V typ
Gain	3.0	4.0	V/mV typ 25°
Fanout	4.0	6.0	74 Series TTL Loads
Propagation Delay - 50 mV Overdrive	20	22	ns max 25°

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technique. The earlier "standard" of using a 100 mV input step with 5.0 mV overdrive has given way to seemingly endless variations. To be meaningful, speed comparisons must be made with identical conditions. It is for this reason that the speed conditions specified for the National parts are the same as those of the parts replaced.

Probably the most impressive speed characteristic of the six National parts is the fact that propagation delay is essentially independent of input overdrive (Figure 1); a highly desir-

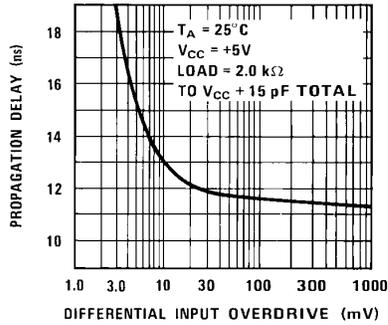


FIGURE 1. Delay vs Overdrive

able characteristic in A to D applications. Their delay typically varies only 3 ns for overdrive variations of 5.0 mV to 500 mV, whereas the other parts have a corresponding delay variation of two to one. As can be seen in Tables I and II, the National parts have an improved maximum delay specification. Further, the 20 ns maximum delay is meaningful since it is specified with a representative load: a 2.0 kΩ resistor to +5.0V and 15 pF total load capacitance. Figure 2 shows typical delay variation with temperature.

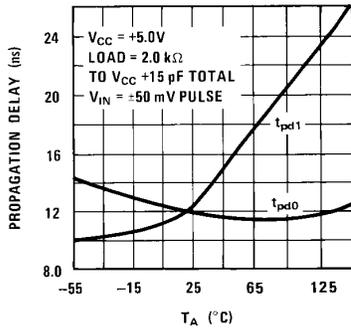


FIGURE 2. Delay vs Temperature

INPUT PARAMETERS

The A to D, level detector, and line receiver applications of these devices require good input accuracy and impedance. In all these cases the differential input voltage is relatively

large, resulting in a complete switch of input bias current as the input signal traverses the reference voltage level. This effect can give rise to reduced gain and threshold inaccuracy, dependent on input source impedances and comparator input bias currents. Tables I and II show that the National parts have a substantially lower maximum bias current to ease this problem. This was done without resorting to Darlington input stages whose price is higher offset voltages and longer delay times. The lower bias currents also raise input resistance in the threshold region. Lower input capacitance and higher input resistance result in higher input impedance at high frequencies.

Even with low source impedances, input accuracy is still dependent on offset voltage. Since none of the devices under discussion has internal offset null capability, ultimate accuracy was improved by designing and specifying lower maximum offset voltage. Refer to Figure 3 for typical offset voltage drift with temperature.

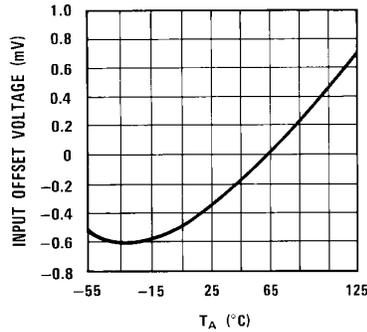


FIGURE 3. Offset Temperature Coefficient

OTHER PERFORMANCE AREAS

In the case of the LM160/LM260/LM360, fanout was doubled over the previous device. For the LM161/LM261/LM361, operating supply voltage range was extended to

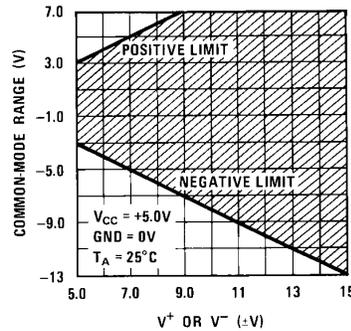


FIGURE 4. LM161 Common Mode Range

±15V op amp supplies which are often readily available where such a comparator is used. Figure 4 reveals the common mode range of the latter device.

The performance improvements previously mentioned were a result of circuit design (Figures 5 and 6) and device processing. Schottky clamping, which can give rise to reliability problems, was not used. Gold doping, which results in processing dependent speeds and low transistor beta, was not used. Instead a non-gold-doped process with high breakdown voltage, high beta, and high f_T (≈ 1.5 GHz) was se-

lected which produced remarkably consistent performance independent of normal process variation. The higher breakdown voltage allows the LM161/LM261/LM361 to operate on $\pm 15V$ supplies and results in lower transistor capacitance; higher beta provides lower input bias currents; and higher f_T helps reduce propagation time.

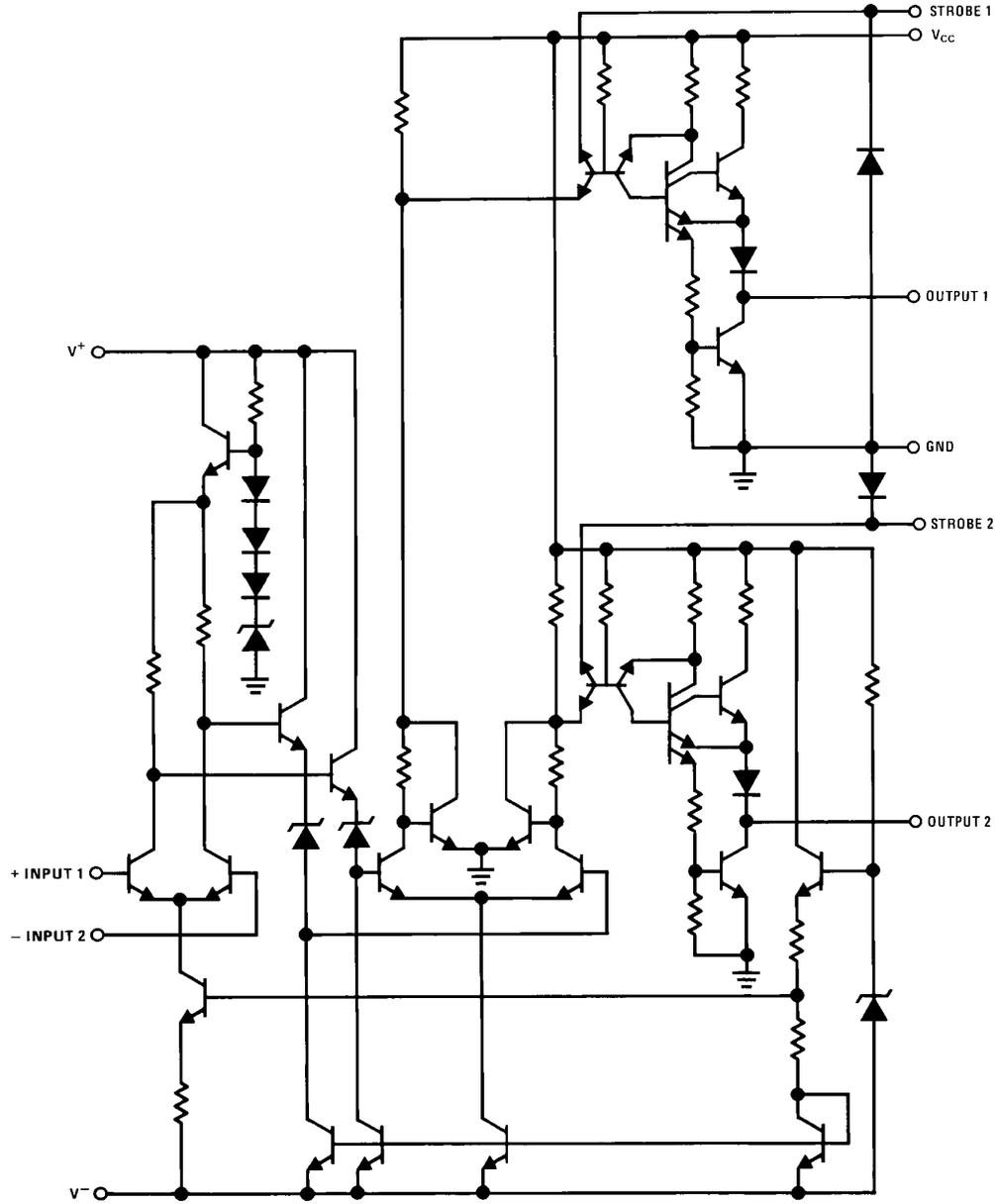


FIGURE 5. LM161 Schematic Diagram

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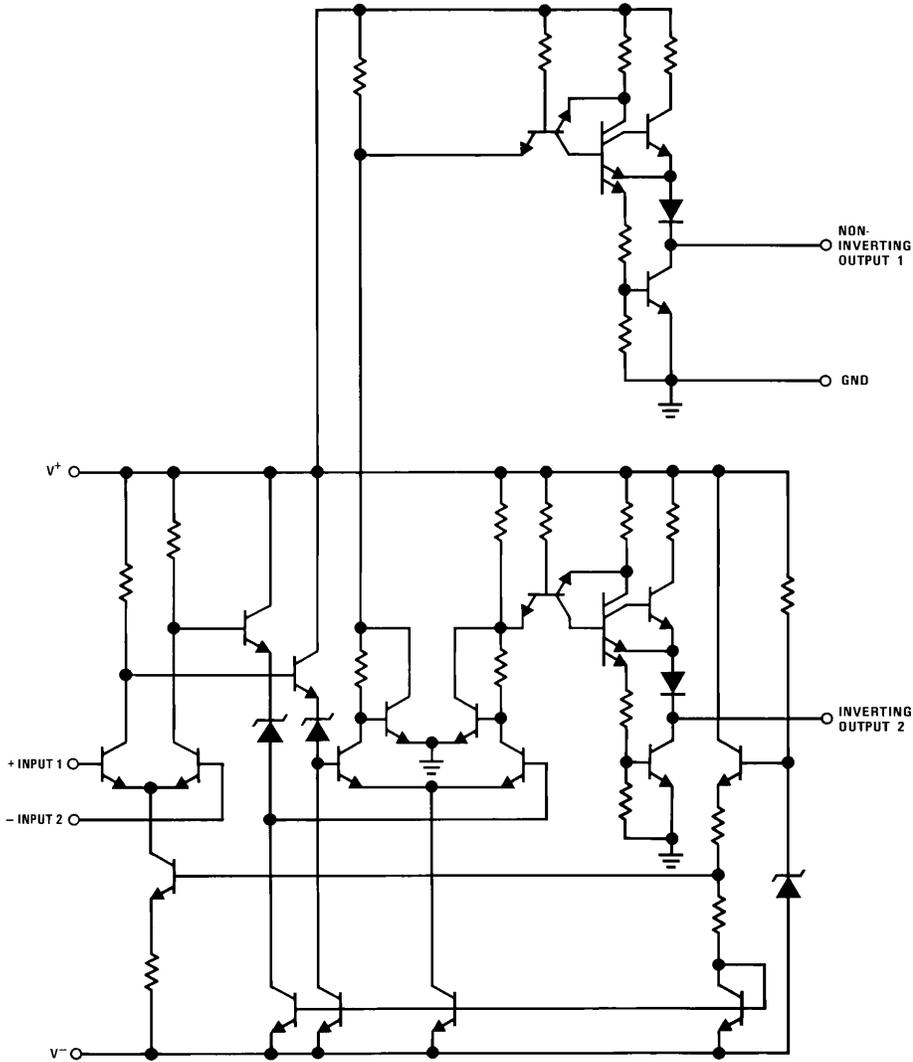


FIGURE 6. LM160 Schematic Diagram

TL/H/7407-6

APPLICATIONS

Typical applications have been mentioned previously. The LM160 and LM161 may be combined as in *Figure 7* to create a fast, accurate peak detector for use in tape and disk-file read channels. A 3-bit A to D converter with 21 ns typical conversion time is shown in *Figure 8*. Although primarily in-

tended for interfacing to TTL logic, direct connection may be made to ECL logic from the LM161 by the technique shown in *Figure 9*. When used this way the common mode range is shifted from that of the TTL configuration. Finally level detectors or line receivers may be implemented with hysteresis in the transfer characteristic as seen in *Figure 10*.

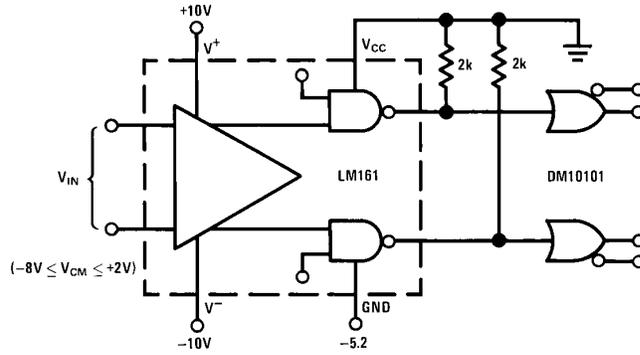


FIGURE 9. Direct Interfacing to ECL

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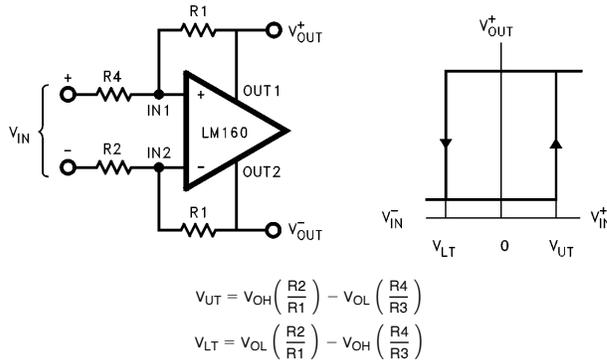


FIGURE 10. Level Detector with Hysteresis

TL/H/7407-10

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