

CD4042BM/CD4042BC Quad Clocked D Latch

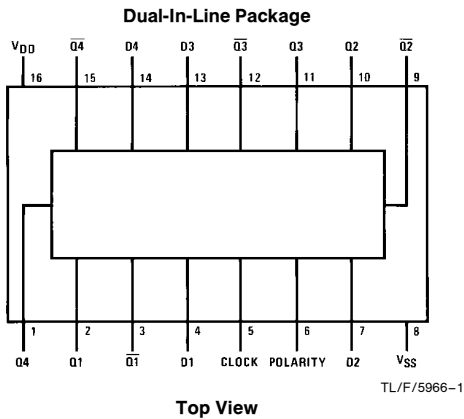
General Description

The CD4042BM/CD4042BC quad clocked "D" latch is a monolithic complementary MOS (CMOS) integrated circuit constructed with P- and N-channel enhancement mode transistors. The outputs Q and \bar{Q} either latch or follow the data input depending on the clock level which is programmed by the polarity input. For polarity = 0; the information present at the data input is transferred to Q and \bar{Q} during 0 clock level; and for polarity = 1, the transfer occurs during the 1 clock level. When a clock transition occurs (positive for polarity = 0 and negative for polarity = 1), the information present at the input during the clock transition is retained at the outputs until an opposite clock transition occurs.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility Fan out of 2 driving 74L or 1 driving 74LS
- Clock polarity control
- Fully buffered data inputs
- Q and \bar{Q} outputs

Connection Diagram

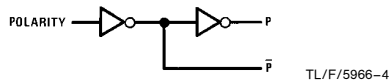
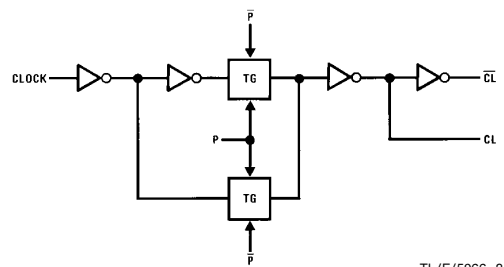
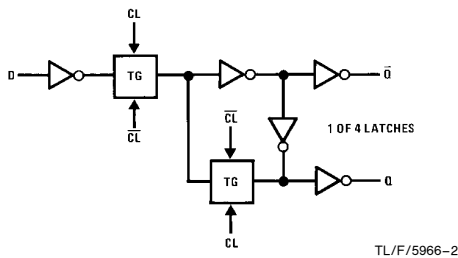


Truth Table

Clock	Polarity	Q
0	0	D
1	0	Latch
1	1	D
1	1	Latch

Order Number CD4042B

Logic Diagrams



Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	-0.5V to +18V
Input Voltage (V_{IN})	-0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4042BM	-55°C to +125°C
CD4042BC	-40°C to +85°C

DC Electrical Characteristics CD4042BM (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		1		0.02	1		30	μA
		$V_{DD} = 10V$		2		0.02	2		60	μA
		$V_{DD} = 15V$		4		0.02	4		120	μA
V_{OL}	Low Level Output Voltage	$ I_O < 1 \mu A, V_{IH} = V_{DD}, V_{IL} = 0V$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$ I_O < 1 \mu A, V_{IH} = V_{DD}, V_{IL} = 0V$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
V_{IL}	Low Level Input Voltage	$ I_O < 1 \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or 9V		3.0		4.5	3.0		3.0	V
V_{IH}	High Level Input Voltage	$ I_O < 1 \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0	5.5		7.0		V
I_{OL}	Low Level Output Current (Note 4)	$V_{IH} = V_{DD}, V_{IL} = 0V$								
		$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
I_{OH}	High Level Output Current (Note 4)	$V_{IH} = V_{DD}, V_{IL} = 0V$								
		$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4042BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5V		4		0.02	4		30	μA
		V _{DD} = 10V		8		0.02	8		60	μA
		V _{DD} = 15V		16		0.02	16		120	μA
V _{OL}	Low Level Output Voltage	I _O < 1 μA, V _{IH} = V _{DD} , V _{IL} = 0V								
		V _{DD} = 5V		0.05		0	0.05		0.05	V
		V _{DD} = 10V		0.05		0	0.05		0.05	V
		V _{DD} = 15V		0.05		0	0.05		0.05	V
V _{OH}	High Level Output Voltage	I _O < 1 μA, V _{IH} = V _{DD} , V _{IL} = 0V								
		V _{DD} = 5V	4.95		4.95	5		4.95		V
		V _{DD} = 10V	9.95		9.95	10		9.95		V
		V _{DD} = 15V	14.95		14.95	15		14.95		V
V _{IL}	Low Level Input Voltage	I _O < 1 μA								
		V _{DD} = 5V, V _O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V _{DD} = 10V, V _O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V _{DD} = 15V, V _O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V _{IH}	High Level Input Voltage	I _O < 1 μA								
		V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V _{DD} = 10V, V _O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I _{OL}	Low Level Output Current (Note 4)	V _{IH} = V _{DD} , V _{IL} = 0V								
		V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
		V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
		V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA
I _{OH}	High Level Output Current (Note 4)	V _{IH} = V _{DD} , V _{IL} = 0V								
		V _{DD} = 5V, V _O = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
		V _{DD} = 10V, V _O = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
		V _{DD} = 15V, V _O = 13.5V	-3.6		-3.0	-8.8		-2.4		mA
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V		-0.3		-10 ⁻⁵	-0.3		-1.0	μA
		V _{DD} = 15V, V _{IN} = 15V		0.3		10 ⁻⁵	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}$, Input $t_r = t_f = 20\text{ ns}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} , t_{PLH}	Propagation Delay Time Data In to Q	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		175 75 60	350 150 120	ns ns ns
t_{PHL} , t_{PLH}	Propagation Delay Time Data In to \bar{Q}	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		150 75 50	300 150 100	ns ns ns
t_{PHL} , t_{PLH}	Propagation Delay Time Clock to Q	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		250 100 80	500 200 160	ns ns ns
t_{PHL} , t_{PLH}	Propagation Delay Time Clock to \bar{Q}	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		250 115 90	500 230 180	ns ns ns
t_H	Minimum Hold Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		60 30 25	120 60 50	ns ns ns
t_{SU}	Minimum Setup Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		0 0 0	50 30 25	ns ns ns
t_W	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 30	200 100 60	ns ns ns
t_{THL} , t_{TLH}	Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		125 60 50	250 125 100	ns ns ns
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

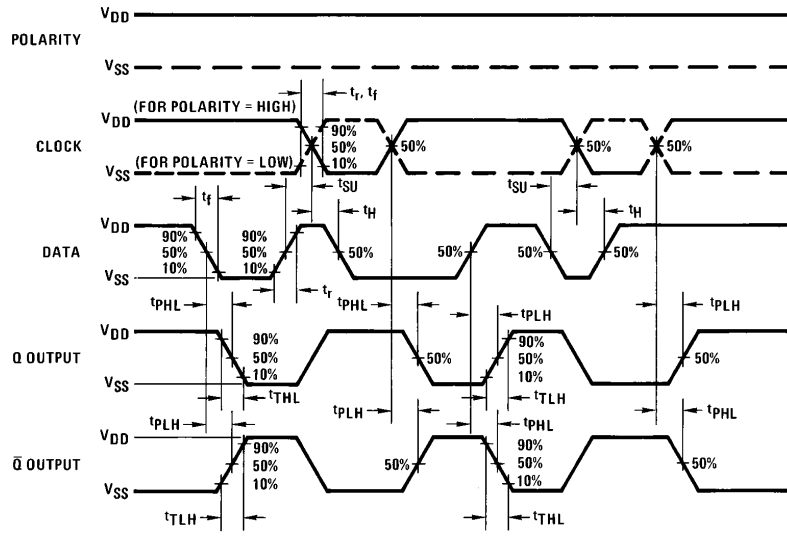
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0\text{V}$ unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

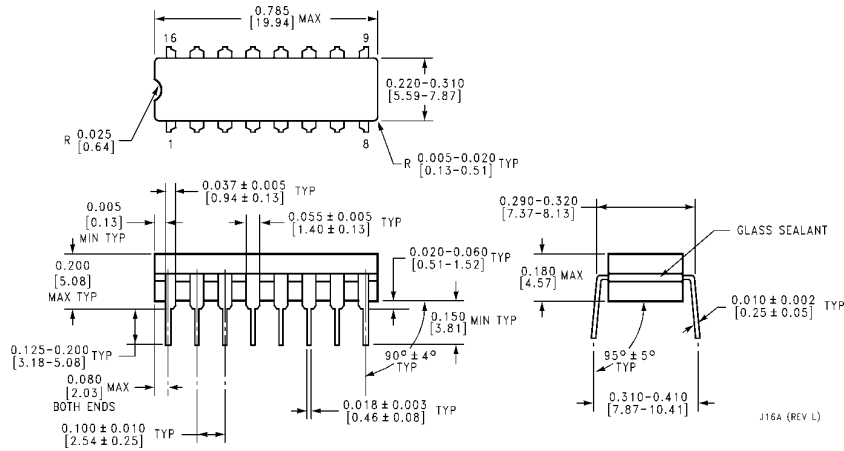
Note 4: I_{OH} and I_{OL} are tested one output at a time.

Switching Time Waveforms

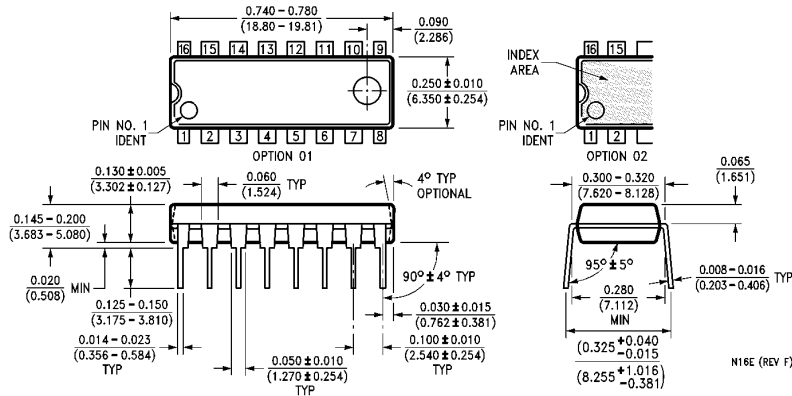


TL/F/5966-5

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4042BMJ or CD4042BCJ
NS Package Number J16A



Molded Dual-In-Line Package (N)
Order Number CD4042BMN or CD4042BCN
NS Package Number N16E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.