

High Speed Data Line Protection

Low current Bridges Rectifiers Lend Themselves to Data Line Protection

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Local Area Network (LAN) data lines require protection against direct and induced transient over voltages on the lines. Protecting these lines and the associated network is not a trivial task. The power range is somewhere between static discharge (very low power) and lightning protection which is at the other end of the spectrum (high power).

Power handling capability is only one aspect of the design. The designer must take care not to “load down” the line with a highly capacitive TVS or R/C network. As data rates go beyond 50 mb. It is not possible to use a TVS unit with capacitance above 100 pF to 200 pF. Most standard TVS devices have zero volt capacitance values greater than 500 pF. To make matters worse, the lower voltage TVS units have higher capacitance values than their higher voltage counterparts. Enter the steering diode bridge.

Vishay offers two surface mount bridge rectifiers. These components are ideal for use in protection circuits where power handling, capacitive loading and cost are all design considerations. These are the 1 A bridge (DF01S) the smaller 1/2 A (MB1S) SMD bridge rectifiers. Each diode within the 1 A part has a 0 V capacitance of 70 pF. The 1/2 bridge has a junction capacitance of about 25 pF. These components can be configured with TVS components (such as an SMBJ12) to form a high performance, low capacitance network capable of outstanding data line protection in LAN and other similar applications where data lines are exposed to transient surges beyond the scope of static discharge. Since each bridge contains four diodes each component can protect 2 independent lines.

Figure 1. shows the forward voltage drop of the 1 and 1/2 A bridge when configured as shown in figure 1. The surge can be applied in either polarity and to either input individually or simultaneously.

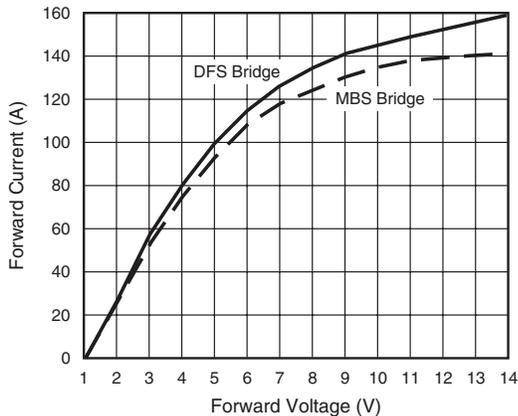


Figure 1. Forward Current vs. Forward Voltage

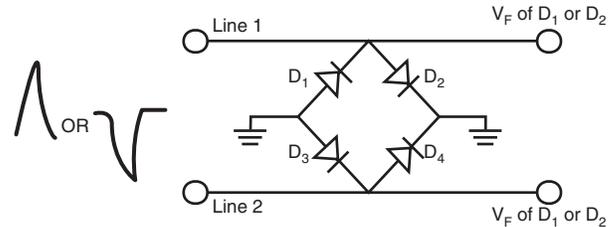


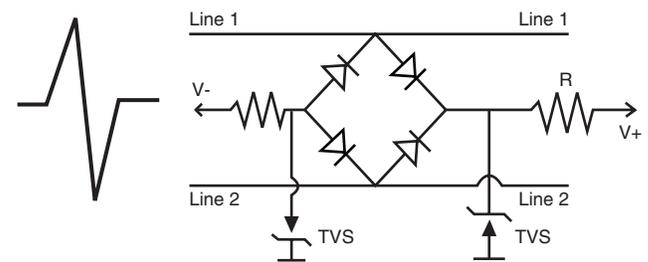
Figure 2.

These small components are capable of handling 120 (MBS) and 160 (DFS) A on the industry standard 10/1000 μ s current waveform. This is the same waveform that is used to test the axial and surface mount TVS components. For the MB1S the maximum V_F encountered at 120 A is 7 V hence, it is possible to use the 100 V version of either bridge in this application without fear of reliability issues caused by reverse breakdown of the diodes within the bridge during surge events.

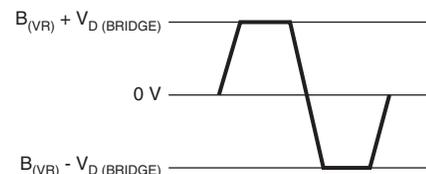
The different Steering diode/TVS configurations are illustrated in figure 3. through 7.

Figure 3. shows the classic symmetrical bidirectional protector. TVS units are utilized to provide clamping protection for both positive and negative going transients. The “turn on threshold” of the network is specified by the B_{VR} of the TVS unit selected plus the forward voltage drop of the rectifier diode junction within the bridge being utilized. Because the currents encountered can vary between below 1 A and higher than 100 A. The forward voltage drop of the bridge may vary between 0.6 V and 7 V.

Incoming Transient



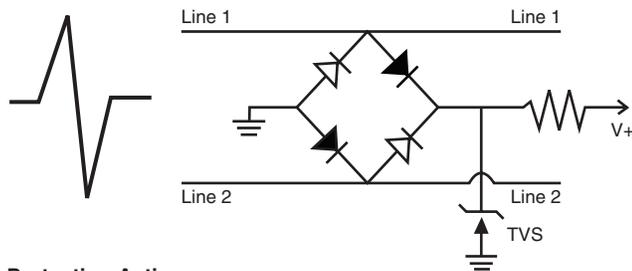
Protection Action



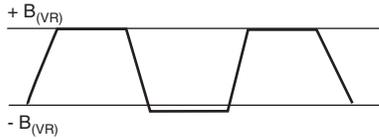
The Surge can be Applied to Either Line or Both
 $+B_{(VR)}$ and $-B_{(VR)}$ are Adjusted via TVS Parts Selection.

Figure 3.

Incoming Transient



Protection Action



The Clamping Voltage Becomes:

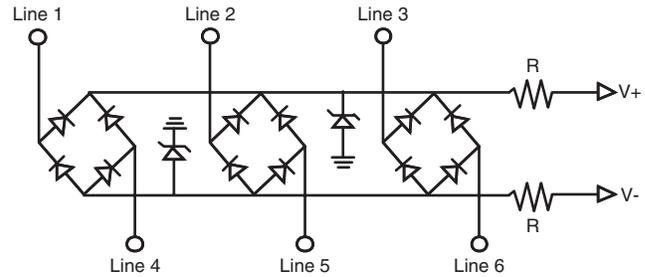
$$B_{(VR)} (TVS) + 2 V_F (BRIDGE) = V_C$$

Figure 4.

Figure 4. is a configuration designed to provide a-symmetrical bi-polar protection, that is, the diode drop of 1 V is observed for negative going transients and the B_{VR} of the selected TVS provides the turn on characteristic for a positive going surge. This is a common configuration when protecting the input stages of transceiver IC's that are powered by ground and B+ and no negative power rail is utilized. The configuration can be reversed to provide the same style of surge suppression with a negative power source.

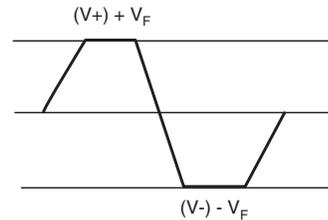
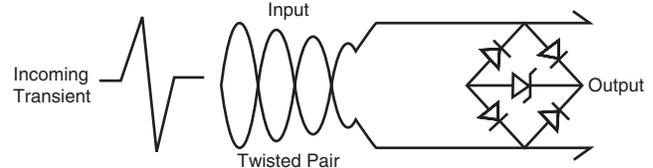
Both figure 3. and 4. have a resistor designated "R" going to either V+ or V-. These resistors can be any low power chip resistor in the 50K or above range. They are optional. The purpose of these resistors is to provide a low current forcing the TVS into the avalanche mode causing the impedance at this node to be low. This reduces crosstalk and maintains a reasonable voltage across the steering diodes minimizing the diode junction capacitance and assuring minimum circuit loading.

Figure 5. graphically shows how multiple SMD bridge rectifiers can be used in conjunction with one or two TVS units in order to protect multiple line applications. Note that the cost of the TVS units then becomes amortized over the number of lines tied into it. In significant volumes it is possible to protect multiple data lines to a legitimate 600 W (on the 10/1000 μ s waveform) level at a cost far less than an individual TVS per line. And all the while the data lines are being loaded with less than 50 pF capacitance.



Multiple line protection can be implemented by tying several bridges into one set of TVS's. For single supply systems, one TVS can be eliminated and that node connected to ground.

Figure 5.



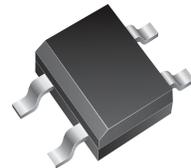
Clamping Occurs at
 $V_+ \text{ (or } V_-) \pm V_F (BRIDGE)$

Figure 6.

Figure 6. shows an alternate method of using a SMD bridge to provide effective low loss protection for "twisted pair" arrangements.



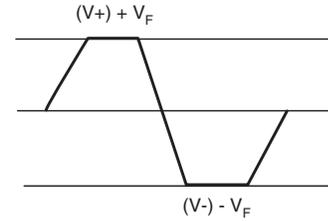
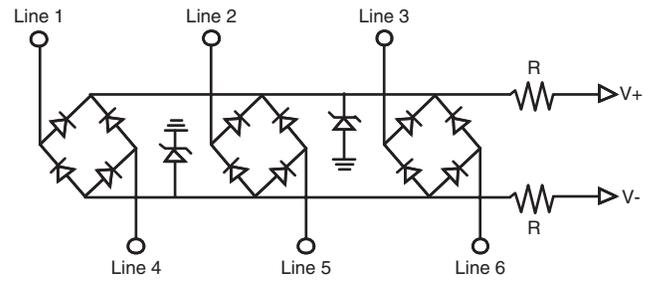
DFS



MBS

Figure 7. demonstrates a method of using the bridge rectifier arrangement to protect transceiver I/O ports by “steering” the transient overvoltages to either power supply rail or a single rail and ground. It is important to remember good “house keeping” when employing this topology ie; low inductance capacitors should bypass the power supply rails close to the circuitry being protected. If these rules are not followed the leading edge of any steep rise time transient will not be absorbed by the power supply. This will result in higher “let through” voltages and less effective protection.

The resultant performance of any of these circuits is severely influenced by parasitic elements in the circuit. Robust low impedance ground planes and simple PCB traces are essential. Series inductance in the PCB traces or grounding scheme will cause higher than expected let through voltage on fast rising transients. How fast is fast? and how much let through voltage is excessive? That will depend on the components you are protecting.



Clamping Occurs at
 $V+ \text{ (or } V- \text{)} \pm V_{F(BRIDGE)}$
 Figure 7.