TIME-TRIGGERED TECHNOLOGY
TTTech Computertechnik AG

TTP Powernode

A TTP Development Board for the Time-Triggered Architecture based on the AS8202NF TTP network controller

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TTP™ As Dependable as Time

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1 Overview

1.1 TTPPowernode Architecture

This board implements a powerful node according to the Time-Triggered Architecture with integrated TTP/C. It is a high-performance, state-of-the-art solution for distributed real-time systems and supports a broad range of interfaces. Front panel connectors and physical layer interface are placed on a separate board which is stacked on the base board of the TTPPowernode. This stackable solution provides a flexible way to adapt the TTPPowernode to customer specific demands on physical layer and connectors.

The TTPPowernode is equipped with the Motorola embedded Power PC processor (MPC555 Black Oak) and the AS8202NF TTP network controller.

The powerful host CPU with an additional on-chip FPU (floating point unit) makes the TTPPowernode suited for simulation purposes (i.e., to execute automatically generated code from tools like Matlab).

The TTPPowernode can be supplied with or without housing and power supply.

The basic architecture of this board is shown in the following Figure 1.1.

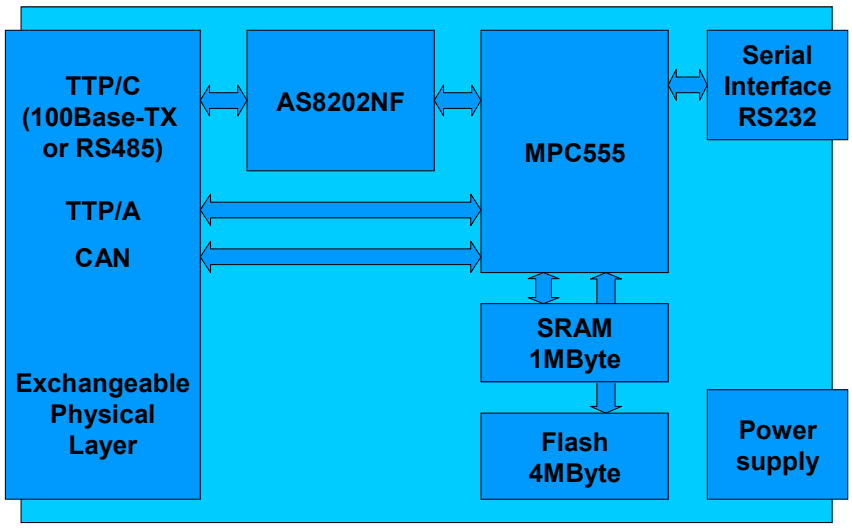

Figure 1.1: Block schematic of the TTPPowernode.

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1.2 Interfaces

The TTPPowernode architecture is very flexible. It provides the following signals on PCB-connectors on the base board:

- Multi-channel serial communication interface
- 32 analog inputs
- 16 channel timer system, 2 TPU units
- 8 PWM channels
- online debug features (BDM)
- 30 digital I/O pins
- 7 LEDs for host application and TTP/C communication status plus one Reset-switch located on the front-panel

The front panel connectors (for TTP/C, TTP/A, CAN and so on) are placed on a separate PCB which is stacked onto the TTPPowernode baseboard. The physical layer board options are described in chapter 5.

Currently two standard physical layer boards are available with the following configuration:

a) Physical layer board using the asynchronous (MFM) interface of the AS8202NF

TTP/C (two RJ45 sockets connected in parallel) on RS485 physical layer

TTP/A (RJ11 socket) on ISO9141 physical layer

CAN (RJ11 socket) on ISO11898 physical layer (Philips 82C250 driver)

b) Physical layer board using the synchronous (MII) interface of the AS8202NF

TTP/C (each channel on one RJ45 connector) on 100BASE-TX physical layer

TTP/A (RJ11 socket) on ISO9141 physical layer

CAN (RJ11 socket) on ISO11898 physical layer (Philips 82C250 driver)

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2 Host CPU

The host CPU system has the following features:

- Motorola MPC555 running at 40MHz
- PowerPC Core with Floating Point Unit
- 1Mbyte RAM (256 K x 32) plus 26kByte internal Static RAM
- 4Mbyte (1M x 32) burst able Flash plus 448kByte internal Flash Memory

The following Table 2.1 shows the memory map of the MPC555 as configured in the demo-software.

```
FLASH       on CS0      0x000000 – 0x3FFFFF   (4 MBytes)
RAM         on CS1      0x800000 – 0x8FFFFF   (1 MByte)
AS8202NF    on CS2      0x900000 – 0x901FFF   (8 KBytes)
```

Table 2.1: Used Chip selects of the MPC555.

The Chip Select configuration (example) for the AS8202NF on CS2 of the MPC555 is described in Table 2.2.

The PN312 generates a TA\ signal (for the MPC555) from the AS8202NF READY\ signal and thus reduces the access time according to the values stated in the datasheet of the AS8202NF.

```
BR2  (Base Register for CS2):       0x00C00827
OR2  (Option Register for CS2):     0xFFFF86F1
```

Table 2.2: Chips select settings for CS2 on PN312.

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3 TTP Global Time

The TTP communication controller provides a global time base with high resolution and high precision (defined by the MEDL of the TTP network controller). This information is provided to the host CPU by a programmable TTP interrupt line. The AS8202NF provides some other features like “remote pin voting” or bus guardian signals. These signals are also configurable by the MEDL. For a detailed description please refer to the AS8202NF datasheet (V1.2 chapter 8.7 LED signals).

On the TTP-Powernode PN312 this LED signals are routed to the physical layer connectors and are available for usage on customer specific physical layer boards.

Function	***Pin of AS8202NF***	***Pin of Host CPU (MPC555)***
TTP interrupt line	INTB (Pin 28)	IRQ3\
Depends on MEDL configuration	LED0 (Pin 33)	May be connected via customer specific physical layer board.
Depends on MEDL configuration	LED1 (Pin 32)	May be connected via customer specific physical layer board.
Depends on MEDL configuration	LED2 (Pin 31)	May be connected via customer specific physical layer board.

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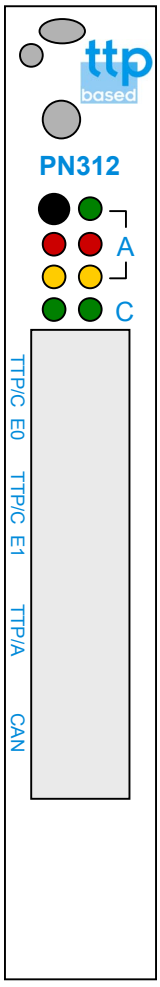
4 Indicator LEDs

The TTP Powernode has seven indicator LEDs, which are mounted on the front panel. The layout and identifiers of the front panel LEDs are given by the following figure:



Left Side	*Right Side*
RESET Switch	HOST1
HOST2	HOST3
HOST4	HOST5
TTP/C a	TTP/C b

The following tables describe the functionality of the individual status LEDs on the front panel.

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Unit	*Pin*[1]	*Front Panel*	*Function*	*Color*
AS8202NF	LED0, LED1	TTP/C b, TTP/C a	See table below	green
Host CPU (MPC555)	MPIO9	HOST1	freely programmable	green
	MPIO12	HOST2	freely programmable	red
	MPIO13	HOST3	freely programmable	red
	MPIO10	HOST4	freely programmable	yellow
	MPIO11	HOST5	freely programmable	yellow

Table 4.1: Status LED description.

TTP/C b (LED0)	*Function*
off	Controller is off
on	Listen state or passive download client
50/50 on/off duty cycle	Passive state
25/75 on/off duty cycle	Synchronized active state

Table 4.2: Status LED0 of the AS8202NF in protocol activity mode.

TTP/C a (LED1)	*Function*
off	No synchronization is achieved.
on	Cluster synchronization is achieved.

Table 4.3: Status LED1 of the AS8202NF in protocol activity mode.

[1] LED0, LED1, MPIO10 and MPIO11 are routed over the physical layer board and thus can have different functions on different physical layer boards. The function according to Table 4.1 is for TTTechs MFM and MII physical layer boards.

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5 TTPPowernode physical layer options

The TTPPowernode is available with different physical layer boards. The following section shows the different available options with their features. The physical layer boards are stacked onto the base board of the TTPPowernode and thus can be exchanged by the customer if required.

5.1 Option “MFM”

Used front panel connectors:

TTP/C E0 : TTP/C (both channels) on RS485 physical layer, max. 5Mbit, MFM coding on the AS8202NFs TTP bus interface.

TTP/C E1 : TTP/C (both channels) on RS485 physical layer, max. 5Mbit, MFM coding on the AS8202NFs TTP bus interface.

TTP/A : TTP/A (two channels) on ISO9141 physical layer.

CAN : CAN (two channels) on ISO11898 physical layer.

5.2 Option “MII”

Used front panel connectors:

TTP/C E0 : TTP/C (Channel A) on 100BASE-TX physical layer, 25Mbit, MII coding on AS8202NFs TTP bus interface.

TTP/C E1 : TTP/C (Channel B) on 100BASE-TX physical layer, 25Mbit, MII coding on AS8202NFs TTP bus interface.

TTP/A : TTP/A (two channels) on ISO9141 physical layer.

CAN : CAN (two channels) in ISO11898 physical layer.

5.3 Instructions for replacing the physical layer board

a) Remove the front-panel.

b) Remove the mounting screws on the physical layer board.

c) Remove the physical layer board. (usage of a lever e.g. screw driver is recommended)

d) Insert the required physical layer board. (for Option “MFM” use Distance bolts A,B,C; for Option “MII” use distance bolts A, C; see Figure 6.1)

e) Fix the physical layer board with the screws.

f) Mount the front panel.

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6 Connectors – base board

The TTPPowernode has thirteen connectors. The following Figure 6.1 shows the position and name of the connectors.

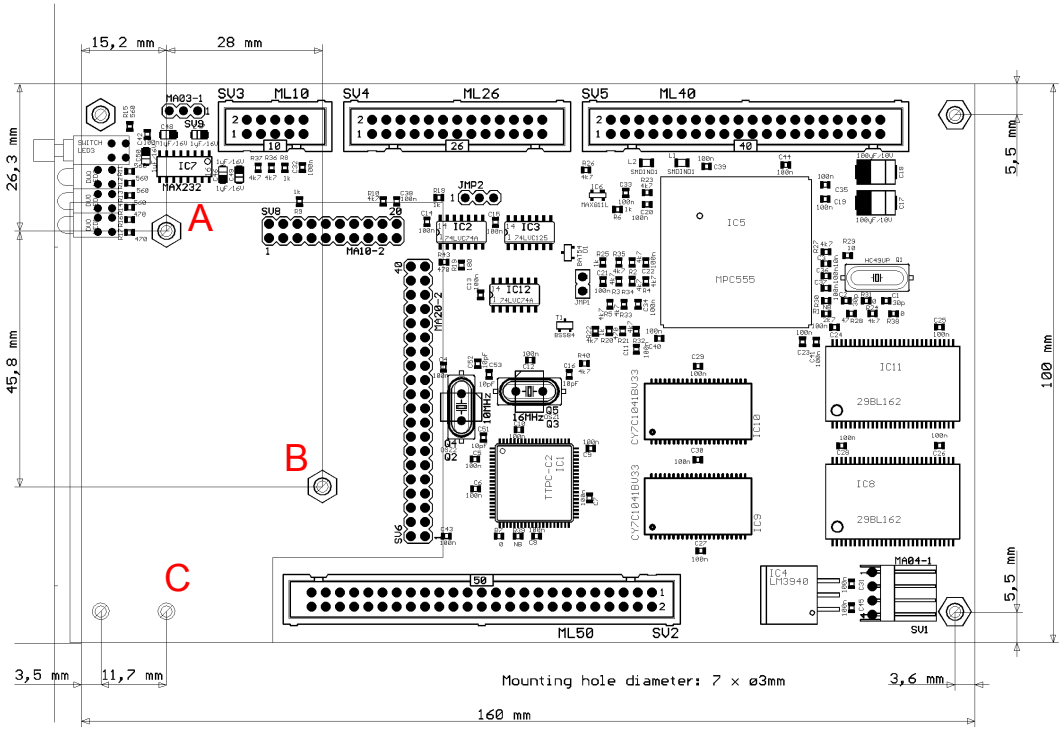

Figure 6.1: Placeplan of the base board of the TTPPowernode (PN312).

6.1 SV1 Power Supply

Pin	*Name*	*Function*
1	VCC	Supply +5V +/- 5%, typ. 300mA, max 1,5 A
2	GND	Supply ground
3	GND	Supply ground
4	+12V	Supply +12V, max 150mA

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6.2 SV2 Multifunction I/O Connector

Pin	*Name*	*I/O CPU Pin*	*Function*	*Direction*
1	MPWM19	MPWM19	PWM channel	I/O
2	MPWM18	MPWM18	PWM channel	I/O
3	MPWM17	MPWM17	PWM channel	I/O
4	MPWM16	MPWM16	PWM channel	I/O
5	MPWM3	MPWM3	PWM channel	I/O
6	MPWM2	MPWM2	PWM channel	I/O
7	MPWM1	MPWM1	PWM channel	I/O
8	MPWM0	MPWM0	PWM channel	I/O
9	GND		Supply Ground	
10	GND		Supply Ground	
11	MDA31	MDA31	timer channel	I/O
12	MDA30	MDA30	timer channel	I/O
13	MDA29	MDA29	timer channel	I/O
14	MDA28	MDA28	timer channel	I/O
15	MDA27	MDA27	timer channel	I/O
16	MDA15	MDA15	timer channel	I/O
17	MDA14	MDA14	timer channel	I/O
18	MDA13	MDA13	timer channel	I/O
19	MDA12	MDA12	timer channel	I/O
20	MDA11	MDA11	timer channel	I/O
21	VF0	VF0	Debug /MPIO	I/O
22	VF1	VF1	Debug /MPIO	I/O
23	VF2	VF2	Debug /MPIO	I/O
24	VFL0	VFL0	Debug /MPIO	I/O
25	VFL1	VFL1	Debug /MPIO	I/O
26	MPIO5	MPIO5	Digital I/O	I/O
27	MPIO6	MPIO6	Digital I/O	I/O
28	MPIO7[2]	MPIO7	Digital I/O	(I/O)
29	MPIO8	MPIO8	Digital I/O	I/O
30	MPIO9[3]	MPIO9	Digital I/O	(I/O)
31	MPIO10[4]	MPIO10	Digital I/O	(I/O)
32	MPIO11[5]	MPIO11	Digital I/O	(I/O)
33	MPIO12[6]	MPIO12	Digital I/O	(I/O)
34	MPIO13[7]	MPIO13	Digital I/O	(I/O)
35	MPIO14	MPIO14	Digital I/O	I/O

[2] This signal is pulled to 5Volt with a 1kOhm resistor and can be configured (with JMP2) to be connected to the front panel switch.

[3] This signal is connected to a front panel LED. See table Table 4.1.

[4] This signal is connected to a front panel LED. See table Table 4.1.

[5] This signal is connected to a front panel LED. See table Table 4.1.

[6] This signal is connected to a front panel LED. See table Table 4.1.

[7] This signal is connected to a front panel LED. See table Table 4.1.

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36	MPIO15	MPIO15	Digital I/O	I/O
37	VDDH		Supply +5V	
38	GND		Supply Ground	
39	QS_ECK	ECK	External baud clock	I
40	QS_RXD2[8]	RXD2	SCI2	I
41	QS_TXD2[9]	TXD2	SCI2	O
42	GND		Supply Ground	
43	GND		Supply Ground	
44	QS_PCS0	PCS0	QSPI	I/O
45	QS_PCS1	PCS1	QSPI	I/O
46	QS_PCS2	PCS2	QSPI	I/O
47	QS_PCS3	PCS3	QSPI	I/O
48	QS_MISO	MISO	QSPI	I/O
49	QS_MOSI	MOSI	QSPI	I/O
50	QS_SCK	SCK	QSPI	I/O

6.3 SV3 BDM Interface

Pin	***Name***	***Function***	***Direction***
1	VFLS0	BDM	O
2	SRESET\	BDM / Soft Reset CPU	I/O
3	GND	Supply Ground	
4	DSCK	BDM	I
5	GND	Supply Ground	
6	VFLS1	BDM	O
7	HRESET\	BDM / Hard Reset CPU	I/O
8	DSDI	BDM	I
9	VDDL	Supply +3,3V	
10	DSDO	BDM	O

6.4 SV4 TPU

Pin	***Name***	***I/O CPU Pin***	***Function***	***Direction***
1	GND		Supply Ground	
2	GND		Supply Ground	
3	B_TPUCH0	B_TPUCH0	TPU channel	I/O

[8] This signal is used on the physical layer board for the TTP/A functionality. It can only be used when IC4 (MC33290) on the physical layer board is removed.

[9] This signal is used on the physical layer board for the TTP/A functionality. It can only be used when IC4 (MC33290) on the physical layer board is removed.

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4	B_TPUCH1	B_TPUCH1	TPU channel	I/O
5	B_TPUCH2	B_TPUCH2	TPU channel	I/O
6	B_TPUCH3	B_TPUCH3	TPU channel	I/O
7	B_TPUCH8	B_TPUCH8	TPU channel	I/O
8	B_TPUCH9	B_TPUCH9	TPU channel	I/O
9	B_TPUCH10	B_TPUCH10	TPU channel	I/O
10	B_TPUCH11	B_TPUCH11	TPU channel	I/O
11	A_T2CLK	A_T2CLK	TPU clock	I/O
12	GND		Supply Ground	
13	A_TPUCH0	A_TPUCH0	TPU channel	I/O
14	A_TPUCH1	A_TPUCH1	TPU channel	I/O
15	A_TPUCH2	A_TPUCH2	TPU channel	I/O
16	A_TPUCH3	A_TPUCH3	TPU channel	I/O
17	GND		Supply Ground	
18	GND		Supply Ground	
19	A_TPUCH4	A_TPUCH4	TPU channel	I/O
20	A_TPUCH5	A_TPUCH5	TPU channel	I/O
21	A_TPUCH6	A_TPUCH6	TPU channel	I/O
22	A_TPUCH7	A_TPUCH7	TPU channel	I/O
23	A_TPUCH12	A_TPUCH12	TPU channel	I/O
24	A_TPUCH13	A_TPUCH13	TPU channel	I/O
25	A_TPUCH14	A_TPUCH14	TPU channel	I/O
26	A_TPUCH15	A_TPUCH15	TPU channel	I/O

6.5 SV5 Analog Inputs

Pin	***Name***	***CPU Pin***	***Function***	***Discrete I/O***
1	AAN0	AAN0_PQB0	analog input	I
2	AAN1	AAN1_PQB1	analog input	I
3	AAN2	AAN2_PQB2	analog input	I
4	AAN3	AAN3_PQB3	analog input	I
5	AAN48	AAN48_PQB4	analog input	I
6	AAN49	AAN49_PQB5	analog input	I
7	AAN50	AAN50_PQB6	analog input	I
8	AAN51	AAN51_PQB7	analog input	I
9	AGND	VSSA	analog ground	
10	AGND	VSSA	analog ground	
11	AAN52	AAN52_PQA0	analog input	I/O
12	AAN53	AAN53_PQA1	analog input	I/O
13	AAN54	AAN54_PQA2	analog input	I/O
14	AAN55	AAN55_PQA3	analog input	I/O
15	AAN56	AAN56_PQA4	analog input	I/O
16	AAN57	AAN57_PQA5	analog input	I/O
17	AAN58	AAN58_PQA6	analog input	I/O
18	AAN59	AAN59_PQA7	analog input	I/O
19	AGND	VSSA	analog ground	

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20	AGND	VSSA	analog ground	
21	BAN0	BAN0_PQB0	analog input	I
22	BAN1	BAN1_PQB1	analog input	I
23	BAN2	BAN2_PQB2	analog input	I
24	BAN3	BAN3_PQB3	analog input	I
25	BAN48	BAN48_PQB4	analog input	I
26	BAN49	BAN49_PQB5	analog input	I
27	BAN50	BAN50_PQB6	analog input	I
28	BAN51	BAN51_PQB7	analog input	I
29	AGND	VSSA	analog ground	
30	AGND	VSSA	analog ground	
31	BAN52	BAN52_PQA0	analog input	I/O
32	BAN53	BAN53_PQA1	analog input	I/O
33	BAN54	BAN54_PQA2	analog input	I/O
34	BAN55	BAN55_PQA3	analog input	I/O
35	BAN56	BAN56_PQA4	analog input	I/O
36	BAN57	BAN57_PQA5	analog input	I/O
37	BAN58	BAN58_PQA6	analog input	I/O
38	BAN59	BAN59_PQA7	analog input	I/O
39	ETRIG2	ETRIG2	External Trigger	
40	ETRIG1	ETRIG1	External Trigger	

6.6 SV6 Physical layer interface

Pin	***Name***	***Function***
1	+12V	Supply +12V
2	+12V	Supply +12V
3	CTS1	AS8202NF, Clear to send – channel B (a)(b)[10]
4	TXD1	AS8202NF, Transmit data – channel B (a)(b)
5	RXER1	AS8202NF, Receive error – channel B (b)
6	TXCLK1	AS8202NF, Transmit clock – channel B (b)
7	RXDV1	AS8202NF, Receive data valid – channel B (b)
8	RXCLK1	AS8202NF, Receive clock – channel B (b)
9	TXD0	AS8202NF, Transmit data – channel A (a)(b)
10	RXD1	AS8202NF, Receive data – channel B (a)(b)
11	TXCLK0	AS8202NF, transmit clock – channel A (b)
12	CTS0	AS8202NF, Clear to send – channel A (a)(b)
13	RXCLK0	AS8202NF, Receive clock – channel A (b)
14	RXER0	AS8202NF, Receive error – channel A (b)
15	RXD0	AS8202NF, Receive data – channel A (a)(b)
16	RXDV0	AS8202NF, Receive data valid – channel A (b)
17	QS_RXD2	MPC555, Receive data, serial interface 2
18	QS_TXD2	MPC555, Transmit data, serial interface 2
19	QS_PCS0	MPC555, SPI Chip select 0
20	QS_PCS1	MPC555, SPI Chip select 1
21	QS_PCS2	MPC555, SPI Chip select 2

[10] (a) ... used in MFM mode, (b) ... used in MII mode.

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22	QS_PCS3	MPC555, SPI Chip select 3
23	VDDL	Supply +3,3V
24	VDDL	Supply +3,3V
25	QS_MISO	MPC555, SPI Master in slave out
26	QS_MOSI	MPC555, SPI Master out slave in
27	QS_SCK	MPC555, SPI Clock
28	MPIO5	MPC555, parallel I/O 5
29	MPIO6	MPC555, parallel I/O 6
30	MPIO10	MPC555, parallel I/O 10
31	MPIO11	MPC555, parallel I/O 11
32	C_LED0	AS8202NF, LED0
33	C_LED1	AS8202NF, LED1
34	C_LED2	AS8202NF, LED2
35	A_CNRX0	MPC555, CAN A receive
36	A_CNTX0	MPC555, CAN A transmit
37	BTPUCH4	MPC555, TPU B channel 4
38	BTPUCH5	MPC555, TPU B channel 5
39	GND	Supply Ground
40	GND	Supply Ground

6.7 SV8 Physical layer interface

Pin	***Name***	***Function***
1	P_LED1	Front panel LED (TTP/C b)
2	P_LED0	Front panel LED (Host 4)
3	P_LED3	Front panel LED (TTP/C a)
4	P_LED2	Front panel LED (Host 5)
5	HRESET\	MPC555, Hard reset
6	SRESET\	MPC555, Soft reset
7	BTPUCH10	MPC555, TPU B channel 10
8	BTPUCH11	MPC555, TPU B channel 11
9	GND	Supply Ground
10	GND	Supply Ground
11	ATPUCH10	MPC555, TPU A channel 10
12	ATPUCH8	MPC555, TPU A channel 8
13	ATPUCH9	MPC555, TPU A channel 9
14	ATPUCH11	MPC555, TPU A channel 11
15	B_CNTX0	MPC555, CAN B transmit
16	B_CNRX0	MPC555, CAN B receive
17	A_IRQ\	MPC555, Interrupt IRQ4\
18	CLK	MPC555, system clock
19	VDDH	Power Supply +5V
20	VDDH	Power Supply +5V

6.8 SV9 Serial interface Host CPU

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Pin	*Name*	*Host CPU Pin*	*Function*	*Direction*
1	GND		Supply Ground	
2	C_TXD	TXD1	Serial output	O
3	C_RXD	RXD1	Serial input	I

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7 How to connect the serial interface cable to the TTPPowernode

7.1 Serial cable on the TTPPowernode PN312

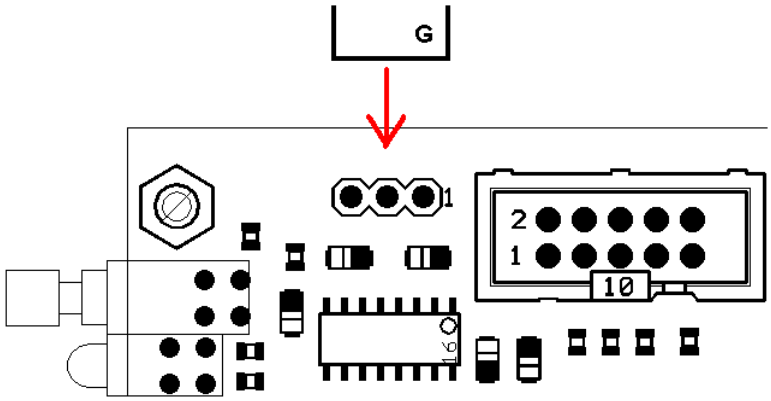

Figure 7.1: Connecting the serial cable to the TTPPowernode PN312.

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8 Mounting Options

8.1 Clock source for the AS8202NF (IC1)

The AS8202NF has the possibility to use either an external quartz or an external quartz oscillator as clock source for the internal PCU and the bus guardian. A mounting option on the PCB of the base board allows the user to use this feature.

8.1.1 Mounting option Quartz oscillator

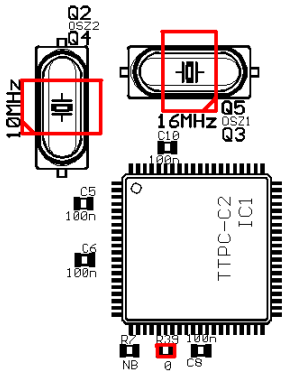

Figure 8.1: Quartz Oscillator and R39 (0Ohm) mounted (red).

8.1.2 Mounting option Quartz

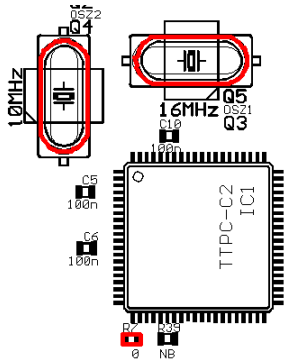

Figure 8.2: Quartz and R7 (0Ohm) mounted (red)

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9 Connectors – physical layer boards

The following Figure 9.1 shows the numbering convention used for the RJ45 physical layer connectors. Figure 9.2 describes the numbering for the RJ11 connectors (TTP/A and CAN).

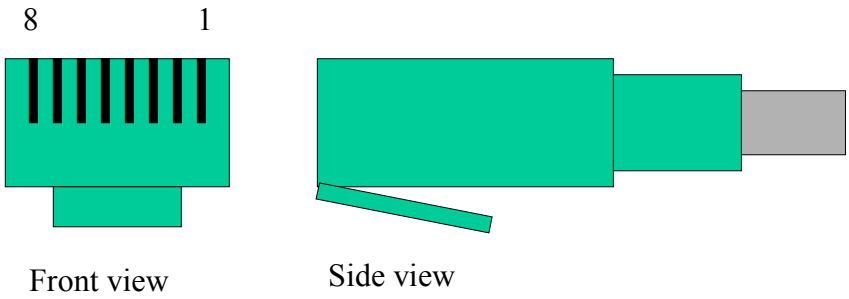

Figure 9.1: Numbering convention used for the TTP physical layer connectors.

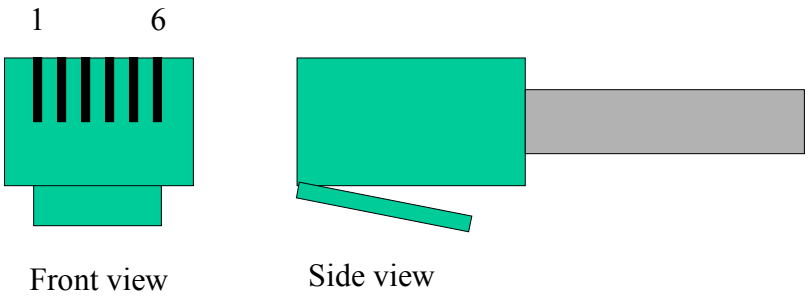

Figure 9.2: Numbering convention used for the TTP/A and CAN connectors.

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9.1 Physical layer board for the asynchronous bus interface of the AS8202NF (MFM/MAN coding, RS485 physical layer)

The place plan of the board is shown in Figure 9.3.

9.1.1 CON3 TTP/C E0

Pin	*Name*	*Function*
1	GND	Supply Ground
2	GND	Supply Ground
3	CH0_LOW	RS485 low signal, channel A
4	CH1_HIGH	RS485 high signal, channel B
5	CH1_LOW	RS485 low signal, channel B
6	CH0_HIGH	RS485 high signal channel A
7	GND	Supply Ground
8	GND	Supply Ground

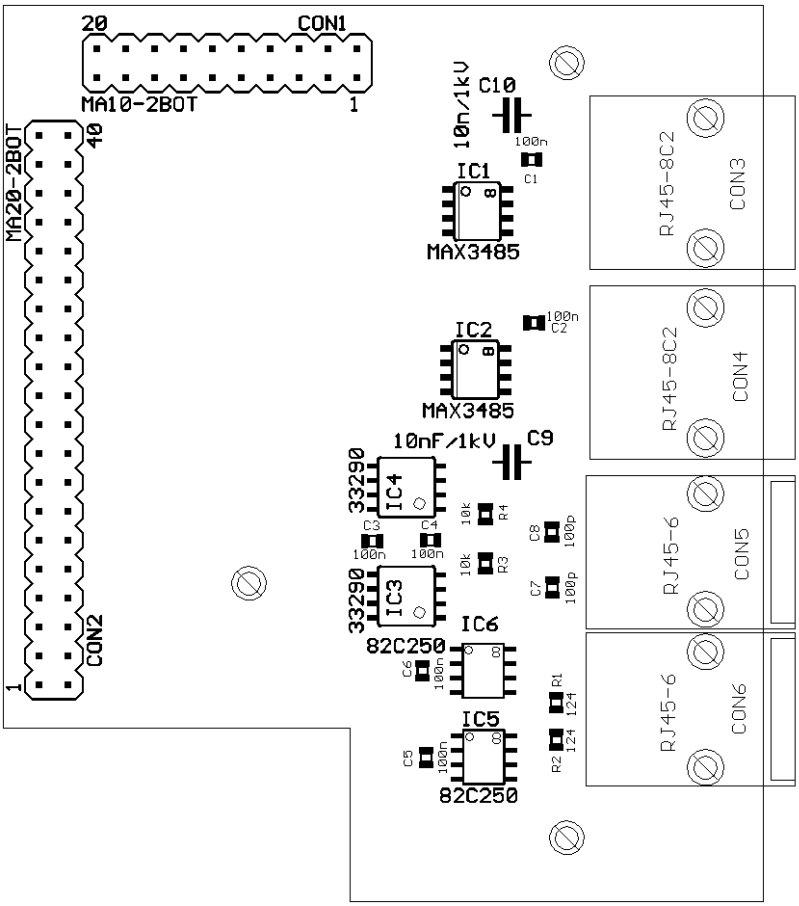

Figure 9.3: Place plan of the physical layer board for the asynchronous TTP bus interface.

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9.1.2 CON4 TTP/C E1

Pin	*Name*	*Function*
1	GND	Supply Ground
2	GND	Supply Ground
3	CH0_LOW	RS485 low signal, channel A
4	CH1_HIGH	RS485 high signal, channel B
5	CH1_LOW	RS485 low signal, channel B
6	CH0_HIGH	RS485 high signal channel A
7	GND	Supply Ground
8	GND	Supply Ground

9.1.3 CON5 TTP/A

Pin	*Name*	*Function*
1	NC	not connected
2	CH A	TTP/A channel A, using MPC555 serial interface 2
3	NC	reserved for external TTP/A supply
4	GND	Supply ground
5	CH B	TTP/A channel B, using MPC555 TPU A channel 10 and 11
6	NC	not connected

9.1.4 CON6 CAN

Pin	*Name*	*Function*
1	CANB_H	CAN high signal, channel B
2	CANB_L	CAN low signal, channel B
3	GND	Supply Ground
4	GND	Supply Ground
5	CANA_H	CAN high signal, channel A
6	CANA_L	CAN low signal, channel A

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9.2 Physical layer board for the synchronous bus interface of the AS8202NF (MII coding, 100BASE-TX physical layer)

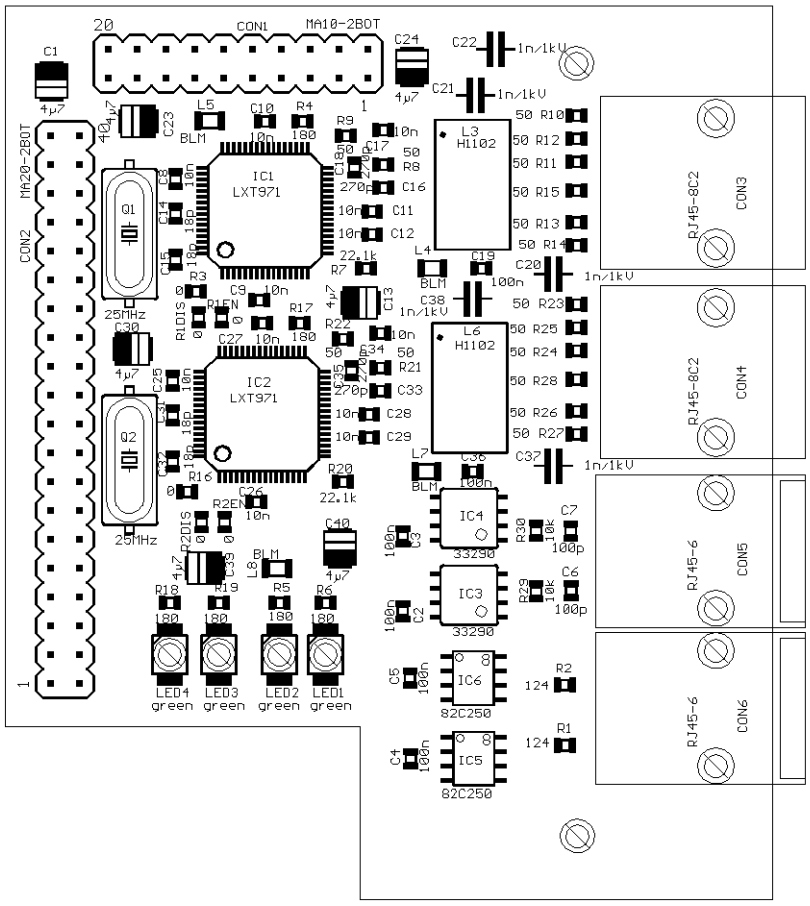

Figure 9.4: Place plan of the physical layer board for the synchronous TTP bus interface.

9.2.1 CON3 TTP/C E0

Pin	*Name*	*Function*
1	RD+	AS8202NF, 100BASE-TX, receive data high
2	RD-	AS8202NF, 100BASE-TX, receive data low
3	TD+	AS8202NF, 100BASE-TX, transmit data high
4	NC	not connected (internal termination)
5	NC	not connected (internal termination)
6	TD-	AS8202NF, 100BASE-TX, transmit data low

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7	NC	not connected (internal termination)
8	NC	not connected (internal termination)

9.2.2 CON4 TTP/C E1

Pin	*Name*	*Function*
1	RD+	AS8202NF, 100BASE-TX, receive data high
2	RD-	AS8202NF, 100BASE-TX, receive data low
3	TD+	AS8202NF, 100BASE-TX, transmit data high
4	NC	not connected (internal termination)
5	NC	not connected (internal termination)
6	TD-	AS8202NF, 100BASE-TX, transmit data low
7	NC	not connected (internal termination)
8	NC	not connected (internal termination)

9.2.3 CON5 TTP/A

Pin	*Name*	*Function*
1	NC	not connected
2	CH A	TTP/A channel A, using MPC555 serial interface 2
3	NC	reserved for external TTP/A supply
4	GND	Supply ground
5	CH B	TTP/A channel B, using MPC555 TPU A channel 10 and 11
6	NC	not connected

9.2.4 CON6 CAN

Pin	*Name*	*Function*
1	CANB_H	CAN high signal, channel B
2	CANB_L	CAN low signal, channel B
3	GND	Supply Ground
4	GND	Supply Ground
5	CANA_H	CAN high signal, channel A
6	CANA_L	CAN low signal, channel A

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10 Jumper

10.1 JMP1

Jumper JMP1 is located in the middle of the board near the MPC555 and has the following function.

Shorted .. Reset Configuration for the MPC555 is fetched from external data-bus (D20 is 1, all other bits are 0).

Open .. Reset Configuration for the MPC555 is either a standard value or fetched from internal NVM, if a valid configuration word is programmed. (NVM is programmable via BDM Flash programmer)

10.2 JMP2

Pin 1-2 connected: Front panel switch connected to MPIO7 pin of the MPC555.

Pin 2-3 connected: Front panel switch is used as reset switch.

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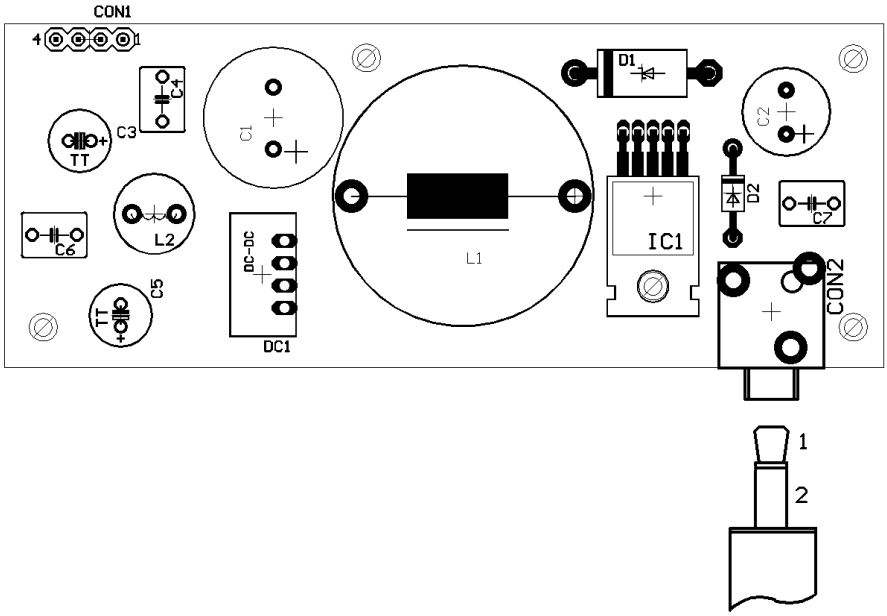
11 Optional Power Supply



11.1 CON1 DC Output

Pin	*Name*	*Function*
1	VCC	Supply +5V, max 1.5 A
2	GND	Supply Ground
3	GND	Supply Ground
4	+12V	Supply +12V, max 150mA

11.2 CON2 DC Input

Pin	*Function*
1	Supply 9 to 60 V DC @ max. 1.2 A
2	Supply Ground

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12 Specifications Summary

Characteristic	*Specifications*	
	TTPPowernode	**Power Supply**
I/O ports	HCMOS Compatible	-
Dimensions	100 mm x 160 mm	39 mm x 100 mm
Operating Temperature	0° C to +70° C	
Storage Temperature	-40° C to +85° C	
Humidity	Max. 90% relative humidity (non condensing) for temperatures up to 40°C Max. 60% relative humidity (non condensing) for temperatures up to 70°C	Max. 90% relative humidity (non condensing) for temperatures up to 40°C Max. 60% relative humidity (non condensing) for temperatures up to 70°C
Power Requirements	5 V DC, +/- 5% @ 1 A (depends on the physical layer used) 12 V DC @ 150 mA	9 to 60 V DC, @ 10 W

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13 Document Revisions

Version	*Date*	*Changes*	*by*
2.0.00	17.12.2003	Original document (derived from TTP-Powernode PN212 manual V2.0.08)	RLE
2.0.01	29.3.2004	Connector info added	RLE
2.0.02	1.12.2004	Minor changes in connector description	RLE
2.0.03	27.05.2005	Minor changes in connector description, Humidity added	RLE

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