Device Features

- **Low power 1.8V operation**
- **Small footprint in 96-ball VFBGA and LGA packages (6x6mm 8x8mm and 10x10mm)**
- **Fully qualified Bluetooth component**
- **0.18µm CMOS technology**
- **Full speed Bluetooth™ operation with full piconet support**
- **Support for 8Mbit external flash**
- **Minimum external components**

BlueCore™2-External

Single Chip Bluetooth System

Production Information Data Sheet for:

BC212013
(UART only version)

BC212015
(USB and UART version)

July 2002

General Description

BlueCore2-External is a single chip radio and baseband IC for Bluetooth 2.4GHz systems. It is implemented in 0.18µm CMOS technology.

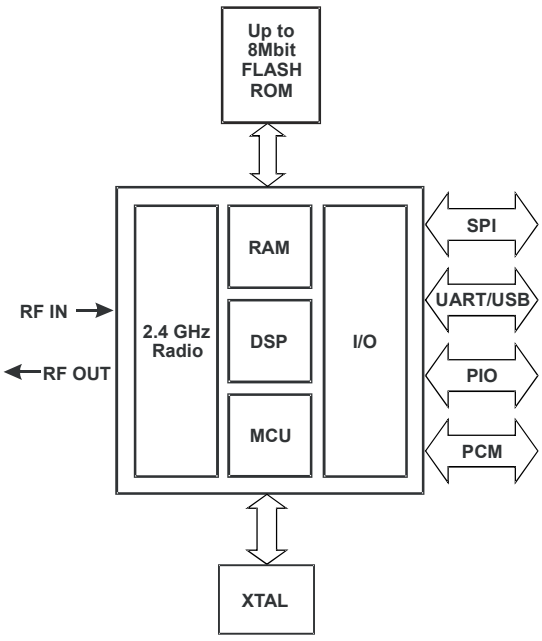
When used with external flash containing the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system for data and voice communications.

Applications

- **PCs**
- **Cellular Handsets**
- **Cordless Headsets**
- **Personal Digital Assistants (PDAs)**
- **Computer Accessories (Compact flash Cards, PCMCIA Cards, SD Cards and USB Dongles)**
- **Mice, Keyboards and Joysticks**
- **Digital Cameras and Camcorders**

BlueCore2-External has been designed to reduce the number of external RF components required, which ensures module production costs are minimised.

The device incorporates auto calibration and built-in self-test routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth specification v1.1.



BlueCore2-External Block Diagram

Bluetooth™ Qualified

Table of Contents

1 Key Features

Radio

- Operation with common TX/RX terminals simplifies external matching circuitry and eliminates external antenna switch
- Extensive built-in self-test minimises production test time
- No external trimming is required in production
- Full RF reference designs are available

Transmitter

- Up to +6dBm RF transmit power with level control from the on-chip 6-bit DAC over a dynamic range greater than 30dB
- Supports Class 2 and Class 3 radios without the need for an external power amplifier or TX/RX switch
- Supports Class 1 radios with an external power amplifier provided by a power control terminal controlled by an internal 8-bit voltage DAC and an external RF TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Digitised RSSI available in real time over the HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser; no external VCO varactor diode or resonator
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands and an integrated low power oscillator for ultra-low Park/Sniff/Hold mode power consumption
- Device can be used with an external Master oscillator and provides a ‘clock request signal’ to control external clock source
- Uncommitted 8-bit ADC and 8-bit DAC are available to application programs

Baseband and Software

- External 8Mbit flash for complete system solution and application flexibility
- 32kbyte on-chip RAM allows full speed Bluetooth data transfer, mixed voice and data, plus full 7 slave piconet operation
- Dedicated logic for forward error correction, header error control, access code correlation, demodulation, cyclic redundancy check, encryption bitstream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud
- UART interface with programmable Baud rate up to 1.5MBaud
- Full speed USB interface supports OHCI and UHCI host interfaces. Compliant with USB v1.1
- Synchronous bi-directional serial programmable audio interface
- Optional I^2C^{TM} compatible interface

Bluetooth Stack Running on an Internal Microcontroller

CSR’s Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM, thus reducing host CPU load

Package Options

- 96-ball LFBGA 10x10x1.4mm 0.80mm pitch
- 96-ball VFBGA 8x8x1.0mm 0.65mm pitch
- 96-ball VFBGA 6x6x1.0mm 0.50mm pitch
- 96-ball VFLGA 6x6x0.65mm 0.50mm pitch

2 Device Pinout Diagram

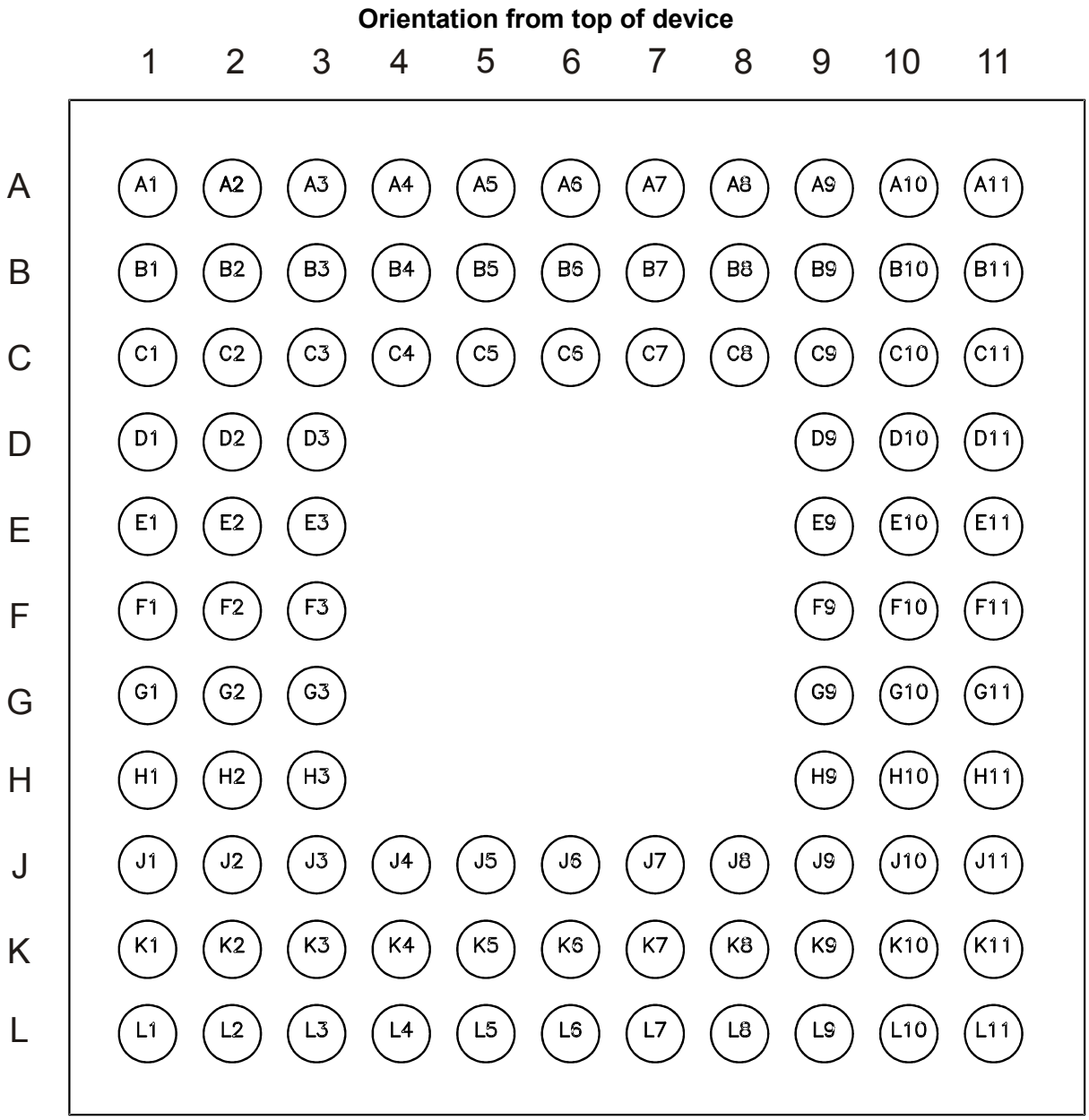


Figure 2.1: BlueCore2-External Device Pinout Diagram

Notes:

Device pinout diagram is the same for:

10x10mm LFBGA (BN)

8x8x1mm VFBGA package (DN)

6x6x1mm VFBGA package (EN)

6x6x0.6mm LGA package (LN)

3 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	E1	Analogue	Single ended receiver input
PIO[0]/RXEN	C1	Bi-directional with weak internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	C2	Bi-directional with weak internal pull-up/down	Control output for external PA Class 1 applications only
TX_A	G1	Analogue	Transmitter output/Switched Receiver input
TX_B	F1	Analogue	Complement of TX_A
AUX_DAC	D2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L1	Analogue	For crystal or external clock input
XTAL_OUT	L2	Analogue	Drive for crystal
LOOP_FILTER	J1	Analogue	Connection to external PLL loop filter

External Memory Port	Ball	Pad Type	Description
REB	D10	CMOS output, tristatable with internal weak pull-up	Read enable for external memory (active low)
WEB	E10	CMOS output, tristatable with internal weak pull-up	Write enable for external memory (active low)
CSB	C10	CMOS output, tristatable with internal weak pull-up	Chip select for external memory (active low)

Address Lines	Ball	Pad Type	Description
A[0]	D9	CMOS output, tristatable	Address line
A[1]	E9	CMOS output, tristatable	Address line
A[2]	E11	CMOS output, tristatable	Address line
A[3]	F9	CMOS output, tristatable	Address line
A[4]	F10	CMOS output, tristatable	Address line
A[5]	F11	CMOS output, tristatable	Address line
A[6]	G9	CMOS output, tristatable	Address line
A[7]	G10	CMOS output, tristatable	Address line
A[8]	G11	CMOS output, tristatable	Address line
A[9]	H9	CMOS output, tristatable	Address line
A[10]	H10	CMOS output, tristatable	Address line
A[11]	H11	CMOS output, tristatable	Address line
A[12]	J8	CMOS output, tristatable	Address line
A[13]	J9	CMOS output, tristatable	Address line
A[14]	J10	CMOS output, tristatable	Address line
A[15]	J11	CMOS output, tristatable	Address line
A[16]	K9	CMOS output, tristatable	Address line
A[17]	K10	CMOS output, tristatable	Address line
A[18]	K11	CMOS output, tristatable	Address line

Data Bus	Ball	Pad Type	Description
D[0]	K8	Bi-directional with weak internal pull-down	Data line
D[1]	L9	Bi-directional with weak internal pull-down	Data line
D[2]	L10	Bi-directional with weak internal pull-down	Data line
D[3]	L11	Bi-directional with weak internal pull-down	Data line
D[4]	L8	Bi-directional with weak internal pull-down	Data line
D[5]	J7	Bi-directional with weak internal pull-down	Data line
D[6]	K7	Bi-directional with weak internal pull-down	Data line
D[7]	L7	Bi-directional with weak internal pull-down	Data line
D[8]	J6	Bi-directional with weak internal pull-down	Data line
D[9]	K6	Bi-directional with weak internal pull-down	Data line
D[10]	L6	Bi-directional with weak internal pull-down	Data line
D[11]	J5	Bi-directional with weak internal pull-down	Data line
D[12]	K5	Bi-directional with weak internal pull-down	Data line
D[13]	L5	Bi-directional with weak internal pull-down	Data line
D[14]	J4	Bi-directional with weak internal pull-down	Data line
D[15]	K4	Bi-directional with weak internal pull-down	Data line

PCM Interface	Ball	Pad Type	Description
PCM_OUT	B9	CMOS output, tristatable with internal weak pull-down	Synchronous data output
PCM_IN	B10	CMOS input, with internal weak pull-down	Synchronous data input
PCM_SYNC	B11	Bi-directional with weak internal pull-down	Synchronous data SYNC
PCM_CLK	B8	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	C8	CMOS output	UART data output active high
UART_RX	C9	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	B7	CMOS output, tristatable with internal pull-up	UART request to send active low
UART_CTS	B6	CMOS input with weak internal pull-down	UART clear to send active low
USB_D+ (1)	A7	Bi-directional	USB data plus
USB_D- (1)	A6	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESET	F3	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
SPI_CSB	A4	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	B5	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	A5	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B4	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	G3	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port[3]	Ball	Pad Type	Description
PIO[2]/ USB_PULL_UP [1] [2]	B3	Bi-directional with programmable weak internal pull-up/down	PIO or USB pull-up (via 1.5kΩ resistor to USB_D+)
PIO[3]/USB_WAKE_ UP/RAM_CSB [1] [2]	B2	Bi-directional with programmable weak internal pull-up/down	PIO or output goes high to wake up PC when in USB mode or external RAM chip select
PIO[4]/USB_ON [1] [2]	B1	Bi-directional with programmable weak internal pull-up/down	PIO or USB on (input senses when VBUS is high, wakes BlueCore2-External)
PIO[5]/USB_DETACH [1] [2]	A3	Bi-directional with programmable weak internal pull-up/down	PIO line or chip detaches from USB when this input is high
PIO[6]/CLK_REQ	C3	Bi-directional with programmable weak internal pull-up/down	PIO line or clock request output to enable external clock for external clock line
PIO[7]	E3	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[8]	D3	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[9]	C4	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[10]	C5	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[11]	C6	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
AIO[0]	K3	Bi-directional	Programmable input/output line
AIO[1]	L4	Bi-directional	Programmable input/output line
AIO[2]	J3	Bi-directional	Programmable input/output line

Notes:

[1] USB functions are available on BC212015 only.

[2] USB functions can be software mapped to any PIO terminal.

[3] All PIO's are configured as inputs with weak pull-downs at reset.

Power Supplies and Control	Ball	Pad Type	Description
VDD_RADIO	D1 H3	VDD	Positive supply connection for RF circuitry
VDD_VCO	H1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	K1	VDD	Positive supply for analogue circuitry
VDD_CORE	A8	VDD	Positive supply for internal digital circuitry
VDD_PIO	A1	VDD	Positive supply for PIO and AUX DAC
VDD_PADS	A10	VDD	Positive supply for all other input/output
VDD_MEM	D11	VDD	Positive supply for external memory port and AIO
VSS_RADIO	E2 F2 G2	VSS	Ground connections for RF circuitry
VSS_VCO	J2 H2	VSS	Ground connections for VCO and synthesiser
VSS_ANA	L3 K2	VSS	Ground connections for analogue circuitry
VSS_CORE	A9	VSS	Ground connection for internal digital circuitry
VSS_PIO	A2	VSS	Ground connection for PIO and AUX DAC
VSS_PADS	A11	VSS	Ground connection for input/output except memory port
VSS_MEM	C11	VSS	Ground connection for external memory port
VSS	C7	VSS	Ground connection for internal package shield

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE	-0.40V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_MEM	-0.40V	3.60V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating Temperature Range[1]	-40°C	105°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE	1.70V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_MEM	1.70V	3.60V

Note:

[1] The device functions across this range. See long form data book for guaranteed performance over temperature.

Input/Output Terminal Characteristics				
Digital Terminals	**Min**	**Typ**	**Max**	**Unit**
Input Voltage				
V_{IL} input logic level low (VDD=3.0V)	-0.4	-	+0.8	V
(VDD=1.8V)	-0.4	-	+0.4	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage				
V_{OL} output logic level low, (I_O = 4.0mA), VDD=3.0V	-	-	0.2	V
V_{OL} output logic level low, (I_O = 4.0mA), VDD=1.8V	-	-	0.4	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=3.0V	VDD-0.2	-	-	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=1.8V	VDD-0.4	-	-	V
Input and Tristate Current with:				
Strong pull-up	-100	-20	-10	µA
Strong pull-down	+10	+20	+100	µA
Weak pull-up	-5	-1	0	µA
Weak pull-down	0	+1	+5	µA
I/O pad leakage current	-1	0	+1	µA
C_I Input Capacitance	2.5	-	10	pF

Input/Output Terminal Characteristics (Continued)				
USB Terminals	**Min**	**Typ**	**Max**	**Unit**
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD_PADS	V
V_{IH} input logic level high	0.7VDD_PADS	-	-	V
Input leakage current				
VSS_PADS< VIN< VDD_PADS[1]	-1	-	1	µA
C_I Input capacitance	2.5	-	10	pF
Output levels to correctly terminated USB Cable				
V_{OL} input logic level low	0	-	0.2	V
V_{OH} input logic level high	2.8	-	VDD_PADS	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_MEM are at 3.0V unless shown otherwise

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

(1) Internal USB pull-up disabled

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC, 8-Bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	8	Bits
Average output step size[1]	12.5	14.5	17	mV
Output Voltage		monotonic[1]		
Voltage range (I_O=0)	VSS_PIO	-	VDD_PIO	V
Current range	-10	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	+1	µA
Offset	-220	-	+120	mV
Integral non-linearity[1]	-2	-	+2	LSB
Starting time (50pF load)	-	-	10	µs
Settling time (50pF load)	-	-	5	µs

Input/Output Terminal Characteristics (Continued)				
Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency [2]	8.0	-	32.0	MHz
Digital trim range [3]	5	6.2	8	pF
Trim step size [3]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance [4]	870	1500	2400	Ω

Input/Output Terminal Characteristics (Continued)				
Power-on reset	**Min**	**Typ**	**Max**	**Unit**
VDD falling threshold	1.40	1.50	1.60	V
VDD rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_MEM are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

[1] Specified for an output voltage between 0.2V and VDD_PIO -0.2V

[2] Integer multiple of 250kHz.

[3] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[4] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF

Radio Characteristics, VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-83	-	≤-70	dBm
	2.441	-	-85	-		dBm
	2.480	-	-85	-		dBm
Maximum received signal at 0.1% BER	2.402	-	-	-	≥-20	dBm
	2.441	-	-	-		dBm
	2.480	-	-	-		dBm
RF transmit power [1]	2.402	-	6.0	-	-6 to +4[2]	dBm
	2.441	-	6.0	-		dBm
	2.480	-	6.0	-		dBm
Initial carrier frequency tolerance	2.402	-	12	-	±75	kHz
	2.441	-	10	-		kHz
	2.480	-	9	-		kHz
20dB bandwidth for modulated carrier	2.402	-	879	-	≤1000	kHz
	2.441	-	816	-		kHz
	2.480	-	819	-		kHz
RF power control range		-	35	-	≥16	dB
RF power range control resolution		-	1.8	-	-	dB

Notes:

[1] BlueCore2-External firmware maintains the transmit power to be within the Bluetooth specification v1.1 limits.

[2] Class 2 RF transmit power range, Bluetooth specification v1.1

Average Current Consumption [1]		
VDD=1.8V Temperature = 20°C		
Mode	**Avg**	**Unit**
SCO connection HV3 (40ms interval Sniff Mode) (Slave)	26.0	mA
SCO connection HV3 (40ms interval Sniff Mode) (Master)	26.0	mA
SCO connection HV1 (Slave)	53.0	mA
SCO connection HV1 (Master)	53.0	mA
ACL data transfer 115.2kbps UART (Master)	15.5	mA
ACL data transfer 720kbps USB (Slave)	53.0	mA
ACL data transfer 720kbps USB (Master)	53.0	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	4.0	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.5	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.6	mA
Standby Mode (Connected to host, no RF activity)	0.047	mA
Deep Sleep Mode[2]	20.0	µA

Notes:

[1] Current consumption is the sum of both BC212013B or BC212015B and the flash.

[2] Current consumption is for the BC212013B and BC212015B devices only.

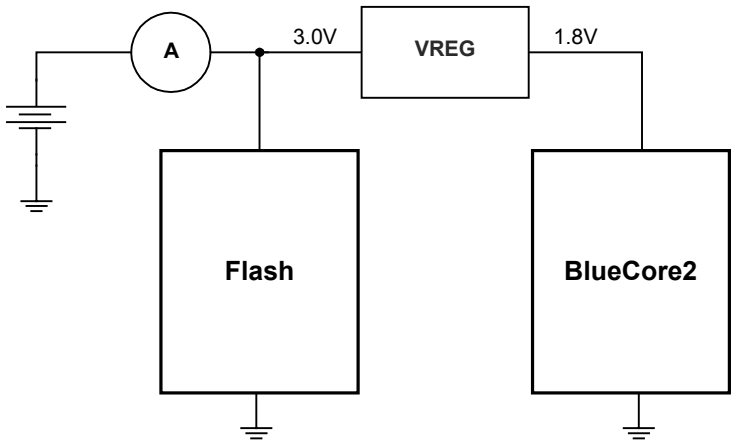


Figure 4.1: Current Measurement Circuit

5 Device Diagram

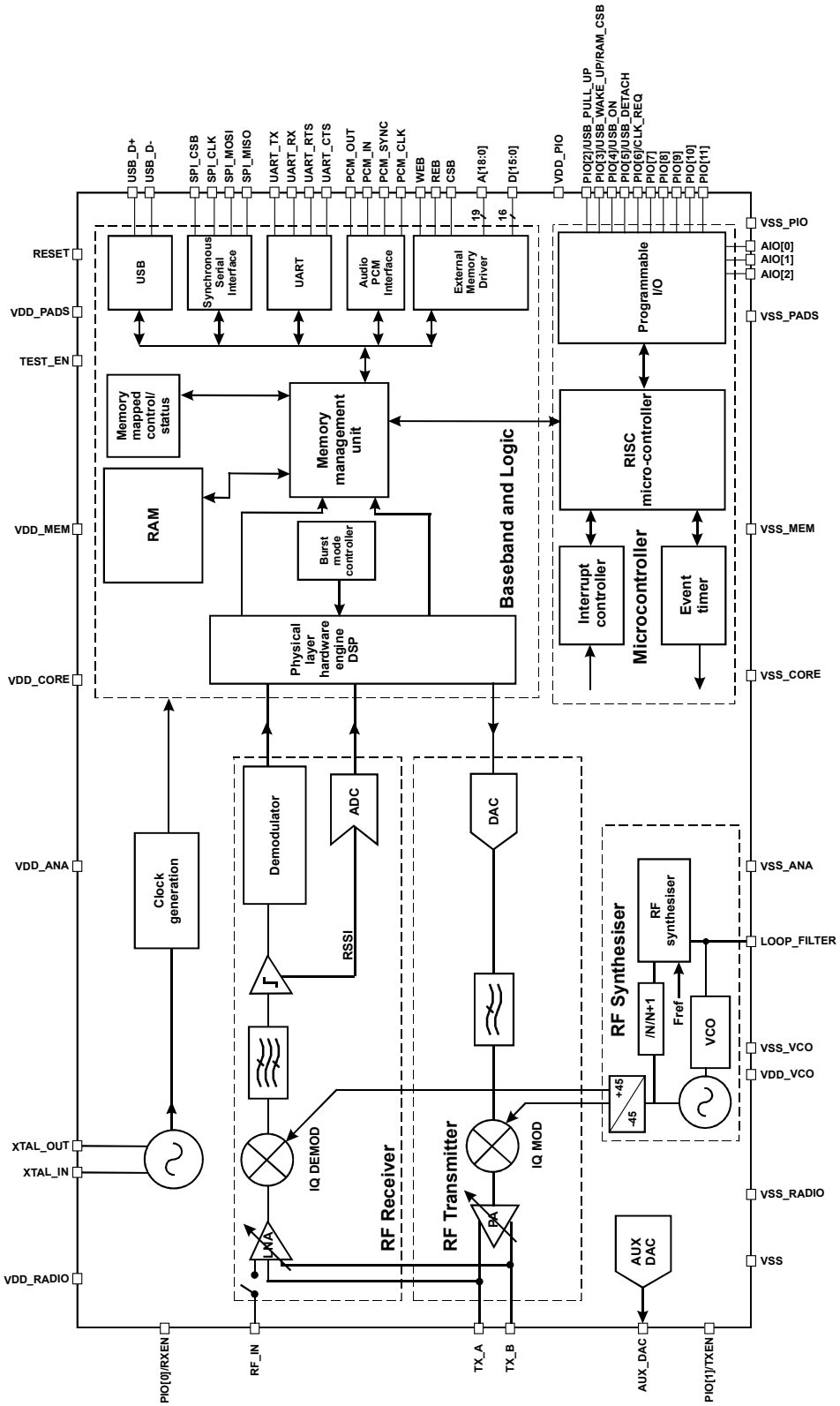


Figure 5.1: BlueCore2-External Device Diagram

6 Description of Functional Blocks

6.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore2-External to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

6.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

6.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

6.2 RF Transmitter

6.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.

6.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore2-External to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

6.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes or LC resonators.

6.4 Baseband and Logic

6.4.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

6.4.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

6.4.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

6.4.4 RAM

32Kbytes of on-chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

6.4.5 External Memory Driver

The External Memory Driver interface can be used to connect to the external Flash memory and also to the optional external RAM for memory intensive applications.

6.4.6 USB

This is a full speed Universal Serial Bus interface for communicating with other compatible digital devices. BlueCore2-External acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

6.4.7 Synchronous Serial Interface

This is a synchronous serial port interface for interfacing with other digital devices. The SPI port can be used for software debugging and for programming the external Flash memory.

6.4.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

6.4.9 Audio PCM Interface

The Audio Pulse Code Modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

6.5 Microcontroller

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit Reduced Instruction Set Computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

6.5.1 Programmable I/O

BlueCore2-External has a total of 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

7 CSR Bluetooth Software Stacks

BlueCore2-External is supplied with Bluetooth stack firmware which runs on the internal RISC microcontroller. This is compliant with the Bluetooth specification v1.1.

The BlueCore2-External software architecture allows Bluetooth processing overheads to be shared in different ways between the internal RISC microcontroller and the host processor. The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

Running the upper stack on BlueCore2-External reduces (or eliminates, in the case of a virtual machine (VM) application) the need for host-side software and processing time. Running the upper layers on the host processor allows greater flexibility.

7.1 BlueCore HCI Stack

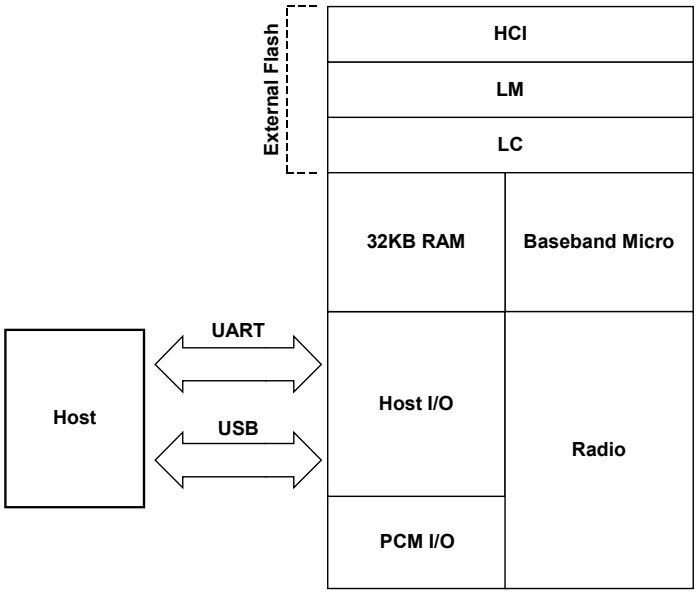


Figure 7.1: BlueCore HCI Stack

In this implementation the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). All upper layers must be provided by the Host processor.

7.1.1 Key Features of the HCI Stack

Standard Bluetooth Functionality

The firmware has been written against the Bluetooth Core Specification v1.1.

- Bluetooth components: Baseband (including LC), LM and HCI
- Standard USB v1.1 and UART (H4) HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2kb/s asymmetric(1)
- Operation with up to 7 active slaves (1)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to 3 SCO links, routed to one or more slaves
- Role switch: can reverse Master/Slave relationship
- All standard SCO voice codings, plus “transparent SCO”
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes
- Standard firmware upgrade via USB (DFU)

The firmware’s supported Bluetooth features are detailed in the standard PICS documents, available from www.csr.com.

Note:
(1) Maximum allowed by Bluetooth specification v1.1.

(2) BlueCore2-External supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.1.

Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth H4 UART Host Transport.
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – "BlueCore Command"), provides:
  - Access to the chip's general-purpose PIO port
  - Access to the chip's Bluetooth clock – this can help transfer connections to other Bluetooth devices
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers – these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable – a simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code.
- A block of BCCMD commands provides access to the chip's "persistent store" configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART "break" condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data – normally used to wake the host from a deep sleep state
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules.
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART.
- A block of "radio test" or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and "RFCOMM builds" (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LED's via the chip's PIO port.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed over HCI (over BCSP). However, a single SCO channel can be routed over the chip's single PCM port (at the same time as routing up to two other SCO channels over HCI). [Future versions of the BC02x firmware will be able to exploit the hardware's ability to route up to three SCO channels through the single PCM port.]

7.2 BlueCore RFCOMM Stack

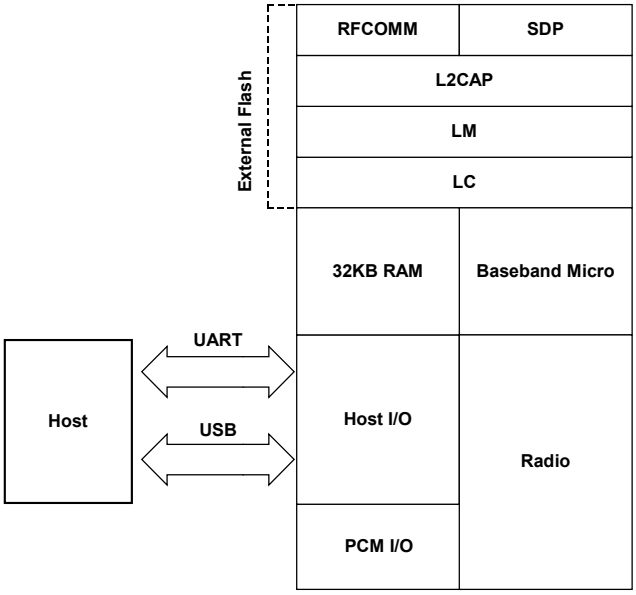


Figure 7.2: BlueCore RFCOMM Stack

In this version of the firmware the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

7.2.1 Key Features of the BlueCore2-External RFCOMM Stack

Interfaces to Host

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350 Kb/s

Security

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

7.3 BlueCore Virtual Machine Stack

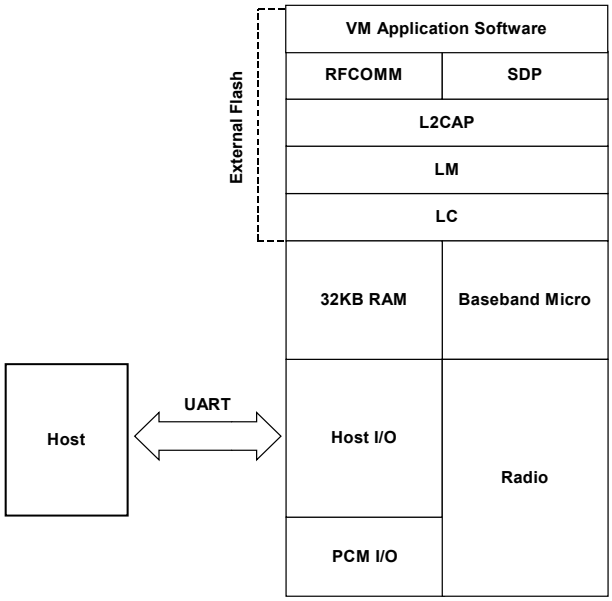


Figure 7.3: Virtual Machine

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab™ software development kit (SDK) supplied with the BlueLab and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

7.4 Host-Side Software

BlueCore2-External can be ordered with companion host-side software:

BlueCore2-PC includes software for a full Windows® 98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with IC hardware described in this document.

BlueCore2-Mobile includes software for a full host-side stack designed for modern ARM based mobile handsets together with IC hardware described in this document.

7.5 Device Firmware Upgrade

BlueCore2-External is supplied with boot loader software which implements a Device Firmware Upgrade (DFU) capability. This allows new firmware to be uploaded to the external Flash memory through BlueCore2-External's UART or USB ports.

7.6 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore2-External, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as ‘C’ source or object code.

7.7 CSR Development Systems

CSR’s BlueLab, Casira and MicroSira development kits are available to allow the evaluation of the BlueCore2-External hardware and software, and as toolkits for developing on-chip and host software.

8 External Interfaces

8.1 Transmitter/Receiver Inputs and Outputs

Terminals TX_A and TX_B form a balanced current output. They require a DC path to VDD and should be connected through a balun to the antenna. The output impedance is capacitive and remains constant, irrespective of whether the transmitter is enabled or disabled. For Class 2 operation these terminals also act as differential receive input terminals with an internal TX/RX switch.

For Class 1 operation the RF_IN ball is provided which is single-ended. A swing of up to 0.5V root mean squared (rms) can be tolerated at this terminal. An external antenna switch can be connected to RF_IN.

8.2 Asynchronous Serial Data Port (UART) and USB Port

UART_TX, UART_RX, UART_RTS and UART_CTS form a conventional asynchronous serial data port. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signalling levels are 0V and VDD_PADS and are inverted with respect to the signaling on an RS232 cable. The interface is programmable over a variety of bit rates; no, even or odd parity; one or two stop bits and hardware flow control on or off. The default condition on power-up is pre-assigned in the external Flash.

The maximum UART data rate is 1.5 MBaud. Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and is active low. UART_CTS is an input and is active low. These signals operate according to normal industry convention.

The port carries a number of logical channels: HCI data (both SCO and ACL), HCI commands and events, L2CAP API, RFCOMM API, SDP and device management. For the UART, these are combined into a robust tunnelling protocol, BlueCore Serial Protocol (BCSP), where each channel has its own software flow control and cannot block other data channels. In addition, the Bluetooth specification v1.1, HCI UART Transport Layer (part H4) format is supported.

Full speed USB (12Mbit/s) is supported in accordance with the Bluetooth specification v1.1, HCI USB Transport Layer (H2). USB_D+ and USB_D- are available on dedicated terminals. Both Open Host Controller Interface (OHCI) and Universal Host Controller Interfaces (UHCI) are supported.

The firmware in Flash can be downloaded through the USB or UART ports by DFU if the CSR supplied boot loader is first programmed. Firmware shipped with BlueCore2-External includes security features to prevent misuse of this upgrade facility.

8.3 PCM CODEC Interface

PCM_OUT, PCM_IN, PCM_CLK and PCM_SYNC carry up to three bi-directional channels of voice data, each at 8ksamples/s. The format of the PCM samples can be 8-bit A-law, 8-bit μ-law, 13-bit linear or 16-bit linear. The PCM_CLK and PCM_SYNC terminals can be configured as inputs or outputs, depending on whether BlueCore2-External is the Master or Slave of the PCM interface.

BlueCore2-External interfaces directly to PCM audio devices includes the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- BlueCore2-External is also compatible with the Motorola SSI™ interface

8.4 Serial Peripheral Interface

BlueCore2-External is a slave device that uses terminals SPI_MOSI, SPI_MISO, SPI_CLK and SPI_CSB. This interface is used for program emulation/debug and IC test. It is also the means by which the external Flash may be programmed ‘in situ’ before any 'boot' program is loaded.

Note:

The designer should be aware that no security protection is built into the hardware or firmware associated with this port, so the terminals should not be permanently connected in a PC application.

8.5 Parallel PIO Port

Fifteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:0] are powered from VDD_PIO and AIO[2:0] are powered from VDD_MEM. PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use. Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore2-External is provided from a system application specific integrated circuit (ASIC). PIO[2] can be configured as a chip select for additional external RAM.

BlueCore2-External has three general purpose analogue interface pins, AIO[0], AIO[1] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip bandgap reference voltage, the other two may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the bandgap reference voltage and a variety of clock signals; 48, 24, 16, 8 MHz and the Xtal clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V).

These pins may also be configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage levels are determined by VDD_MEM which may be either 1.8V or 3.0V, dependant upon the external flash.

8.6 I^2C Interface

PIO[3] and PIO[2] can be used to form a Master I^2C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

9 Schematic

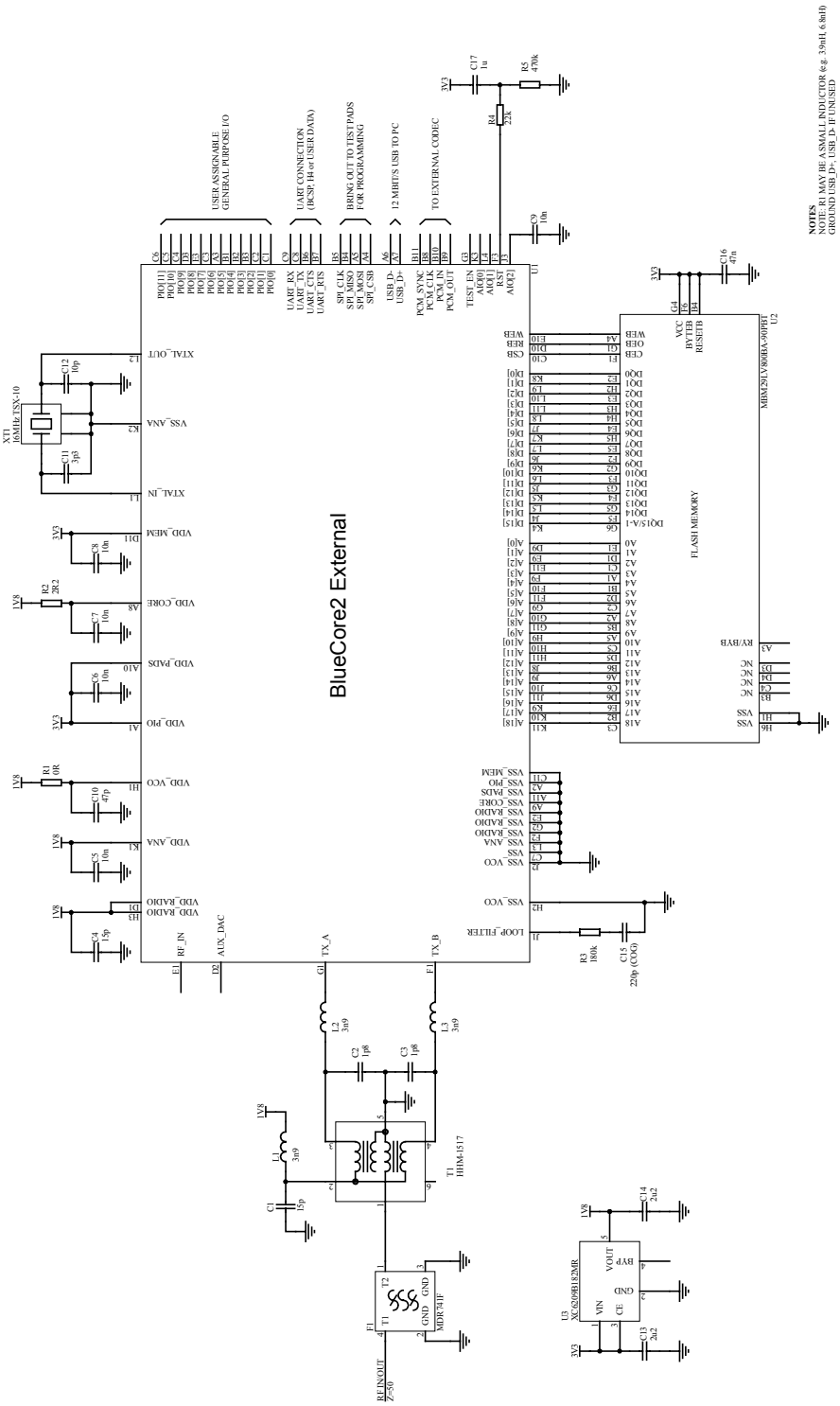


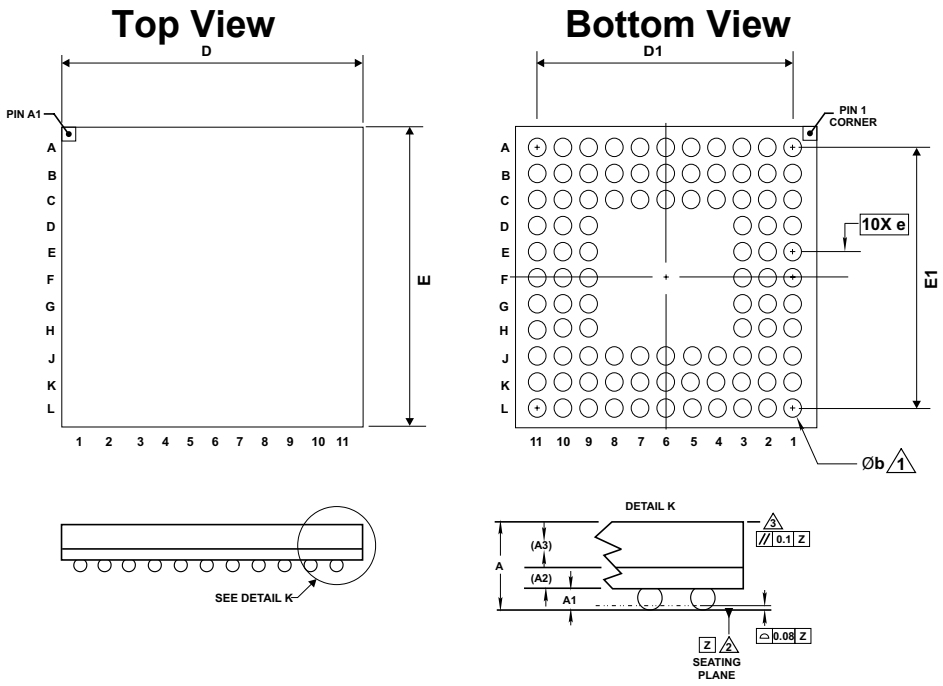
Figure 9.1: Example Application Circuit

Note:

For a full BlueCore2-External reference design contact your local CSR representative.

10 Package Dimensions

10.1 96-Ball VFBGA

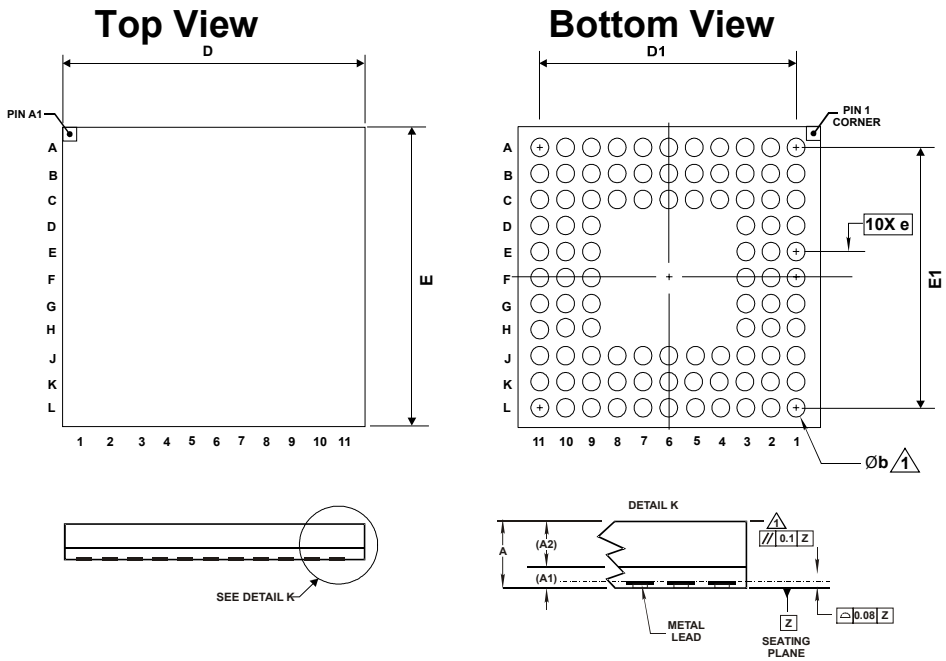


BC212015DN and BC212013DN 8x8x1mm VFBGA			
DIM	MIN	MAX	NOTES
A	0.8	1	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.2	0.3	
A2	0.22 REF		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3	0.45 REF		
b	0.25	0.35	3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
D	8 BSC		
E	8 BSC		
e	0.65 BSC		
D1	6.5 BSC		
E1	6.5 BSC		
VFBGA 96 BALLS 8X8X1mm (JEDEC MO-225)			UNIT: MM

BC212015EN and BC212013EN 6x6x1mm VFBGA			
DIM	MIN	MAX	NOTES
A	0.8	1	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.2	0.3	
A2	0.22 REF		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3	0.45 REF		
b	0.25	0.35	3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
D	6 BSC		
E	6 BSC		
e	0.5 BSC		
D1	5 BSC		
E1	5 BSC		
VFBGA 96 BALLS 6X6X1mm (JEDEC MO-225)			UNIT: MM

Figure 10.1: BlueCore2-External VFBGA Package Dimensions

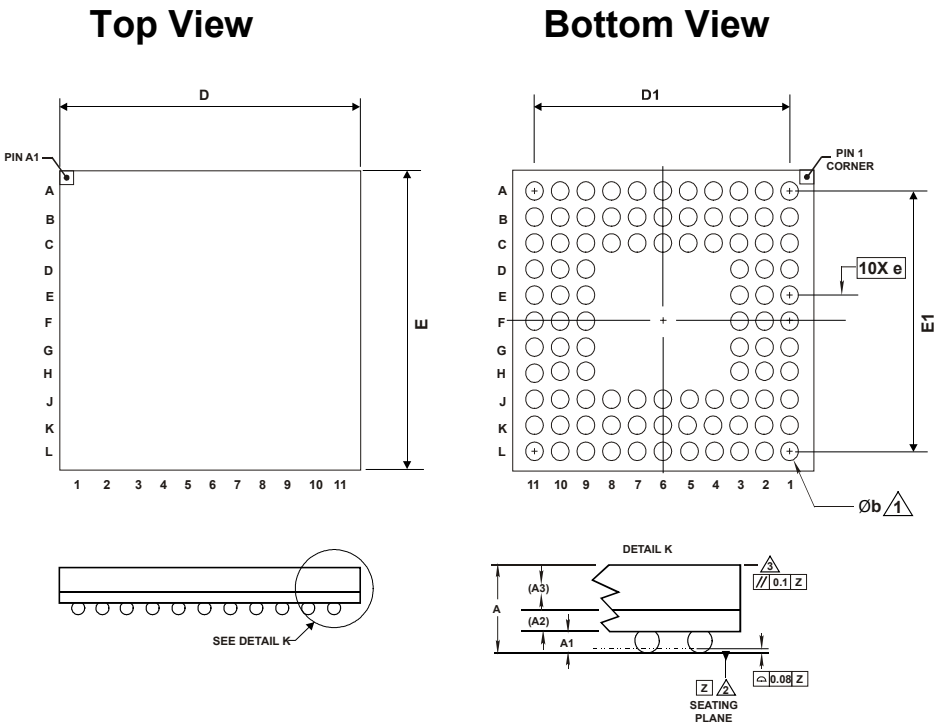
10.2 96-Ball LGA



BC212015LN and BC212013LN 6x6x0.6mm LGA				
DIM	MIN	TYP	MAX	NOTES
A		0.6	0.65	⚠1 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
A1		0.22 REF		
A2	0.32	0.37	0.42	
b	0.15		0.25	
D		6 BSC		
E		6 BSC		
e		0.5 BSC		
D1		5 BSC		
E1		5 BSC		
LGA 96 BALLS 6X6X0.6mm (JEDEC MO-222)				UNIT: MM

Figure 10.2: BlueCore2-External LGA Package Dimensions

10.3 96-Ball LFBGA



BC212015BN 10x10x1.4mm LFBGA			
DIM	MIN	MAX	NOTES
A	---	1.4	1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.3	0.4	
A2	0.26 REF		2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3	0.8 REF		
b	0.35	0.45	3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
D	10 BSC		
E	10 BSC		
e	0.8 BSC		
D1	8 BSC		
E1	8 BSC		
LFBGA 96 BALLS 10X10X1.4mm (JEDEC MO-210)			UNIT: MM

Figure 10.3: BlueCore2-External LFBGA Package Dimensions

11 Ordering Information

BlueCore2-External Standard Packaging Options

Firmware: HCI/on-chip RFCOMM

Interface Version	Package			Order Number
	Type	Size (mm)	Shipment Method	
UART	96-ball VFBGA	6x6x1	Tape and reel	BC212013BEN-E4
	96-ball VFBGA Lead Free	6x6x1	Tape and reel	BC212013BRN-E4
	96-ball LGA	6x6x0.65	Tape and reel	BC212013BLN-E4
UART and USB	96-ball LFBGA	10x10x1.4	Tape and reel	BC212015BN-E4
	96-ball VFBGA	8x8x1	Tape and reel	BC212015BDN-E4
	96-ball VFBGA	6x6x1	Tape and reel	BC212015BEN-E4
	96-ball VFBGA Lead Free	6x6x1	Tape and reel	BC212015BRN-E4
	96-ball LGA	6x6x0.65	Tape and reel	BC212015BLN-E4

Additional Software Options: BlueCore2-External is available with additional software options. These are shown in table below. To order these versions attach the appropriate order code to the main packaging order number, e.g., BC212013BDN-E4-0112.

Additional Software Options

Product Family	Description	Order Code
BlueCore2-Ext-PC	Bluetooth for Windows v1.2 English	-0112
BlueCore2-Ext-Embedded	Bluetooth Embedded v1.2	-4012
BlueCore2-Ext-BCHS[1]	BlueCore Host Software	-8010

Note:

[1] Only available for UART interface versions.

Packaging Option
2kpcs Taped and Reeled

12 Contact Information

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Seoul 151-767
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To contact a CSR representative, go to www.csr.com/contacts.htm

13 Document References

Document References	Version
Specification of the Bluetooth system	v1.1, 22 February 2001
Universal Serial Bus Specification	v1.1, 23 September 1998

14 Acronyms and Definitions

Term:	Definition:
BlueCore	Group term for CSR's range of Bluetooth chips.
Bluetooth	A set of technologies providing audio and data transfer over short-range radio connections
ACL	Asynchronous Connection-Less. A Bluetooth data packet.
AC	Alternating Current
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BGA	Ball Grid Array
BIST	Built-In Self-Test
BOM	Bill of Materials. Component part list
BMC	Burst Mode Controller
BSC	Basic. Represents theoretical exact dimension or dimension target.
C/I	Carrier Over Interferer
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CSB	Chip Select
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
FSK	Frequency Shift Keying
GCI	General Circuit Interface. Standard synchronous 2B+D ISDN timing interface
GSM	Global System for Mobile communications
HCI	Host Controller Interface
Host	Application's microcontroller
Host Controller	Bluetooth integrated chip
HV	Header Value
IQ Modulation	In-Phase and Quadrature Modulation
IAC	Inquiry Access Code
IF	Intermediate Frequency
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksamples/s	kilosamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LGA	Land Grid Array
LNA	Low Noise Amplifier
LSB	Least-Significant Bit
µ-law	Encoding standard
MMU	Memory Management Unit
MISO	Master In Serial Out
OHCI	Open Host Controller Interface

PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PDA	Personal Digital Assistant
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Not Read enable
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
ROM	Read Only Memory
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SMS	Short Message Service
SOC	System On Chip
SPI	Serial Peripheral Interface
SPP	Serial Port Profile
SRAM	Static Random Access Memory
SS	Supplementary Services
SSI	Signal Strength Indication
SSL	Secure Sockets Layer
SUT	System Under Test
SW	Software
SWAP	Shared Wireless Access Protocol
TA	Terminal Adaptor
TAE	Terminal Adaptor Equipment
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable
www	world wide web

Status of Information

The progression of CSR Product Data Sheets follows the following format:

Advance Information

Information for designers on the target specification for a CSR product in development.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Final pinout and mechanical dimensions. All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

The status of this Data Sheet is **Production Information.**

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CSR Ltd reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

15 Record of Changes

Date:	Revision:	Reason for Change:
12 SEPT 2001	a	Original publication of document.
20 OCT 2001	b	Application information added.
27 MAR 2002	c	Amendments made to ordering codes.
5 MAY 2002	d	Production information added.
28 JUNE 2002	e	RF characteristics, current consumption and 10x10 packaging information added in line with BlueCore2-External Data Book.

BlueCore™2-External Product Data Sheet

BlueCore™2-External Product Data Sheet

BC212015-ds-001e

July 2002