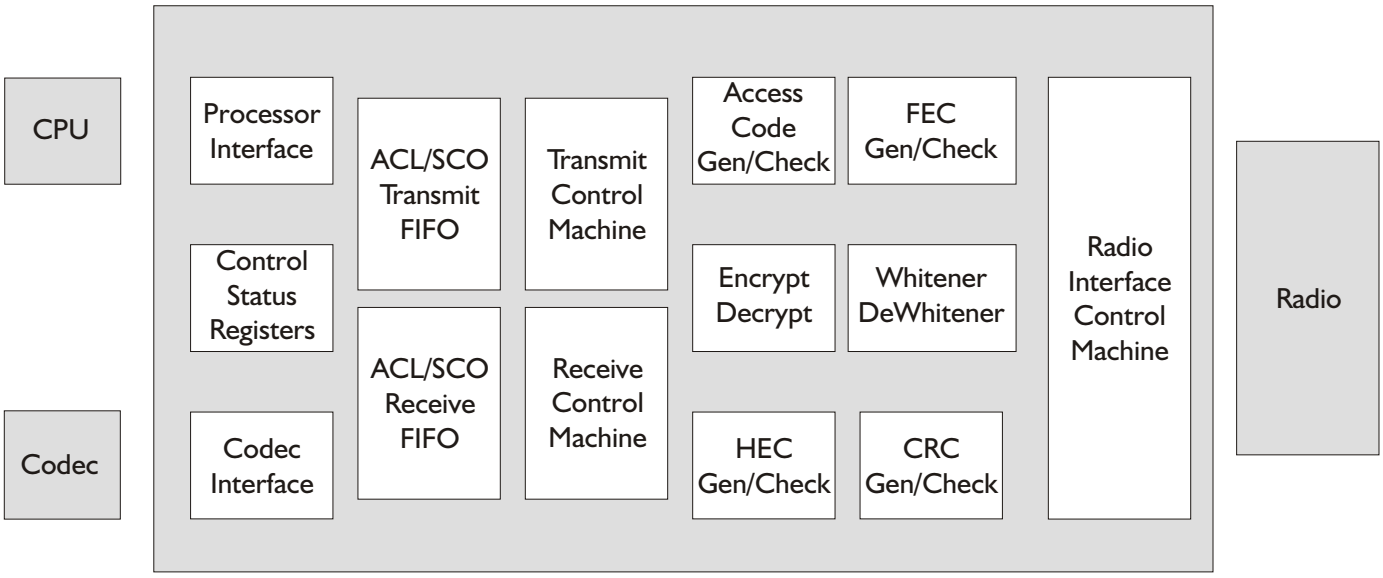
EtherMind Bluetooth™ Baseband Controller



Block Diagram

MindTree's approach to Bluetooth Baseband design provides maximum flexibility to chip vendors without compromising performance parameters such as processor load and memory requirements. Compliant with Bluetooth 1.1 specifications, the Ethermind Baseband Controller is available as silicon proven synthesizable Verilog core with LMP/HCI firmware. The IP can be reconfigured to work with any 8/16/32 bit microcontroller on which LMP/HCI firmware resides and be reconfigured to interface with many Bluetooth radio implementations.

Voice applications can easily be built, as the SCL data transfer is supported in the Ethermind Baseband design itself. The core executes all datapath functions with error detection and correction logic in addition to the management and control of the lower layer protocol. The Ethermind Baseband core also manages channel selection and hopping functions, relieving the host processor(s) to manage only the LMP/HCI layer functions. Intelligent radio control ensures low power consumption in addition to alternately low power features of Bluetooth wireless technology.

EtherMind Baseband architecture is flexible enough to support various on-chip FIFOs and sizes to enable optimal custom application designs. With minimum processor load and and chip power consumption, fabless companies can easily customize EtherMind Baseband to develop the lowest foot print SOC design for any target application.

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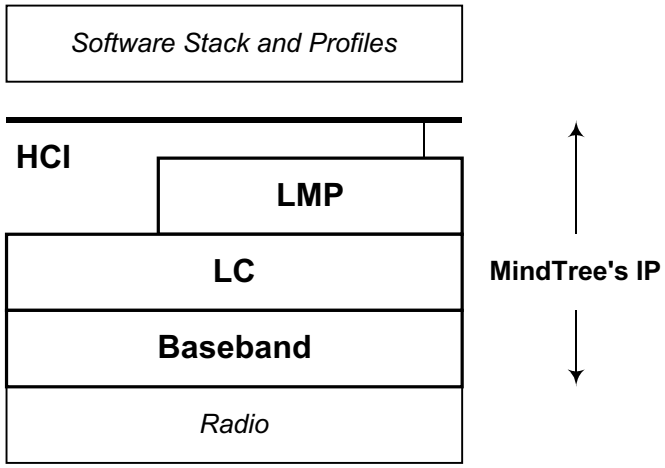
Features

- Bluetooth specification 1.1 compliant
- Technology independent synthesizable Verilog core
- Data rates upto 721Kbps
- Supports all ACL and SCO packets
- Supports Bluetooth security through hardware encryption
- Package composer/decomposer includes FEC, HEC and CRC functions
- Independent FIFOs for slaves, ACL and SCO
- Configurable FIFO sizes
- Generic host interface for microcontrollers
- Codec interface for SCO channels (A-Law, u-Law, CVSD)
- Re-configurable radio interface (Blue RF compliant)
- Supports scatternet functionality
- Supports 3 SCO channels
- LMP 1.1
- HCI 1.1



Deliverables

- RTL synthesizable Verilog core
- Design and verification documents
- Synthesis scripts
- LMP & HCI source code and design documentation
- Test environment
- Golden test cases (mandatory and optional as mentioned by Bluetooth SIG)
- Application documents
- User manual