ALATEK AL8255
IP Core Application Note

December 10, 1999
(version 1.0)

General Information

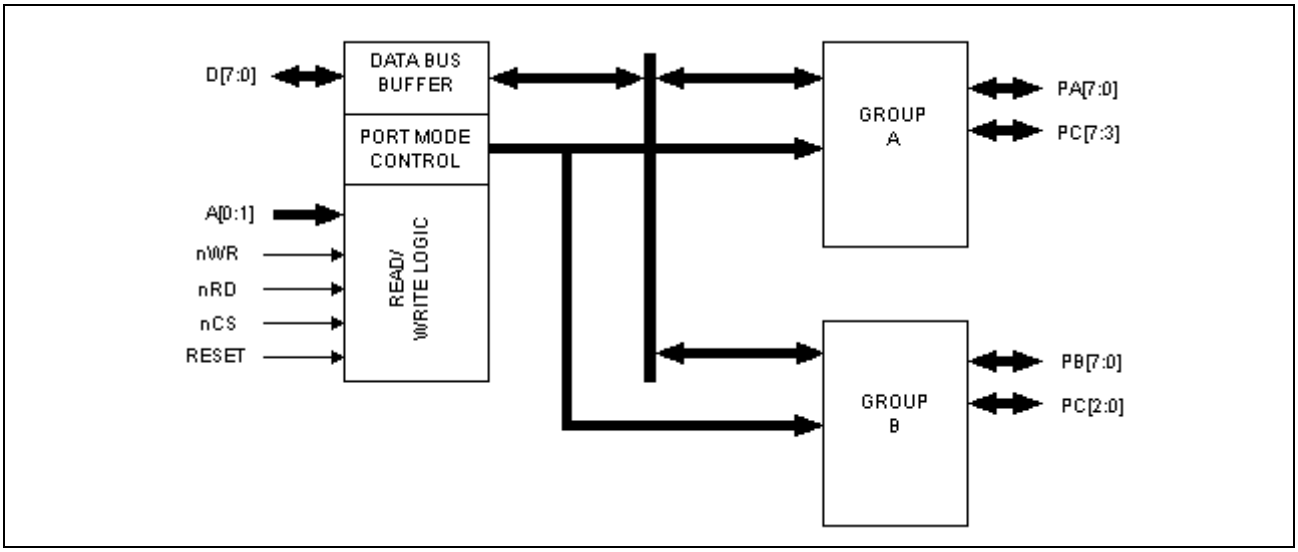
The AL8255 core is the VHDL model of the Intel™ 8255 Programmable Peripheral Interface device designed for use in Intel microcomputer systems. It reduces the external logic normally needed to interface peripheral devices. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus.

Features

- Functionally based on the Intel 8255A device
- Three 8-bit peripheral ports: PA, PB, PC
- Three programming modes for peripheral ports
- Total of 24 programmable I/O lines
- 8-bit bidirectional system data bus with standard microprocessor interface controls

Block Diagram

The basic structure of the AL8255 core is shown below:



The Core Contents

A. Behavioral

The behavioral model is designed for the functional simulation only and it cannot be synthesized or implemented into FPGAs. The behavioral model contains the following files:

- **AL8255.vhd** - the top level file of the behavioral model

B. Synthesizable

See the Deliverables section of this document for further details.

C. Test Vectors

See the Deliverables section of this document for further details.

The Core Interface

The pinout of the AL8255 core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the table.

Signal Name	Signal Direction	Polarity	Description
CS	IN	LOW	Chip Select
RD	IN	LOW	Read Control
RESET	IN	HIGH	Reset
WR	IN	LOW	Write Control
A[1:0]	IN	-	Address
D[7:0] 1)	INOUT	-	Data Bus
PA[7:0] 1)	INOUT	-	Port A
PB[7:0] 1)	INOUT	-	Port B
PC[7:0] 1)	INOUT	-	Port C

NOTES:

1. Each bi-directional pin is defined in the core interface as three separated VHDL ports. Optionally, using the VHDL Interface (See the Deliverables section of this document for further details), it can be merged to one bi-directional VHDL port.

Implementation Data

The core has been synthesized and implemented to different types of reprogrammable devices. The model has been verified using the simulation environment and tested on the real hardware.

Software				
Synthesis Tool	Synopsys FPGA Express™ build 2.1.3.3220			
Implementation Tools	Xilinx Foundation™ 2.1i SP2, Altera MAX+plusII™ 9.21, Quartus™ 1.0 A			
Verification Tool	Active-HDL™ 3.5 build 437			
Hardware				
Vendor	**Xilinx**		**Altera**	
Device Family	4K	Virtex™	FLEX™ 10K	APEX™ 20K
Target Device	XC4062XLA-9	XCV300-4	EPF10K100-1	APEX20
Area*)	90CLBs (3%)	99Slices (3%)	197LCs (34%)	soon come
System Clock f_{max}	53MHz	57MHz	97MHz	soon come

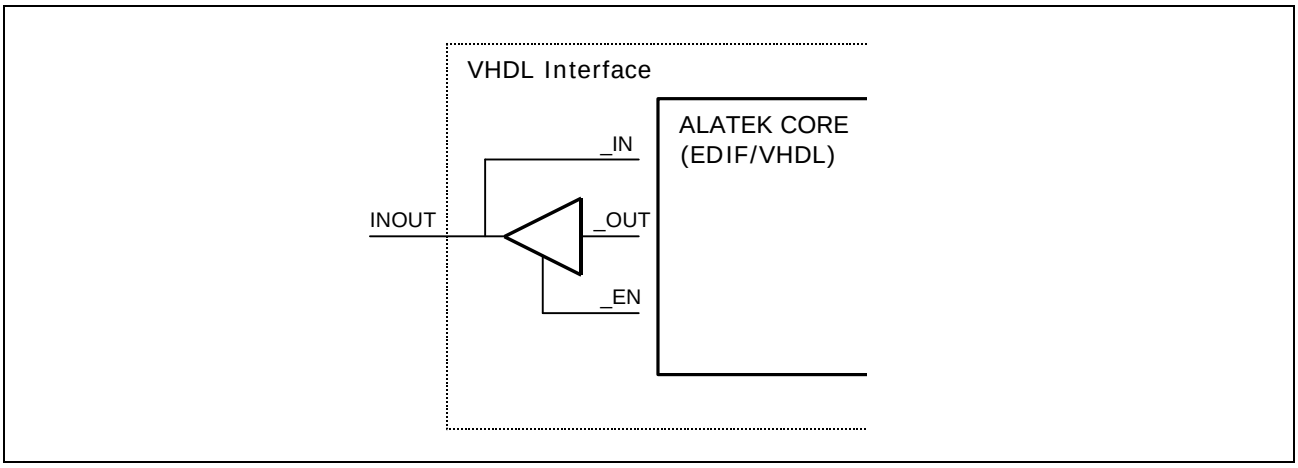
*) with RAM and ROM implemented

Deliverables

After you request the desired compiled synthesizable core, ALATEK delivers the following files:

- Both technology-dependent EDIF (AL8255_CORE.EDN) and VHDL (AL8255_CORE.VHD) netlists
- ALATEK VHDL Interface (AL8255.VHD)
- User-Guide and Application Notes
- Sample designs

Usually ALATEK delivers both EDIF and VHDL netlists for customers who order the synthesizable model. The EDIF netlist is used for the place and route process and VHDL is the post-synthesis netlist used for the simulation only. Of course, both netlists are technology-dependent, because they are created after the synthesis where the customer needs to specify a vendor, target family, etc.
ALATEK provides optionally a VHDL interface for its synthesizable models for these customers who need bi-directional ports in the core interface. See the picture below:



ALATEK can provide also a set of VHDL test benches for their cores. Usually they are sold at the additional charge.

Source codes are sold on a case-by-case basis.