TCP/IP PROTOCOL STACK LSI S7600A

SII-designed iChip S-7600A, by using low power CMOS design, contains TCP/IP Protocol Stacks that act as an accelerator between MPU and Internet or network which uses TCP/IP protocol.

iChip S7600A -- designed to provide Internet connectivity to devices using popular microcontrollers -- provides the functionality necessary for remote management and monitoring applications, portable email, Internet downloads, network access, and much more.

iChip S7600A is a completely self-contained, drop-in solution for any device requiring networking connectivity and will provide a high connect speed with low power consumption -- integrating full TCP/IP, PPP, and UDP protocols, and 10K of on-chip SRAM for those protocol supports.

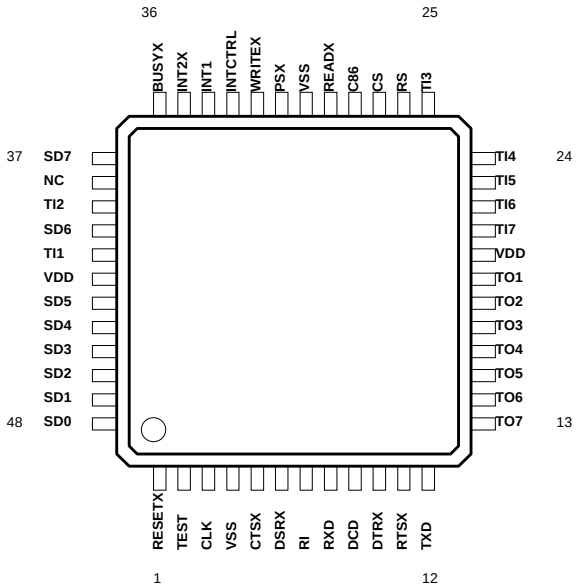
The chip is based upon iReady's Internet Tuner® technology.

■ Features

- TCP/IP ver.4 / UDP/ PPP
- 2 General sockets
- Low clock rate bit-rate x 4
- Low power consumption less than 3 mW at 256 kHz operating speed
- 68/80(MOTO/Intel) MPU bus interface
- UART Interface
- Wide operating voltage range 2.4~3.6V
- Stand-by mode

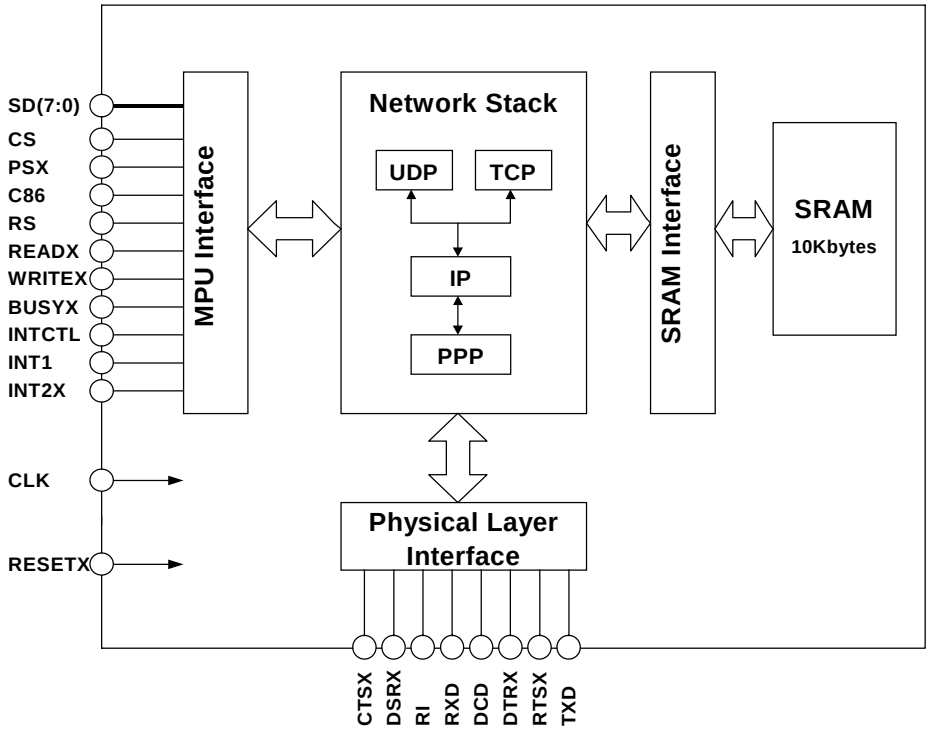
■ Pin Assignment

Figure 1



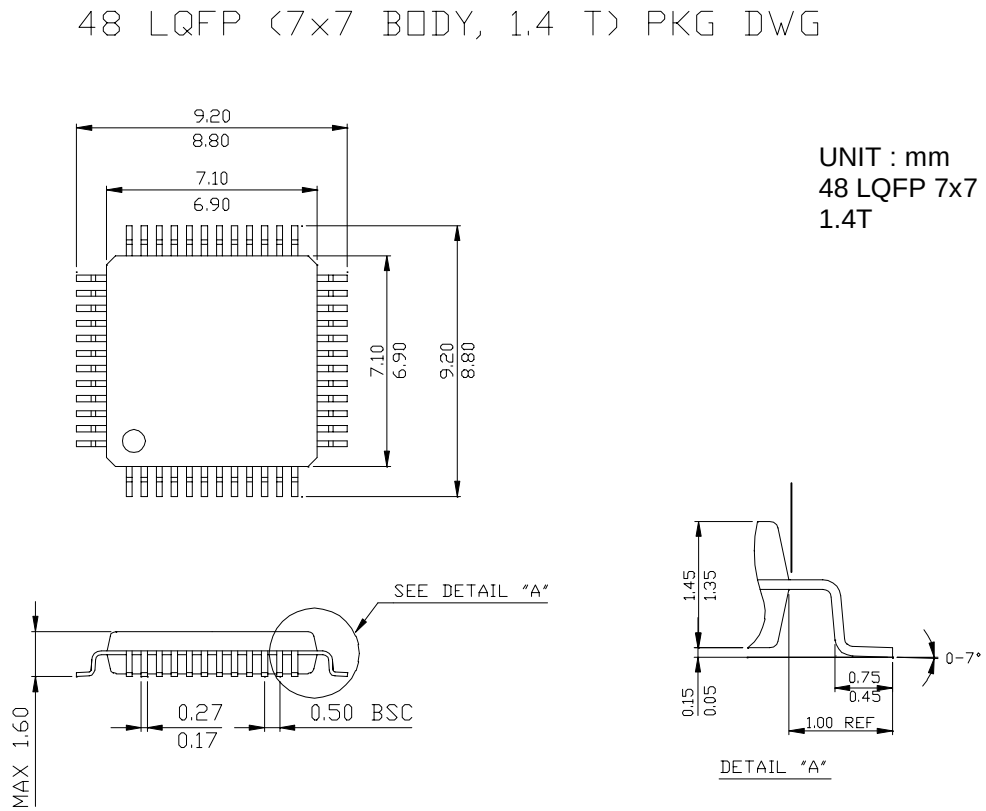
■ Block Diagram

Figure 2



■ Dimensions

Figure 3



■ Function of Each Pin

Table 1 Function of Each Pin

Name	I/O	Description
VDD1,VDD2	-	Positive power supply
VSS1,VSS2	-	GND potential
RESETX	I	Reset input
TEST, TI1 to TI7	I	Test input (built in pull-down resistor)
TO1 to TO7	O	Test output
CLK	I	Clock input
CTSX	I	Clear to send input
DSRX	I	Data set ready input
RI	I	Ring indicator input
RXD	I	Serial received data input
DCD	I	Data carrier detect input
DTRX	O	Data terminal ready output
RTSX	O	Request to send output
TXD	O	Serial transmit data output
RS	I	Register selection input
CS	I	Chip selection input
C86	I	MPU interface mode selection input(1: 68k mode, 0: x80 mode)
READX	I	x80 mode : read requirement input , 68k mode : enable input
PSX	I	parallel/serial interface selection input
WRITEX	I	x80 mode: write requirement input 68k mode: read/write selection input
INTCTRL	I	INT1/INT2X drive type(CMOS/OD) selection input
INT1	*OT	Interrupt output(active High) from S-7600A chip to MPU
INT2X	*OT	Interrupt output(active Low) from S-7600A chip to MPU
BUSYX	O	busy indicator output
SD7	B	x80/68k mode : data bus Serial mode: serial data input
SD6	B	x80/68k mode : data bus Serial mode: serial clock input
SD5	B	x80/68k mode : data bus Serial mode: serial data output
SD0 to SD4	B	Data bus

*OT: Three-state output

■ Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Storage Temperature	T_{sta}		-40 to +125	°C
Operating Temperature	T_{opr}		-10 to +70	°C
Operating Voltage	V_{DD}	Ta=25°C	-0.3 to 4.0	V
Input Voltage	V_{IN}	Ta=25°C	VSS-0.3 to VDD+0.3	V
Output Voltage	V_{OUT}	Ta=25°C	VSS to VDD	V

■ Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Frequency range	F_{OPR}	Ta=-10 to +70°C	-	0.256	5	MHz	1
Operating voltage range	V_{DD}	Ta=-10 to +70°C	2.4	-	3.6	V	
Input voltage	V_{IN}	Ta=-10 to +70°C	0	-	VDD	V	

Note1: The clock is inputted by CLK pin and needs integer times of the BAUD rate.
(integer tolerance <2%)

■ MPU Interface

Overview

The S-7600A supports two MPU interfaces: parallel and serial. In parallel interface mode, S-7600A can interface with x80 Family MPU or 68k Family MPU.

Table 4 Interface Selection

PSX	CS	RS	READX	WRITEX	BUSYX	C86	SD7	SD6	SD5	SD4 to SD0
H: Parallel x80	CS	RS	READX	WRITEX	BUSYX	L	D7	D6	D5	D4 to D0
H: Parallel 68k	CS	RS	E	R/WX	BUSYX	H	D7	D6	D5	D4 to D0
L: serial	CS	RS	H or L	R/WX	BUSYX	H or L	SI	SCL	SO	Hi-Z

■ Parallel Interface

Setting **PSX** to “H” select the parallel interface. In parallel interface mode the S-7600A can interface with either x80 Family MPU and 68k Family MPU. The desired MPU mode can be selected by setting the **C86** pin to “H” or “L”.

Table 5 Connection Relationship between MPU and Pins

RS	68 Family MPU WRITEX(R/WX)	80 Family MPU		Function
		READX	WRITEX	
1	1	0	1	Read Register
1	0	1	0	Write Register
0	1	0	1	Read Index Register
0	0	1	0	Write Index Register

■ 68k Family MPU Mode

This mode can be selected by pulling the **C86** input pin "H" and the **PSX** input pin "H". In this mode, the address and data are muxed into a single 8-bit bus. All cycles start by placing an address on the bus and setting the **RS** pin to "L". In this mode **WRITEX** signal works as read/write(R/WX) signal and **READX** is the enable (E) signal for 68k Family MPU interface. After the address cycle, the MPU generates a read or writes strobe by setting the **READX** and **WRITEX** pins. The S-7600A MPU interface logic assert a **BUSYX** signal low during data write and read phases. The MPU samples the **BUSYX** bit before starting a new cycle. The can initiate a new cycle if the bit is "H".

■ x80 Family MPU Mode

This mode is selected by pulling the **C86** input pin "L" and the **PSX** input pin "H". In this mode, the address and data are muxed onto a single 8-bit bus. All cycles start with the address placed on the bus. This address is then latched internally on the rising edge of **WRITEX**. The **RS** pin "L" indicates that the **WRITEX** strobe is for the address phase. In the next phase, data is either written or read by generating **WRITEX** or **READX** strobe. The MPU interface logic will assert the **BUSYX** signal after **READX** or **WRITEX** strobes are de-asserted. The **BUSYX** signal is de-asserted after the S-7600A complete a read or writes operation. The MPU samples the **BUSYX** bit before starting a new cycle. The MPU can initiate a new cycle after the **BUSYX** signal gets de-asserted.

■ Serial Interface

This mode is selected by pulling the **PSX** input pin "L". In this mode Bit 6 of the Data Bus is used as the serial clock and bit 5 and 7 are used as Data Input and Data Output. Bit 0 to 4 are high impedance. By pulling **WRITEX** signal to "H" or "L", the MPU performs a read or write operation.

■ Interrupt

The interrupt signal outputs an active level while the interrupt flag is set in the interrupt register in the S-7600A's interrupt register. The interrupt signal returns to an inactive level if the flag clears.

The **INT1** and **INT2X** can be Open Drain or CMOS output depending on the setting of **INTCTL**. The **INT1** and **INT2X** outputs are CMOS if **INTCTL** is "H" otherwise outputs are Open Drain. Table 7 defines the interrupt selection.

Table 7 Interrupt Selection

Interrupt flag	INTCTL	INT1	INT2X
Set	H	H	L
Set	L	H	L
Reset	H	L	H
Reset	L	Hi-Z	Hi-Z

■ S-7600A Register Definitions

Overview

This section covers the S-7600A's API registers. The registers are divided into three types: global, direct and indexed.

Global registers occupy the address space from 0x00 to 0x1D and 0x60 to 0x6F. Direct and indexed registers occupy the configuration space from 0x20 to 0x3F. Indexed registers require the socket index to be set prior to accessing the register.

iAPI Register Map

Table 8 and Table 9 shows the complete iAPI register map for the S-7600A chip. All registers not listed are reserved, and should not be accessed.

Table 8 iAPI Register Map

Add	Register	Bit Definitions							
0x00	Revision	Major Revision Number				Minor Revision Number			
0x01	General_Control	-	-	-	-	-	-	-	SW_RST
0x02	General_Socket_Location	0	0	0	0	0	0	1 S1	1 S0
0x04	Master_Interrupt	-	-	-	-	-	PT_INT	LINK_INT	SOCK_INT
0x08	Serial_Port_Config	S_DAV Loop back Mode	DCD	DSR/ HWFC	CTS	RI	DTR	RTS	SCTL
0x09	Serial_Port_Int	PINT	DSINT	-	-	-	-	-	-
0x0A	Serial_Port_Int_Mask	PINT_EN	DSINT_EN	-	-	-	-	-	-
0x0B	Serial_Port_Data	Serial Data Register							
0x0C - 0x0D	BAUD_Rate_Div	BAUD Rate Divider Registers							
0x10 - 0x13	Our_IP_Address	Our IP Address							
0x1C	Clock_Div_Low	Low Byte for 1 kHz clock divider							
0x1D	Clock_Div_High	High Byte for 1 kHz clock divider							
0x20	Index	Socket index							
0x21	TOS*	Type of Service Field							
0x22	Socket_ Config_Status_Low*	TO	Buff_Empty	Buff_Full	Data_Avail/RST	-	Protocol_Type		
0x23	Socket_Status_Mid*	URG	RST	Term	ConU	TCP State			
0x24	Socekt_Activate	-	-	-	-	-	-	S1	S0
0x26	Socket_Interrupt	-	-	-	-	-	-	I1	I0
0x28	Socket_Data_Avail	-	-	-	-	-	-	DAV1	DAV0

NOTE: 1) Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

2) Indexed registers are signified by an asterisk (*).

Table 9 iAPI Register Map (Continued)

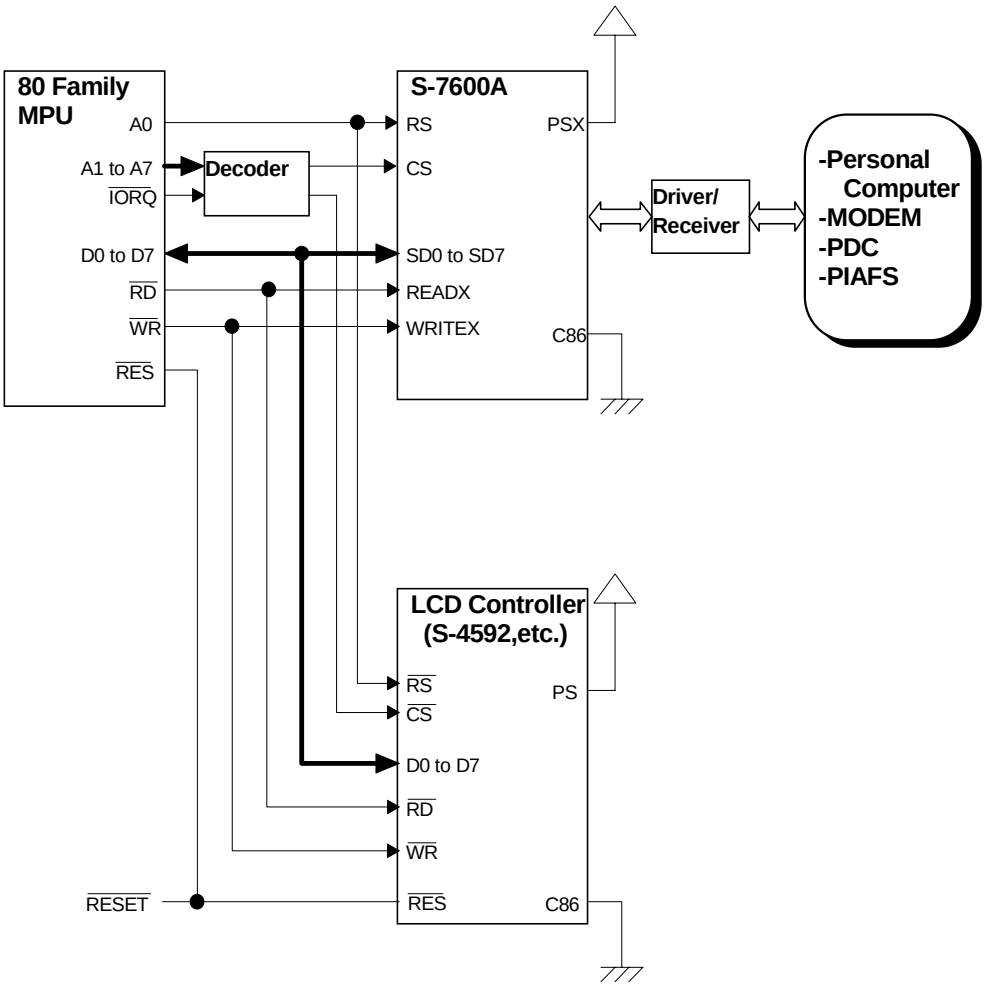
Add	Register	Bit Definitions							
0x2A	Socket_Interrupt_ Mask_Low*	TO_ En	Buff_ Emp_ En	Buff_F ull	Data_ Avail_ En	-	-	-	-
0x2B	Socket_Interrupt_ Mask_High*	URG_En	RST_ En	Term_ En	ConU En	-	-	-	-
0x2C	Socket_Interrupt_Low*	TO	Buff_ Empty	Buff_ Full	Data_ Avail	-	-	-	-
0x2D	Socket_Interrupt_High*	URG	RST	Term	ConU	-	-	-	-
0x2E	Socket_Data*	Socket 8-bit data							
0x30	TCP_Data_Send (WO)*	Any write causes data to be sent							
0x30 - 0x31	Buffer_Out (RO)*	Buffer Out Length							
0x32 - 0x33	Buffer_In (RO)*	Buffer In Length							
0x34 - 0x35	Urgent_Data_Pointer*	Urgent Data Offset Pointer, UDP Datagram Size							
0x36 - 0x37	Their_Port*	Target Port Address							
0x38 - 0x39	Our_Port*	Our Port Address							
0x3A	Socket_Status_High*	-	-	-	-	-	-	-	Snd_ bsy
0x3C - 0x3F	Their_IP_Address*	Target IP Address							
0x60	PPP_Control_Status	PPP_Int	Con_ Val	Use_ PAP	To_ Dis	PPP_ Int_En	Kick	PPP_ En	PPP_ Up / SRset
0x61	PPP_Interrupt_Code	Interrupt Code							
0x62	PPP_Max_Retry	-				PPP Maximum retry			
0x64	PPP_String	Pap user name and password							
0x6F	PPP Test Control	-	-	-	-	Test	Bypass	-	Loop Back

NOTE: 1) Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.
2) Indexed registers are signified by an asterisk (*).

■ Application Example

In case of 80 Family MPU with LCD Controller

Figure 4 80 Family MPU example



Seiko Instruments Inc.
1-8, Nakase, Mihama-ku, Chiba-shi, Chiba 261, Japan
Components Sales Div.
Telephone : +81-43-211-1196 Facsimile : +81-43-211-8032
E-mail : component@sii.co.jp

Seiko Instruments USA Inc.
Electronic Components Div.
2990 W. Lomita Blvd, Torrance, CA 90505, USA
Telephone : +1-909-934-9334 Facsimile : +1-909-975-5699
E-mail : seiko-ecd@salessupport.com
http://www.seiko-usa-ecd.com

S-7600A RELIABILITY TEST DATA (OCTOBER, 1999)

Test	Condition	Duration	Result
High Temp Operation*	$T_A = 125^0C$, $V_{DD} = V_{opr}max$	1,000 hr	0/22
High Temp Bias*	$T_A = 125^0C$, $V_{DD} = 0.9*V_{abs}max$	1,000 hr	0/22
High Humidity & High Temp Bias*	$T_A = 85^0C$, RH == 85%, $V_{DD} = 0.9*V_{abs}max$	1,000 hr	0/22
Unsaturated Pressure Cooker Bias*	$T_A = 85^0C$, RH == 85%, $V_{DD} = 0.9*V_{abs}max$ $P = P_A*2*10^8$	1,000 hr	0/22
High Temp Storage*	$T_A = 150^0C$	1,000 hr	0/22
Low Temp Storage*	$T_A = -65^0C$	1,000 hr	0/22
Temp Cycle*	$T_A = -65^0C$ to $+150^0C$, 30 min each	200 cycles	0/22
Thermal Shock*	$T_A = -65^0C$ to $+150^0C$, 5 min each (liquid to liquid)	100 cycles	0/22
Solderability	$T = 230^0C$	5 seconds	0/11
Lead Strength	Pull force = 1.0 Newton	30 seconds	0/11
Lead Strength (Bending Test)	Force = 0.5 Newton, 45 degree bend a lead	2 X	0/11
ESD	V = 2,000 V, C = 100 pF, R = 1,500 ohms Referenced to V_{DD}/V_{SS}	5 pulses	0/20
Latch Up	+/- 100 mA ($V_{CLAMP} = V_{abs}$ max) 10 ms pulse, $V_{DD} = V_{opr}max$	1 pulse	0/5

Notes:

Result = Number of Failures / Sample Quantity

$V_{abs}max$ = Absolute Maximum Voltage $V_{opr}max$ = Maximum Operating Voltage

"*" indicates that this test is performed after "pre-treatment":

1. High Temp Storage ($+125^0C$) for 24 hours, plus
2. High Humidity (65%) with High Temp Storage ($+85^0C$) for 168 hours, plus
3. Soldering Heat (245^0C) for 10 seconds.