Features

- **USB 2.0 Full Speed Host/Function Processor**
  - **Real-time Host/Function Switching Capability**
  - **Internal USB and System Interface Controllers**
  - **32-bit Generic System Processor Interface with DMA**
  - **Separate TX and RX Buffers for Host and Function Operations**
  - **In-System Firmware Upgrade**
- **Autonomous USB Host Operation without System Processor Intervention**
  - **Device Enumeration**
  - **USB Protocol Management**
  - **Bus Bandwidth Reclamation**
  - **Status Handling**
  - **Control, Bulk, Interrupt and Isochronous Transfers**
- **Full-speed Function Controller**
  - **1 Bi-directional Control Endpoint**
  - **6 Programmable (Maximum Packet Size and Endpoint Type) Endpoints**
  - **Control, Interrupt, Bulk and Isochronous Transfer Support**
  - **Automatic Retry for Non-Isochronous Endpoints**
- **Integrated USB Firmware**
  - **Easy-to-use, ANSI C Compliant API USB Device Driver Development**
  - **Embedded, OS Agnostic USB Host Stack**
  - **Embedded System Interface Controller Driver**
  - **Embedded USB Hub Driver**
- **6 MHz Operation**
- **1.8 V and 3.3 V Operation**
- **100-pin LQFP Package**

Description

Atmel's AT43USB370 is a USB 2.0 compliant, dual-role, full-speed Host/Function processor designed specifically to enable point-to-point USB connectivity for embedded devices. It features an integrated USB host stack, a system interface driver, on-chip USB signaling hardware, 32-bit generic system processor interface with DMA support, and on-the-fly host/function switching capability.

The on-chip USB hardware features a USB transceiver, a serial interface engine (SIE), a SIE controller, and an SOF generation block. It supports the physical and data link layer of the USB protocol whereas the USB transaction layer is implemented in firmware.

In host mode, the integrated USB firmware consists of the Host USB Controller Driver (HUSBCD) running on the USB Controller (USBC) and the Host System Interface Controller Driver (HSICD) resident on the System Interface Controller (SIC). The HUSBCD provides complete USB protocol management including device enumeration, transaction management, scheduling and frame management, and bus reclamation. The HSICD serves as an interface between the HUSBCD and applications resident on the external system processor. It handles all of the high-level data flow management during a USB transaction. Together, the HUSBCD and the HSICD deliver complete USB host operations autonomously, without the intervention of the system processor.

USB 2.0 Full-Speed Host/Function Processor

AT43USB370

Preliminary

Rev. 3340A–USB–5/12/03

The AT43USB370 communicates with the external system processor through its generic 32-bit host processor interface. This system interface contains 2 Kbytes of FIFO and a DMA engine designed to ensure maximum bus utilization. The automatic USB retry mechanism minimizes data traffic across the system interface.

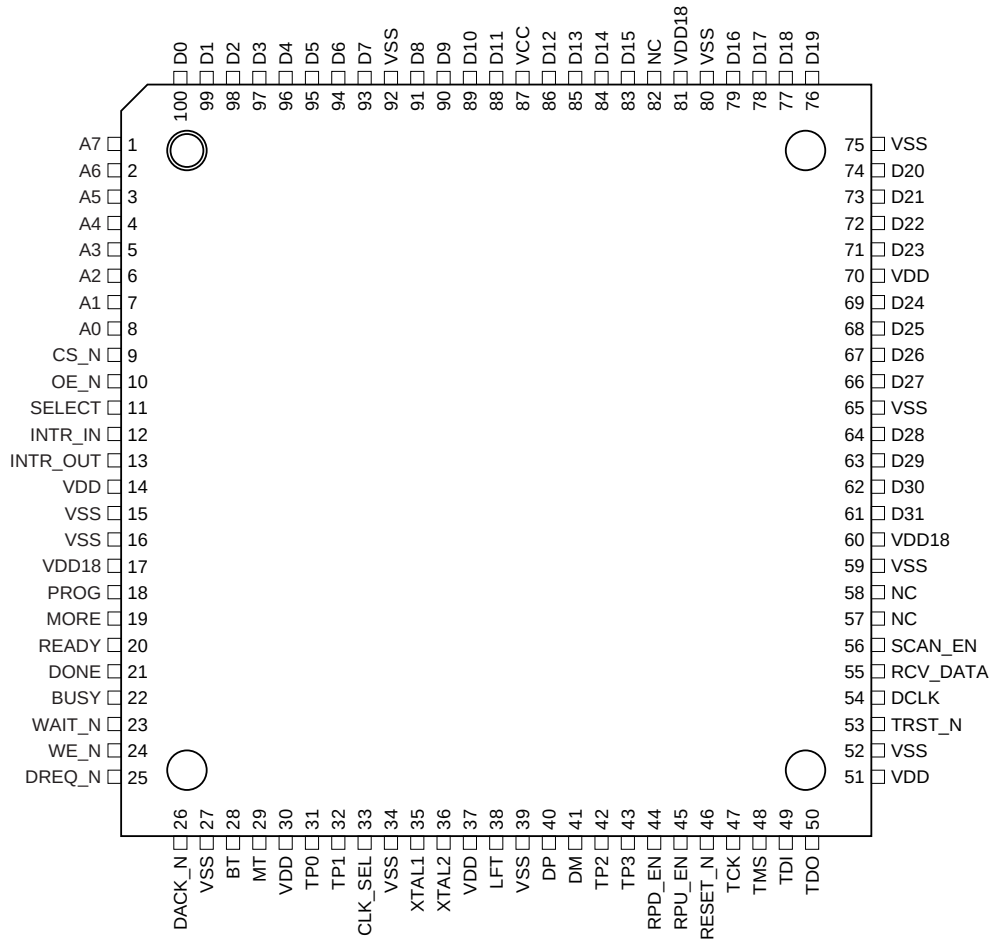
As a function, the AT43USB370 operates in full-speed mode. It supports one control endpoint and a maximum of six programmable (maximum packet size and endpoint type) endpoints. The internal USB controller runs the function firmware that manages USB enumeration and data flow control without system processor intervention.

Communication between the AT43USB370 firmware and applications resident in the system processor is realized through a small set of ANSI C compliant, system interface Application Protocol Interfaces (APIs). This API set encapsulates the complete USB functionality. It is used as the basic building blocks for constructing application specific USB device drivers of any type.

The AT43USB370, with its highly integrated USB hardware/firmware architecture, not only hides the complexity of the traditional USB design, but also frees system resources from being burdened by timing critical USB activities. It is an ideal solution for point-to-point USB connectivity in the resource constrained embedded environment.

Pin Configuration

Figure 1. AT43USB370 100-lead LQFP



Pin Assignment

Pin #	Signal	Type
1	A7	Input
2	A6	Input
3	A5	Input
4	A4	Input
5	A3	Input
6	A2	Input
7	A1	Input
8	A0	Input
9	CS_N	Input
10	OE_N	Input
11	SELECT	Input
12	INTR_IN	Input
13	INTR_OUT	Output
14	VDD	Power Supply/Gnd
15	VSS	Power Supply/Gnd
16	VSS	Power Supply/Gnd
17	VDD18	Power Supply/Gnd
18	PROG	Input
19	MORE	Input
20	READY	Output
21	DONE	Input
22	BUSY	Output
23	WAIT_N	Output
24	WE_N	Input
25	DREQ_N	Output
26	DACK_N	Input
27	VSS	Power Supply/Gnd
28	BT	Input
29	MT	Input
30	VDD	Power Supply/Gnd
31	TP0	Input
32	TP1	Output
33	CLK_SEL	Input
34	VSS	Power Supply/Gnd
35	XTAL1	Input
36	XTAL2	Output
36	XTAL2	Output
37	VDD	Power Supply/Gnd
38	LFT	Input
39	VSS	Power Supply/Gnd
40	DP	Bi-directional
41	DM	Bi-directional
42	TP2	Input
43	TP3	Input
44	RPD_EN	Output
45	RPU_EN	Output
46	RESET_N	Input
47	TCK	Input
48	TMS	Input
49	TDI	Input
50	TDO	Output
51	VDD	Power Supply/Gnd
52	VSS	Power Supply/Gnd
53	TRST_N	Input
54	DCLK	Output
55	RCV_DATA	Output
56	SCAN_EN	Input
57	NC	Not Connected
58	NC	Not Connected
59	VSS	Power Supply/Gnd
60	VDD18	Power Supply/Gnd
61	D31	Bi-directional
62	D30	Bi-directional
63	D29	Bi-directional
64	D28	Bi-directional
65	VSS	Power Supply/Gnd
66	D27	Bi-directional
67	D26	Bi-directional
68	D25	Bi-directional
69	D24	Bi-directional
70	VDD	Power Supply/Gnd
71	D23	Bi-directional
72	D22	Bi-directional
73	D21	Bi-directional
74	D20	Bi-directional
75	VSS	Power Supply/Gnd
76	D19	Bi-directional
77	D18	Bi-directional
78	D17	Bi-directional
79	D16	Bi-directional
80	VSS	Power Supply/Gnd
81	VDD18	Power Supply/Gnd
82	NC	Not Connected
83	D15	Bi-directional
84	D14	Bi-directional
85	D13	Bi-directional
86	D12	Bi-directional
87	VCC	Power Supply/Gnd
88	D11	Bi-directional
89	D10	Bi-directional
90	D9	Bi-directional
91	D8	Bi-directional
92	VSS	Power Supply/Gnd
93	D7	Bi-directional
94	D6	Bi-directional
95	D5	Bi-directional
96	D4	Bi-directional
97	D3	Bi-directional
98	D2	Bi-directional
99	D1	Bi-directional
100	D0	Bi-directional

Pin Description

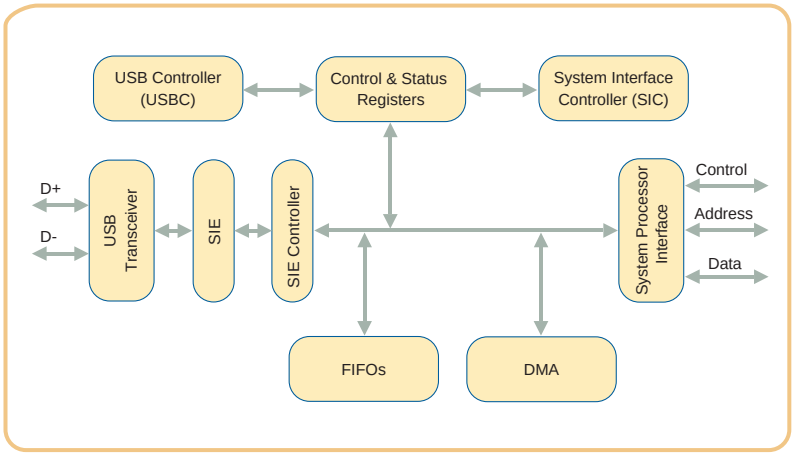
Pin Name	Type	Description
A[7:0]	Input	**ADDRESS BUS** – System Address Bus
CS_N	Input	**CHIP_SELECT** – from System Processor. Active Low
OE_N	Input	**OUTPUT_ENABLE** – from System Processor. Active Low
SELECT	Input	**PROCESSOR_SELECT** – from System Processor – used to select between the USB Controller (USBC) and System Interface Controller (SIC) when firmware is downloaded to these controllers through the System Processor. Logic “1” selects SIC and Logic “0” selects USBC.
INTR_IN	Input	**Interrupt to AT43USB370** – from System Processor. Active High
INTR_OUT	Output	**Interrupt from AT43USB370** – to System Processor. Active High
VCC	Power Supply/Gnd	**3.3V Power Net**
VDD	Power Supply/Gnd	**3.3V Power Supply**
VSS	Power Supply/Gnd	**Ground**
VDD18	Power Supply/Gnd	**1.8V Power Supply**
PROG	Input	**PROGRAM_LOAD_ENABLE** – from System Processor – used when the program is downloaded in the USB Controller and System Interface Controller through the System Processor. Active High
MORE	Input	**PIO Mode Handshake Signal** – from System Processor. Active High
READY	Output	**READY** – to System Processor – used when the program is downloaded in the USB Controller and System Interface Controller through the System Processor. Active High
DONE	Input	**DONE** – from System Processor – used when the program is downloaded in the USB Controller and System Interface Controller through the System Processor. Active High
BUSY	Output	**BUSY** – to System Processor – used when the System Interface Controller is busy in an interrupt service routine and does not want the System Processor to issue an interrupt. Active High
WAIT_N	Output	**WAIT** – to System Processor. Active Low
WE_N	Input	**WRITE_ENABLE** – from System Processor. Active Low
DREQ_N	Output	**DMA Request** – to System Processor – used to signal to the System Processor that the AT43USB370 wants to start a DMA transfer. Active Low
DACK_N	Input	**DMA Acknowledge** – from System Processor. Active Low
BT	Input	**BIST** – Test Signal
MT	Input	**Memory** – Test Signal
TP0	Input	**Test Pin 0**
TP1	Output	**Test Pin 1**
TP2	Input	**Test Pin 2**
TP3	Input	**Test Pin 3**
CLK_SEL	Input	**External/PLL Clock Selection** – Low selects crystal-PLL clock source while a High uses XTAL1, bypassing the PLL.
XTAL1	Input	**Oscillator Input** – Input to the inverting oscillator amplifier.
XTAL2	Output	**Oscillator Output** – Output of the inverting oscillator amplifier.

Pin Description (Continued)

Pin Name	Type	Description
LFT	Input	**PLL Loop Filter** – For proper operation of the PLL, this pin should be connected through a 2.2 nF capacitor in parallel with a 470 Ω resistor in series with a 22 nF capacitor to ground (VSS). Both capacitors must be high quality ceramic.
DP	Bi-directional	**D+** (USB Line)
DM	Bi-directional	**D-** (USB Line)
RPD_EN	Output	**Pull Down Enable**
RPU_EN	Output	**Pull Up Enable**
RESET_N	Input	**RESET** – Active Low
TCK	Input	**JTAG Clock**
TMS	Input	**JTAG Mode Select**
TDI	Input	**JTAG Serial Data IN**
TDO	Output	**JTAG Serial Data OUT**
TRST_N	Input	**JTAG Reset** – Active Low
DCLK	Output	**Recovered SIE DPLL Clock**
RCV_DATA	Output	**Recovered Serial Data**
SCAN_EN	Input	**Scan Test Enable**
NC	–	**Not Connected**
D[31:0]	Bi-directional	**System Data Bus**

Block Diagram

Figure 2. AT43USB370 Hardware



Architectural Overview

The AT43USB370 host/function processor is available in the SRAM version. It utilizes two on-chip microcontrollers, the USB controller (USBC) and the System Interface Controller (SIC) to offload USB related processing from the system processor. On power-up or reset, the system processor downloads the appropriate firmware into the USBC and SIC via the system bus interface.

Functionally, the USBC manages the low-level USB protocol such as enumeration, frame management and transaction scheduling, in addition to handling USB hub driver. The SIC provides data flow management to and from the system processor. It is responsible for constructing USB packets of appropriate sizes, handling retries, channeling data to and from FIFOs, and providing API support to the external system processor.

The USBC and the SIC share the same set of on-chip Control and Status Registers with the System Processor Interface. The system interface logic makes use of this register set to facilitate data exchange between the AT43USB370 and the system processor. In a typical design scenario, the AT43USB370 appears as a memory mapped peripheral to the system processor. Externally accessible registers are shown in Table 1 on page 11. The read and write accesses to the system interface registers by the system processor are made through external memory operations on the system bus.

The system processor connects to the AT43USB370 through the generic 32-bit system processor interface. The system interface signals consist of an address bus, a data bus, a chip select, a read enable and write enable. The on-chip DMA engine provides maximum data throughput between the system processor and the on-chip USB FIFO blocks. The system processor communicates with the DMA engine through standard DMA signaling.

The embedded USB hardware consists of a USB Transceiver, a Serial Interface Engine (SIE), a SIE Controller, an SOF (Start of Frame) Generation and a FIFO block. The FIFO block is divided into a 128-bytes control endpoint and 2 Kbytes of memory block dynamically configurable to support different data endpoint requirements.

The AT43USB370 can be configured to operate either in host mode or function mode. The mode of operation is determined by writing corresponding values to the specified registers and downloading the corresponding USBC and SIC firmware to the AT43USB370. The AT43USB370 commences its operation once it is configured.

The AT43USB370 requires an external 6-MHz crystal to provide a reference clock frequency for the on-chip PLL. The PLL provides all of internal clock sources required for the AT43USB370.

Functional Description

USB Transceiver

A Universal Serial Bus Revision 2.0 compliant transceiver is embedded in the AT43USB370. The transceiver provides the physical layer signaling and is capable of transmitting and receiving serial data at 12 Mbps and 1.5 Mbps. The driver portion of the transceiver is differential while the receiver section is comprised of a differential and two single-ended receivers. Internally, the transceiver interfaces to the Serial Interface Engine. Externally, the transceiver interfaces directly with the USB connectors and cables through external termination resistors.

Serial Interface Engine (SIE)

The SIE is implemented entirely in hardware. It performs the following functions:

- Clock and Data Recovery from incoming USB data stream
- Serial/parallel conversion

- NRZI encoding/decoding
- CRC calculation (generation and checking)
- Generating full-speed and low-speed USB physical layer signaling
- Device connection/disconnection detection
- Token generation (IN, OUT, SOF, SETUP etc.)
- Keep Alive signal for low-speed devices
- Bit stuffing and unstuffing

SIE Controller

This block serves as the interfaces between the SIE and the USBC. It decodes the commands received from the USBC and updates the status after the end of a USB transaction. This block also controls the FIFOs for data and control packets and provides the USB Controller access to these FIFOs for internal data management such as automatic retries for failed transactions.

USB Controller

This internal microcontroller is dedicated to managing the USB Protocol in both the host mode and the function mode. The Control and Status registers of the AT43USB370 are mapped into its data memory for fast and easy access. The firmware running on this controller determines its operating mode, either host or function.

System Interface Controller

This internal microcontroller serves as an interface between the USB Controller and the external system processor. Firmware running on this controller manages the data flow to and from the system processor. It also provides a generic USB device driver interface to system applications.

FIFO

The FIFO block contains one data FIFO block and one control FIFO block. The control FIFO has a 128 bytes of memory which is divided into one TX and one RX control FIFO. AT43USB370 uses this FIFO for the bi-directional control endpoint.

The data FIFO has 2 Kbytes of memory. The FIFO control logic allows for dynamic configuration of the data FIFO. In host mode, the FIFO memory is divided into 1 Kbytes of TX endpoint and 1 Kbytes of RX endpoint. The HUSBCD uses this memory for storing data packets. In the event of an error during a USB transaction, the SIE controller is informed of the error and the transaction is retried.

In function mode, the FIFO is divided into two 1 Kbytes blocks, one for the IN endpoints and one for the OUT endpoints. Each of the 1 Kbytes endpoint block can then be dynamically configured during runtime to support up to 3 endpoint in the same direction, but of varying maximum packet sizes.

Control and Status Registers

This block is used to configure the AT43USB370 at the start of operation. The USBC and the SIC share this register set with the system processor interface logic.

By default this block is pre-configured for Host operation with the DMA enabled for the 32-bit data bus. In function mode, this block is used to define the number and nature of the endpoints for the function. A maximum of 3 IN and 3 OUT endpoints can be specified aside from the bi-directional control endpoint. Endpoint type and, maximum packet size and other parameters are also defined using this block.

A subset of the Control and Status register set, the System Processor Interface registers, is accessible by the system processor as external memory locations. It is used to facilitate data exchange between the system processor and the AT43USB370.

System Processor Interface

The system processor interface provides 32-bit bi-directional data paths to the external processor for read and write operations to the AT43USB370's System Processor Interface registers and FIFO. The AT43USB370 appears as a memory mapped peripheral to the external system processor. The interface logic requires a number of control lines and an 8-bit address bus.

DMA

The DMA engine provides DMA support for the system processor to transfer data between the processor's memory and the AT43USB370's internal FIFO. The system processor's DMA controller controls the DMA operation through standard DMA Request and Acknowledgement signals. The AT43USB370 can only operate as a DMA slave.

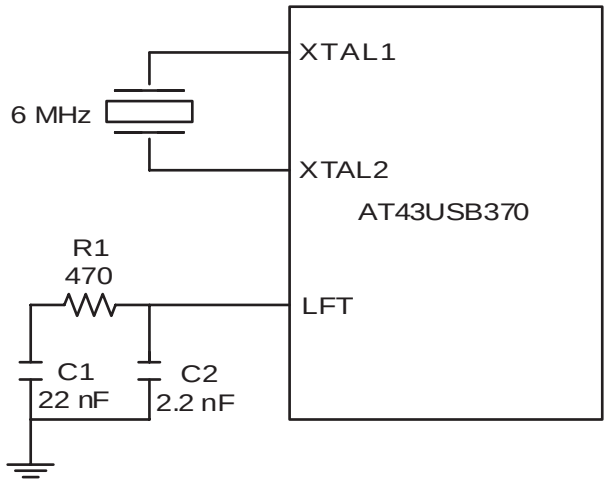
Oscillator and PLL

XTAL1 and XTAL2 are the clock pins to the AT43USB370. An external oscillator or a crystal can be connected to these pins. All clock signals required to operate the AT43USB370 are derived from the on-chip PLL. The on-chip PLL is of a special, low-drive type, designed to operate with most of the 6-Mhz crystals without any external components. The crystal must be of the parallel resonance type requiring a load capacitance of about 10 pF. If the crystal requires a higher value capacitance, external capacitors can be added to the two terminals of the crystal and ground to meet the required value. To assure a quick start-up, a crystal with a high Q, or low ESR, should be used.

The 48-MHz clock can also be externally sourced. In this case, the clock source is connected to XTAL1 pin with XTAL2 pin left open and the CLK_SEL pin tied to logic “1”.

For proper operation of the PLL, an external RC filter consisting of a series RC network of 470 Ω and 22 nF in parallel with a 2.2 nF capacitor must be connected from the LFT pin to V_{SS}. Only high-quality ceramic capacitors are recommended. Figure 3 shows the required crystal and external circuitry.

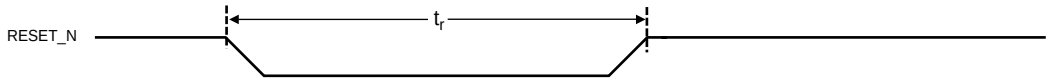
Figure 3. Oscillator and PLL



Reset

The reset signal to the AT43USB370 is active low. On reset, both the USBC and SIC are initialized and the System Processor Interface Registers are restored to their default values. Figure 4 shows the Reset timing diagram. For Reset timing, see Table 5 on page 44.

Figure 4. Reset Timing



Power Supply

The AT43USB370 requires an external supply of 3.3 V and 1.8 V.

Firmware Download Mechanism

The AT43USB370 provides an in-system programming of the USBC and the SIC through the external system processor. Programming requires SELECT, PROG, READY and DONE control signals. These control I/Os are dedicated to in-system firmware download and are not used during normal operation.

The firmware is downloaded in the program memories (SRAM) of the internal controllers after power-up or reset. The SELECT signal is used to select the USBC or the SIC for programming. The PROG signal is used to mark the start and end of firmware download. The READY and DONE signals are used for handshaking during successive programming write cycles.

The programming sequence of an internal controller is described as follows:

1. One of the controllers is selected using the SELECT pin of the AT43USB370. Logic low selects the USBC and logic high selects the SIC. The order of programming of the controllers is immaterial. Any of the controllers can be programmed first.
2. The PROG pin is asserted high by the system processor to indicate the start of programming.
3. The system processor writes the 32-bit program word on the data bus.
4. The system processor waits for READY to be asserted high by the AT43USB370.
5. AT43USB370 asserts READY logic high to signal to the system processor that the 32-bit data word has been written to the program memory of the selected controller.
6. The system processor asserts the DONE signal high after detecting logic high on READY
7. AT43USB370 asserts READY logic low.
8. The system processor asserts logic low on DONE.
9. This completes one 32-bit write cycle of the controller's programming. Steps 2 to 8 repeated until the entire firmware is downloaded in the program memory of the selected controller.
10. Step 1 is then repeated to select the remaining controller. Step 2 to 9 are repeated to program the remaining controller.
11. The PROG is de-asserted by the system processor once the firmware download is complete. This signals an end of in-system programming of the AT43USB370.

The 32-bit word written by the system processor to its system bus must conform to the following format:

- Bits15:0: Address of the instruction
- Bits 31:16: The actual instruction itself

Both controllers reset internally and start executing the firmware when PROG is de-asserted. The AT43USB370 starts its operation as a USB host or USB function depending upon the firmware downloaded by the system processor.

Figure 5 and Figure 6 illustrate the programming waveform for the USBC and the SIC respectively.

Figure 5. Typical USB Controller's Programming Waveform

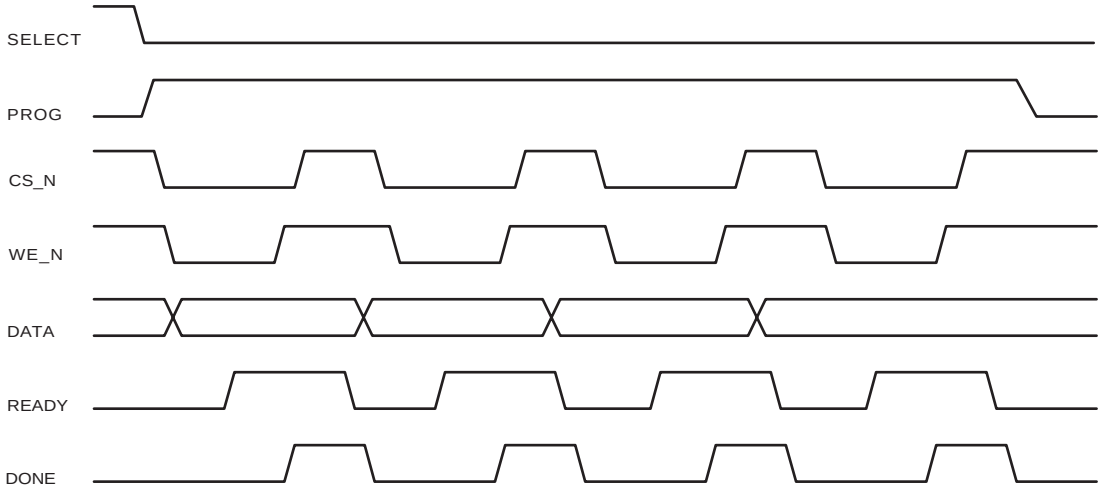
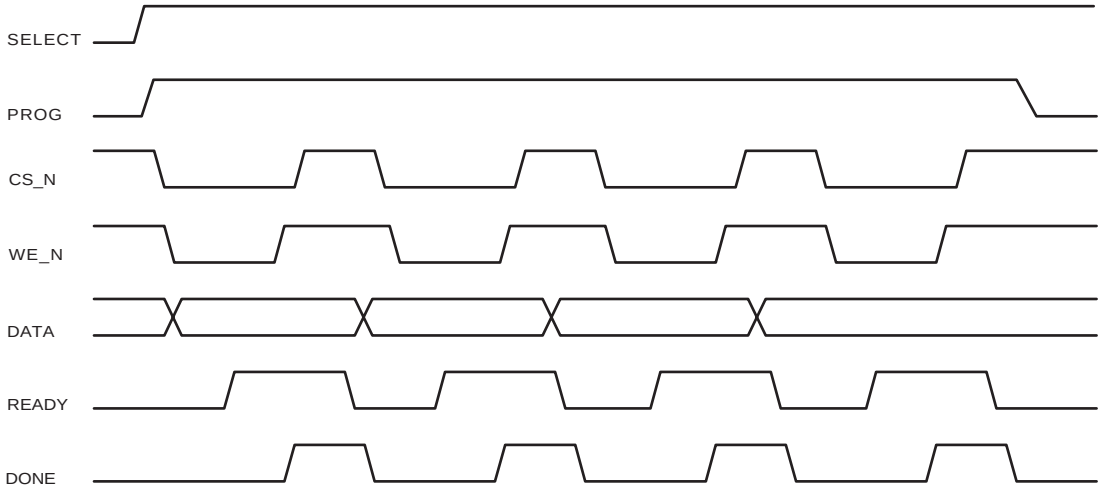


Figure 5 shows the programming waveform for the SIC.

Figure 6. Typical System Interface Controller Programming Waveform



System Processor Interface Register Set

The System Processor Interface register set is used by the AT43USB370 to interact with the system processor. The same register set is used in both the host and the function modes except where explicitly stated. All registers are 32-bit wide and require access on 4-bytes boundaries.

Reading a register for which the external system processor does not have read access will yield a zero value result. Writing to a register for which the external system processor does not have write access has no effect. For detailed usage of the registers, please refer to the *AT43USB370 Software Development Guide*.

Naming Convention

The following naming convention applies to the System Processor Interface Register Set.

- Three different fields in the register name are separated by underscores '_'
- The first field in the register name is a prefix indicating the Write access identification literal:

  - USBP indicates the register is always written by the AT43USB370 USB Processor
  - SYSP indicates the register is always written by the system processor
- The second field in the register name indicates the functionality of the register
- The third field in the register name is a suffix 'REG' common to all the registers

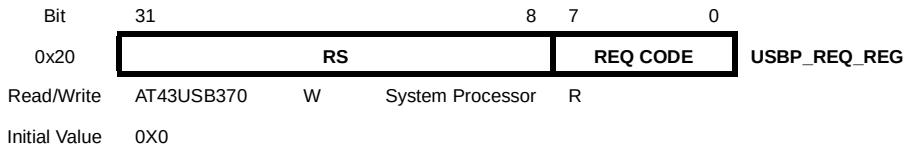
Table 1. System Processor Interface Register Set

Address	Name	Function
0x20	USBP_REQ_REG	Request Register
0x21	SYSP_CMD_REG	Command Register
0x22	SYSP_DEVADDR_REG	Device Address Register
0x23	USBP_DEVADDR_REG	Device Address Register
0x24	USBP_CLASSCD_REG	Class Code Register
0x25	Reserved	Unused
0x26	USBP_CMDID_REG	Command ID Register
0x27	USBP_EXECMDID_REG	Executed Command ID Register
0x28	SYSP_EPATT_REG	Endpoint Attributes Register
0x29	SYSP_PKTSIZE_REG [7:0]	Packet Size Register (LSB)
0x2A	SYSP_PKTSIZE_REG [15:8]	Packet Size Register (MSB)
0x2B - x2F	Reserved	Unused
0x30	SYSP_CMDPRM0_REG	Command Parameter 0 Register
0x31	SYSP_CMDPRM1_REG	Command Parameter 1 Register
0x32	SYSP_CMDPRM2_REG	Command Parameter 2 Register
0x33	SYSP_CMDPRM3_REG	Command Parameter 3 Register
0x34	SYSP_CMDPRM4_REG	Command Parameter 4 Register
0x35	SYSP_CMDPRM5_REG	Command Parameter 5 Register
0x36	SYSP_CMDPRM6_REG	Command Parameter 6 Register
0x37	SYSP_CMDPRM7_REG	Command Parameter 7 Register
0x38	USBP_VENDID_REG [7:0]	Vendor ID Register (LSB)
0x39	USBP_VENDID_REG [15:8]	Vendor ID Register (MSB)
0x3A	USBP_PRODID_REG [7:0]	Product ID Register (LSB)
0x3B	USBP_PRODID_REG [15:8]	Product ID Register (MSB)
0x3C	USBP_RELNUM_REG [7:0]	BCD Release Number Register (LSB)
0x3D	USBP_RELNUM_REG [15:8]	BCD Release Number Register (MSB)
0x3E	USBP_HUBADDR_REG	Hub Address Register
0x3F	USBP_PORTNUM_REG	Port Number Register
0x40 - 0x47	Reserved	Unused
0x48	USBP_REQPRM0_REG	Request Parameter 0 Register
0x49	USBP_REQPRM1_REG	Request Parameter 1 Register
0x4A	USBP_REQPRM2_REG	Request Parameter 2 Register

Table 1. System Processor Interface Register Set (Continued)

Address	Name	Function
0x4B	USBP_REQPRM3_REG	Request Parameter 3 Register
0x4C	USBP_REQPRM4_REG	Request Parameter 4 Register
0x4D	USBP_REQPRM5_REG	Request Parameter 5 Register
0x4E	USBP_REQPRM6_REG	Request Parameter 6 Register
0x4F	USBP_REQPRM7_REG	Request Parameter 7 Register
0x50	SYSP_SNDADDR_REG [7:0]	Send Data Address Register (LSB)
0x51	SYSP_SNDADDR_REG [15:8]	Send Data Address Register
0x52	SYSP_SNDADDR_REG [23:16]	Send Data Address Register
0x53	SYSP_SNDADDR_REG [31:24]	Send Data Address Register (MSB)
0x54	SYSP_SNDCNT_REG [7:0]	Send Data Count Register (LSB)
0x55	SYSP_SNDCNT_REG [15:8]	Send Data Count Register
0x56	SYSP_SNDCNT_REG [23:16]	Send Data Count Register
0x57	SYSP_SNDCNT_REG [31:24]	Send Data Count Register (MSB)
0x58 - 0x5F	Reserved	Unused
0x60	SYSP_GETADDR_REG [7:0]	Get Data Address Register (LSB)
0x61	SYSP_GETADDR_REG [15:8]	Get Data Address Register
0x62	SYSP_GETADDR_REG [23:16]	Get Data Address Register
0x63	SYSP_GETADDR_REG [31:24]	Get Data Address Register (MSB)
0x64	SYSP_GETCNT_REG [7:0]	Get Data Count Register (LSB)
0x65	SYSP_GETCNT_REG [15:8]	Get Data Count Register
0x66	SYSP_GETCNT_REG [23:16]	Get Data Count Register
0x67	SYSP_GETCNT_REG [31:24]	Get Data Count Register (MSB)
0x68 - 0x71	Reserved	Unused
0x72	SYSP_DIRFCNT_REG [7:0]	Direct FIFO Count Register (LSB)
0x73	SYSP_DIRFCNT_REG [15:8]	Direct FIFO Count Register (MSB)
0x74 - 0x77	Reserved	Unused
0x78	USBP_XFRADDR_REG [7:0]	Transfer Address Register (LSB)
0x79	USBP_XFRADDR_REG [15:8]	Transfer Address Register
0x7A	USBP_XFRADDR_REG [23:16]	Transfer Address Register
0x7B	USBP_XFRADDR_REG [31:24]	Transfer Address Register (MSB)
0x7C	USBP_XFRCNT0_REG [7:0]	Transfer Count Register (LSB); DMA Mode
0x7D	USBP_XFRCNT1_REG [15:8]	Transfer Count Register (MSB)
0x7E-0xFE	Reserved	Unused
0xFF	SYSP_FIFODATA_REG	FIFO Access Register

Request Register – USBP_REQ_REG



- **Bit 7:0 - REQ CODE**

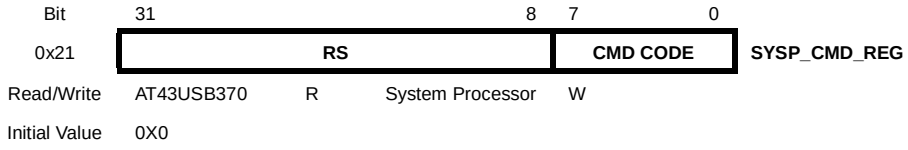
Request code of the request issued by the AT43USB370.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to write the request codes while issuing requests to the system processor. After power-up or reset, this register will contain the value 0x00.

Command Register – SYSP_CMD_REG



- **Bit 7:0 - CMD CODE**

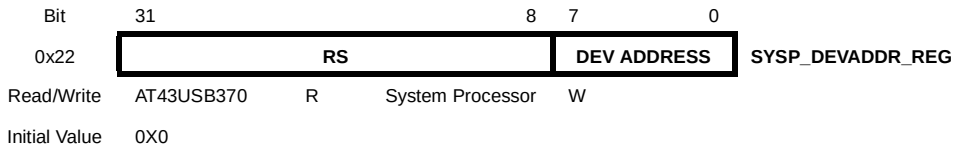
Command code of the command issued by the system processor.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the system processor to write the commands codes while issuing commands to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Device Address Register – SYSP_DEVADDR_REG



- **Bit 7:0 - DEV ADDR**

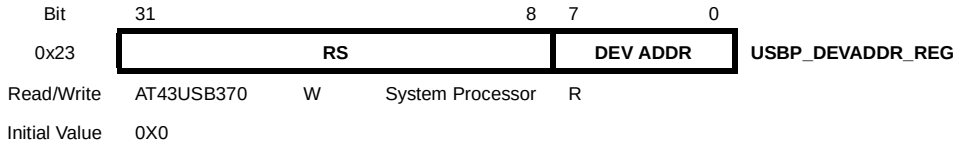
Device address of the target device.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero.

This register is used by the system processor to write the address of the device for which a command is being issued to the AT43USB370. This register is only used by the AT43USB30 Host. After power-up or reset, this register will contain the value 0x00.

Device Address Register – USBP_DEVADDR_REG



- **Bit 7:0 - DEV ADDR**

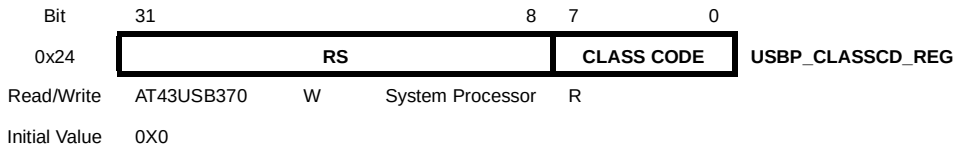
Device address of the target device.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to write the address of the device for which a request is being issued to the system processor. This register is used only by the AT43USB30 Host. After power-up or reset, this register will contain the value 0x00.

Class Code Register – USBP_CLASSCD_REG



- **Bit 7:0 - CLASS CODE**

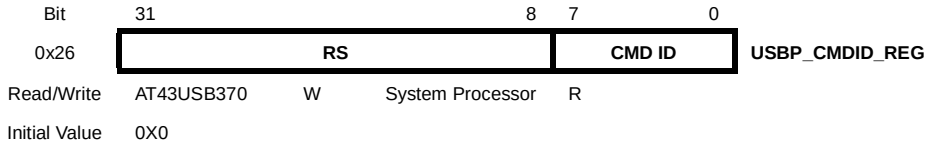
Class code value the device.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to write the class code value while issuing a request to the system processor. This register is used only by the AT43USB30 Host. After power-up or reset, this register will contain the value 0x00.

Command ID Register – USBP_CMDID_REG



- **Bit 7:0 - CMD ID**

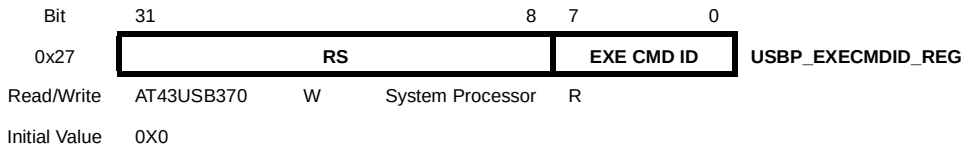
Command ID of the command.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to write the Command ID in response to a command issued by the system processor. After power-up or reset, this register will contain the value 0x00.

Executed Command ID Register – USBP_EXECMDID_REG



- **Bit 7:0 - EXE CMD ID**

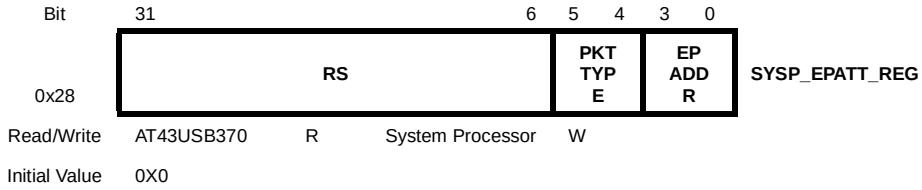
Command ID of the command executed.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to write the Command ID of a particular command executed by the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Endpoint Attributes Register – SYSP_EPATT_REG



- **Bit 3:0 - EP ADDR**

Endpoint address of the target endpoint.

- **Bit 5:4 - PKT TYPE**

Packet type of the packet.

00 IN Packet, OUT Packet

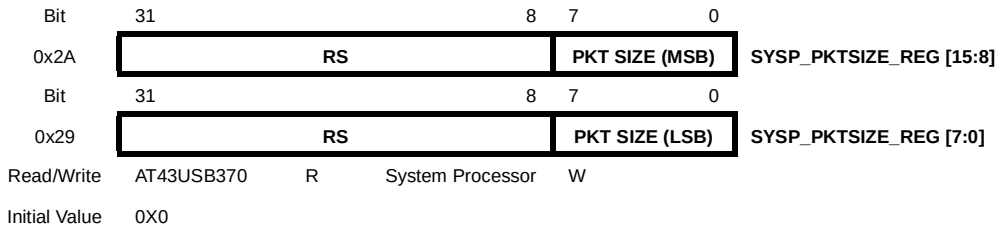
11 SETUP Packet

- **Bit 31:6 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify the endpoint attributes. After power-up or reset, this register will contain the value 0x00.

Packet Size Register – SYSP_PKTSIZE_REG



- **Bit 15:0 PCK SIZE**

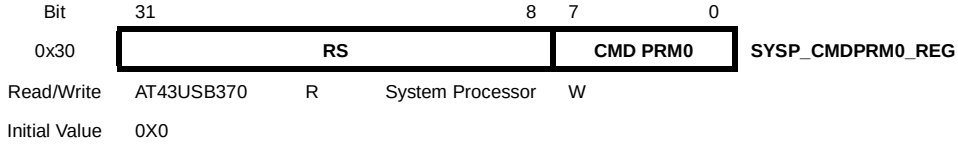
Packet size in bytes.

- **Bit 31:16 - RS**

Reserved. Must be reset to zero by the system processor.

These registers are used by the system processor to specify the Packet Size while issuing a command to the AT43USB370. This packet size is used by the AT43USB370 Host for every transaction associated with this command. This register is used only by the AT43USB30 Host. After power-up or reset, these registers will contain the value 0x00.

Command Parameter 0 Register – SYSP_CMDPRM0_REG



- **Bit 7:0 - CMD PRM0**

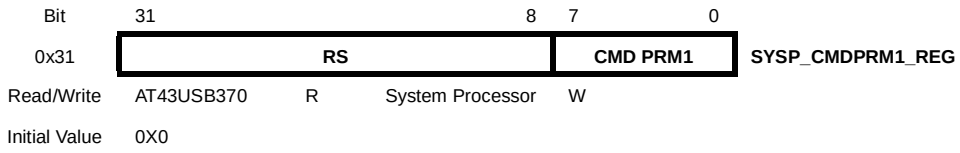
Command-specific parameter.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify a command-specific parameter while issuing a command to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Command Parameter 1 Register – SYSP_CMDPRM1_REG



- **Bit 7:0 - CMD PRM1**

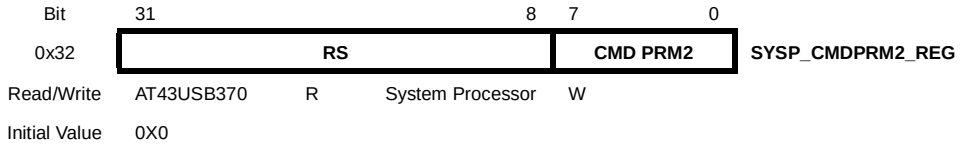
Command-specific parameter.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify a command-specific parameter while issuing a command to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Command Parameter 2 Register – SYSP_CMDPRM2_REG



- **Bit 7:0 - CMD PRM2**

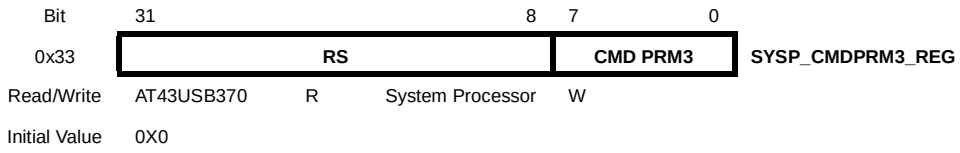
Command-specific parameter.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify a command-specific parameter while issuing a command to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Command Parameter 3 Register – SYSP_CMDPRM3_REG



- **Bit 7:0 - CMD PRM3**

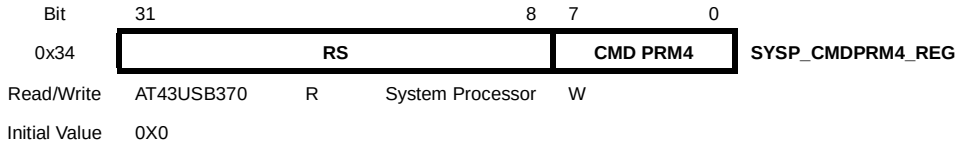
Command-specific parameter.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify a command-specific parameter while issuing a command to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Command Parameter 4 Register – SYSP_CMDPRM4_REG



- **Bit 7:0 - CMD PRM4**

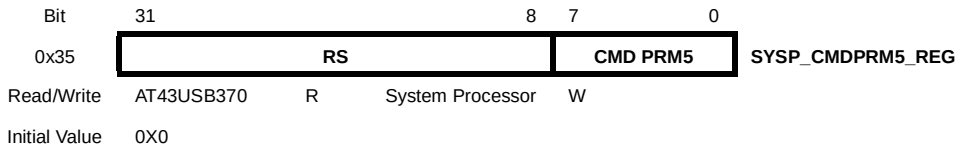
Command-specific parameter.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify a command-specific parameter while issuing a command to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Command Parameter 5 Register – SYSP_CMDPRM5_REG



- **Bit 7:0 - CMD PRM5**

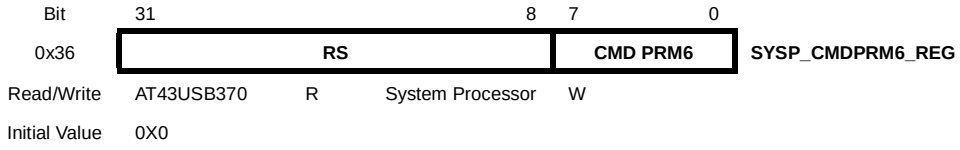
Command-specific parameter.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify a command-specific parameter while issuing a command to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Command Parameter 6 Register – SYSP_CMDPRM6_REG



- **Bit 7:0 - CMD PRM6**

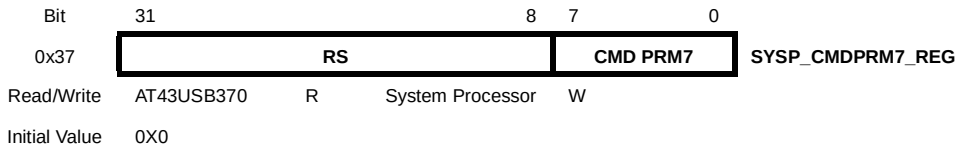
Command-specific parameter.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify a command-specific parameter while issuing a command to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Command Parameter 7 Register – SYSP_CMDPRM7_REG



- **Bit 7:0 - CMD PRM7**

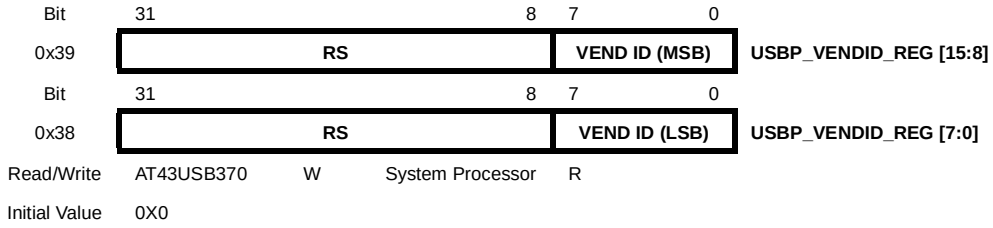
Command-specific parameter.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor.

This register is used by the system processor to specify a command-specific parameter while issuing a command to the AT43USB370. After power-up or reset, this register will contain the value 0x00.

Vendor ID Register – USBP_VENDID_REG



- **Bit 15:0 VEND ID**

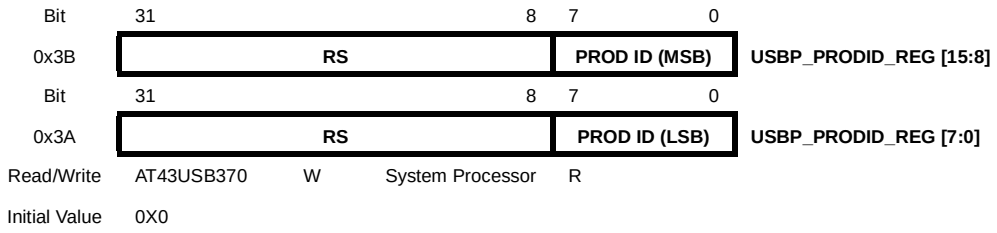
Vendor ID of the USB device.

- **Bit 31:16 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the AT43USB370 to specify the Vendor ID while issuing a request to the system software. They are only used in the host mode. After power-up or reset, these registers will contain the value 0x00.

Product ID Register – USBP_PRODID_REG



- **Bit 15:0 PROD ID**

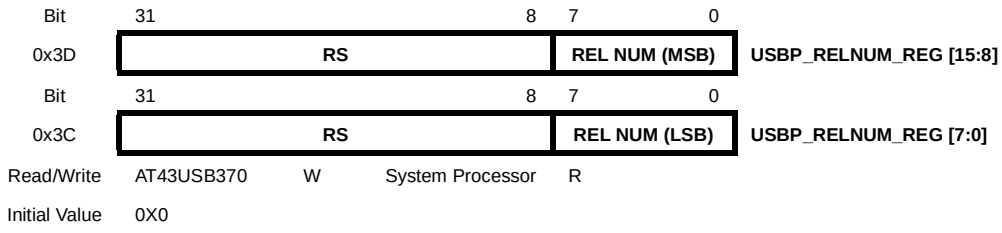
Product ID of the USB device.

- **Bit 31:16 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the AT43USB370 to specify the Product ID while issuing a request to the system processor. They are only used in the host mode. After power-up or reset, they will contain the value 0x00.

BCD Release Number Register – USBP_RELNUM_REG



- **Bit 15:0 REL NUM**

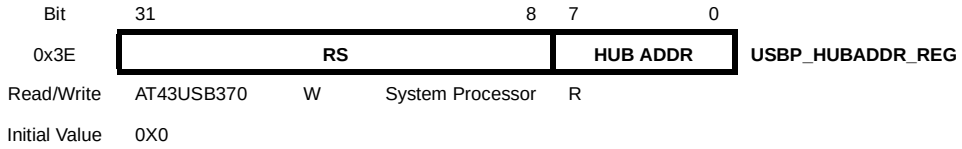
BCD Release Number of the USB device.

- **Bit 31:16 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the AT43USB370 to specify the BCD Release Number while issuing a request to the system processor. They are used only in the host mode. After power-up or reset, they will contain the value 0x00.

Hub Address Register – USBP_HUBADDR_REG



- **Bit 7:0 - HUB ADDR**

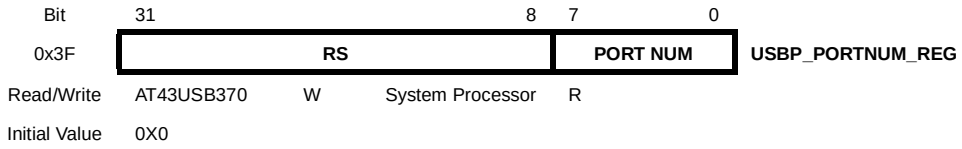
Device address of the Hub to which the USB device is connected.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to write the device address of the hub to which a USB device is connected while issuing a request to the system processor. This register is used only by the AT43USB30 Host. After power-up or reset, this register will contain the value 0x00.

Port Number Register – USBP_PORTNUM_REG



- **Bit 7:0 - PORT NUM**

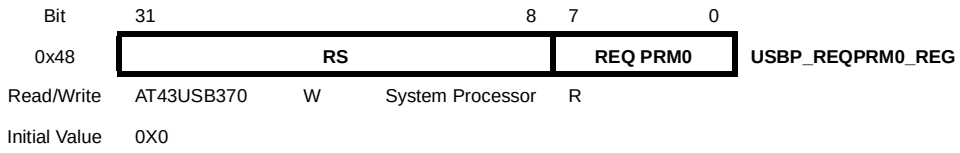
Port number of the Hub to which the USB device is connected.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to write the port number of the hub to which a USB device is connected while issuing a request to the system processor. This register is used only in the host mode. After power-up or reset, this register will contain the value 0x00.

Request Parameter 0 Register – USBP_REQPRM0_REG



- **Bit 7:0 - REQ PRM0**

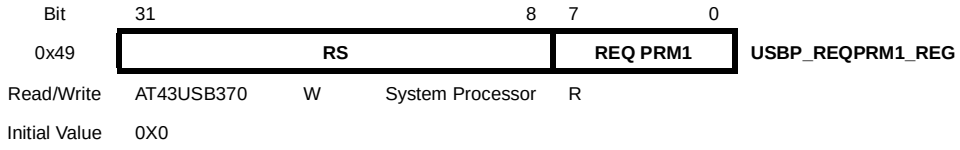
Request-specific parameter.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to specify a request-specific parameter while issuing a request to the system processor. After power-up or reset, this register will contain the value 0x00.

Request Parameter 1 Register – USBP_REQPRM1_REG



- **Bit 7:0 - REQ PRM1**

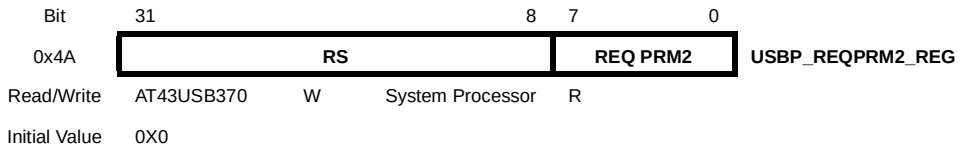
Request-specific parameter.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to specify a request-specific parameter while issuing a request to the system processor. After power-up or reset, this register will contain the value 0x00.

Request Parameter 2 Register – USBP_REQPRM2_REG



- **Bit 7:0 - REQ PRM2**

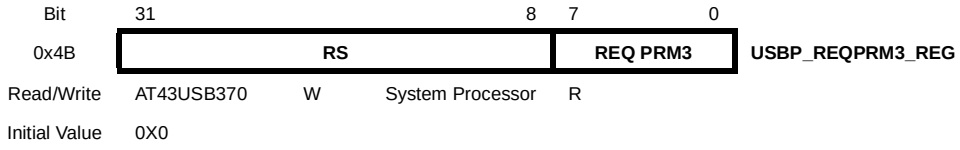
Request-specific parameter.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to specify a request-specific parameter while issuing a request to the system processor. After power-up or reset, this register will contain the value 0x00.

Request Parameter 3 Register – USBP_REQPRM3_REG



- **Bit 7:0 - REQ PRM3**

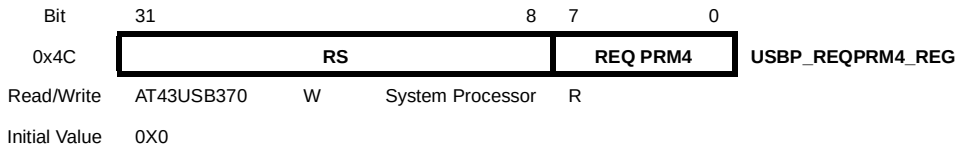
Request-specific parameter.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to specify a request-specific parameter while issuing a request to the system processor. After power-up or reset, this register will contain the value 0x00.

Request Parameter 4 Register – USBP_REQPRM4_REG



- **Bit 7:0 - REQ PRM4**

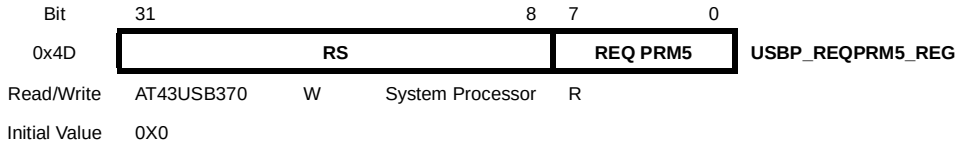
Request-specific parameter.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to specify a request-specific parameter while issuing a request to the system processor. After power-up or reset, this register will contain the value 0x00.

Request Parameter 5 Register – USBP_REQPRM5_REG



- **Bit 7:0 - REQ PRM5**

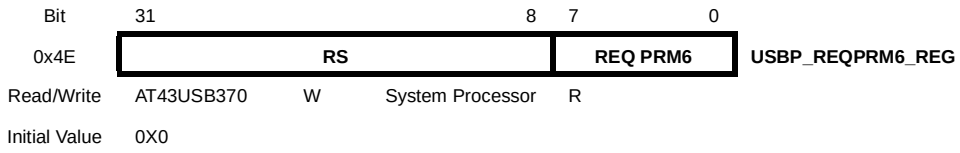
Request-specific parameter.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to specify a request-specific parameter while issuing a request to the system processor. After power-up or reset, this register will contain the value 0x00.

Request Parameter 6 Register – USBP_REQPRM6_REG



- **Bit 7:0 - REQ PRM6**

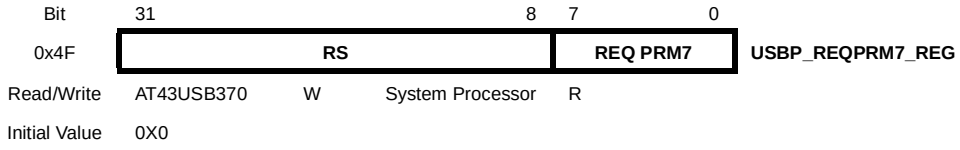
Request-specific parameter.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to specify a request-specific parameter while issuing a request to the system processor. After power-up or reset, this register will contain the value 0x00.

Request Parameter 7 Register – USBP_REQPRM7_REG



- **Bit 7:0 - REQ PRM7**

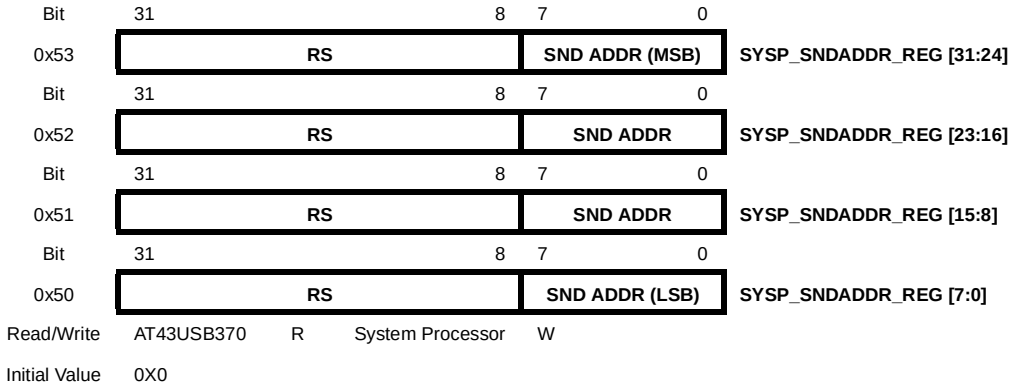
Request-specific parameter.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

This register is used by the AT43USB370 to specify a request-specific parameter while issuing a request to the system processor. After power-up or reset, this register will contain the value 0x00.

Send Data Address Register – SYSP_SNDADDR_REG



- **Bit 7:0 - SND ADDR**

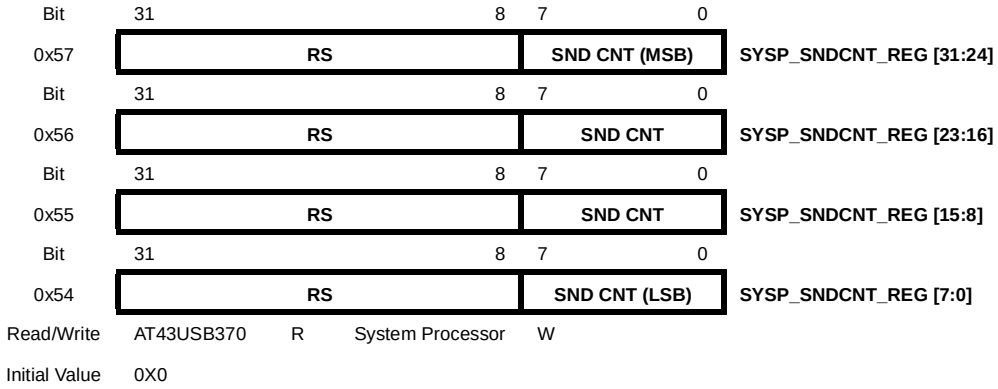
Address of the buffer for sending data. Bit 7:0 of each of the register locations are concatenated together to form the 32-bit SND ADDR.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the system processor to specify the start address of the data buffer while issuing a command to the AT43USB370 to transfer data from the system processor's memory to a USB device. After power-up or reset, this register will contain the value 0x00.

Send Data Count Register – SYSP_SNDCNT_REG



- **Bit 7:0 - SND CNT**

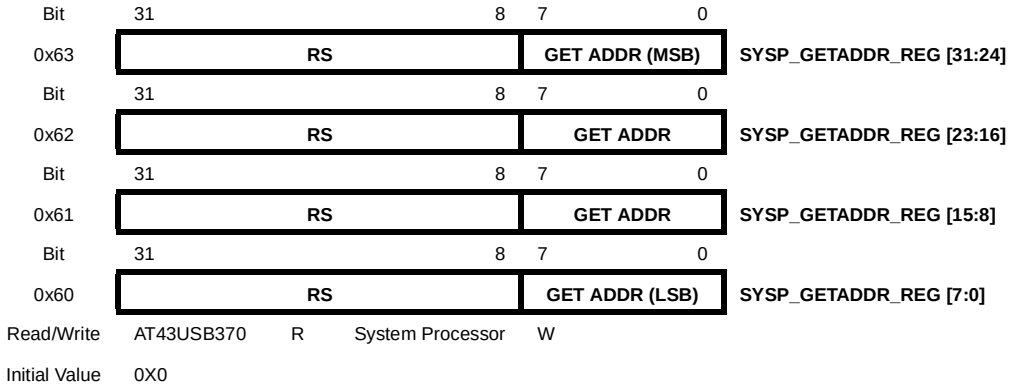
Count of the buffer for sending data. Bit 7:0 of each of the register locations are concatenated together to form the 32-bit SND CNT.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the system processor to specify the size of the data buffer while issuing a command to the AT43USB370 to transfer data from the system processor's memory to a USB device. This is the size of the buffer whose address is specified in Send Data Address Register. After power-up or reset, this register will contain the value 0x00.

Get Data Address Register – SYSP_GETADDR_REG



- **Bit 7:0 - GET ADDR**

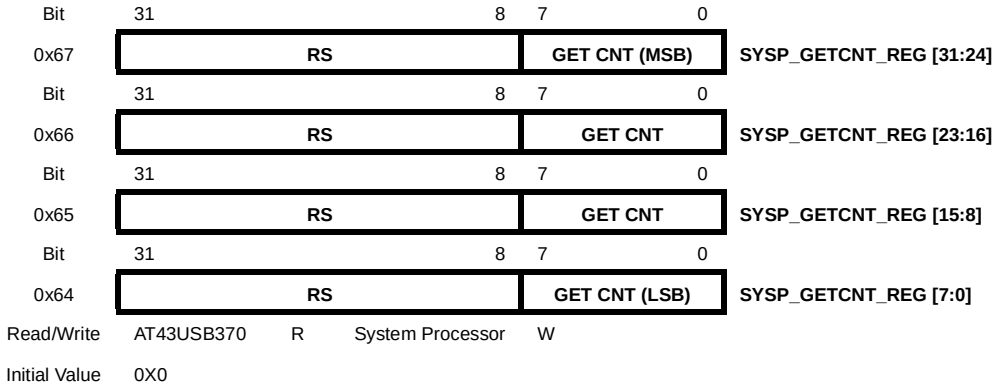
Address of the buffer for storing data. Bit 7:0 of each of the register locations are concatenated together to form the 32-bit GET ADDR.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the system processor to specify the start address of the data buffer while issuing a command to the AT43USB370 to transfer data from the USB device to the system processor's memory. After power-up or reset, this register will contain the value 0x00.

Get Data Counter Register – SYSP_GETCNT_REG



- **Bit 7:0 - GET CNT**

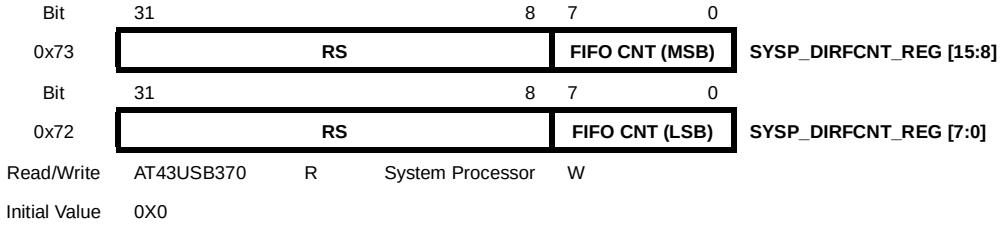
Count of the data buffer for receiving data. Bit 7:0 of each of the register locations are concatenated together to form the 32-bit GET CNT.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the system processor to specify the size of the data buffer while issuing a command to the AT43USB370 to transfer data from the USB device to the system processor's memory. This is the size of the buffer specified in Get Data Address register. After power-up or reset, this register will contain the value 0x00.

Direct FIFO Count Register – SYSP_DIRFCNT_REG



- **Bit 7:0 - FIFO CNT**

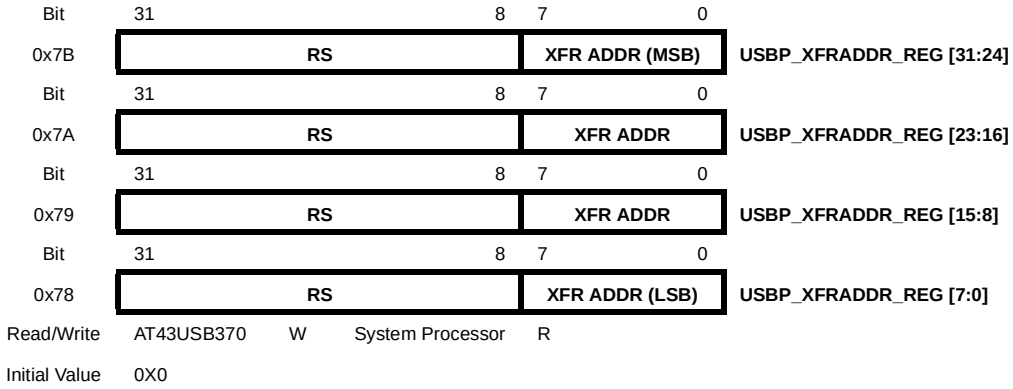
Count of the data to be transferred through Direct FIFO. Bit 7:0 of each of the register locations are concatenated together to form the 32-bit FIFO CNT. Bit 31:16 of the SYSP_DIRCNT_REG default to zero.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the system processor to specify the count while issuing a command to the AT43USB370 to transfer data between the system processor's memory and the AT43USB370's FIFO. After power-up or reset, this register will contain the value 0x00.

Transfer Address Register – USBP_XFRADDR_REG



- **Bit 7:0 - XFR ADDR**

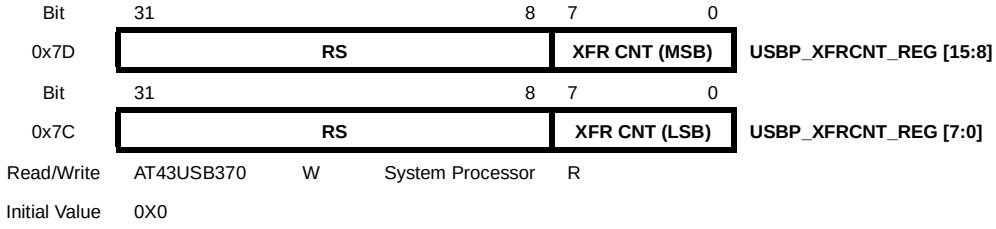
Address for the data transfer. Bit 7:0 of each of the register locations are concatenated together to form the 32-bit XFR ADDR.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the AT43USB370 to specify the start address of the memory while issuing a request to system processor to transfer data. After power-up or reset, this register will contain the value 0x00.

Transfer Count Register – USBP_XFRCNT_REG



- **Bit 7:0 - XFR CNT**

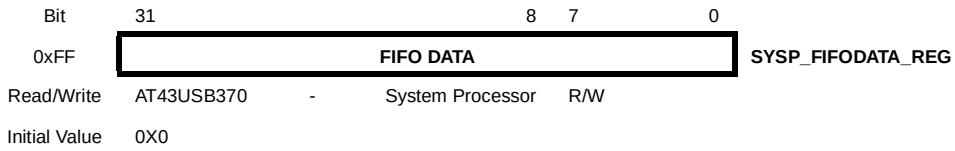
Transfer count in bytes. Bit 7:0 of each of the register locations are concatenated together to form the 32-bit XFR CNT. Bit 31:16 of the XFR CNT register default to zero.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the AT43USB370.

These registers are used by the AT43USB370 to specify the number of bytes while issuing a request to the system processor to transfer data. This register specifies the count to be transferred from the location specified in the Transfer Address register. After power-up or reset, this register will contain the value 0x00.

FIFO Data Access Register – SYSP_FIFODATA_REG



- **Bit 31:0 - FIFO Data Access Register**

Actual data to and from the FIFO.

This register is used by the system processor to either fetch the data from the AT43USB370 or push the data into the AT43USB370 FIFO. After power-up or reset, this register will contain the value 0x00.

Data Transfer Mechanisms

The AT43USB370 supports three types of data transfer mechanisms

- Programmable IO (PIO) Interface
- DMA Interface
- Direct FIFO Interface

Programmable IO Interface

The Programmable Input/Output interface is used by the system processor to perform single or multiple read/write operations to the AT43USB370's system processor interface registers. A PIO write operation allows the system processor to write to the AT43USB370 register(s). Similarly a PIO read operation allows the system processor to read the AT43USB370 register(s).

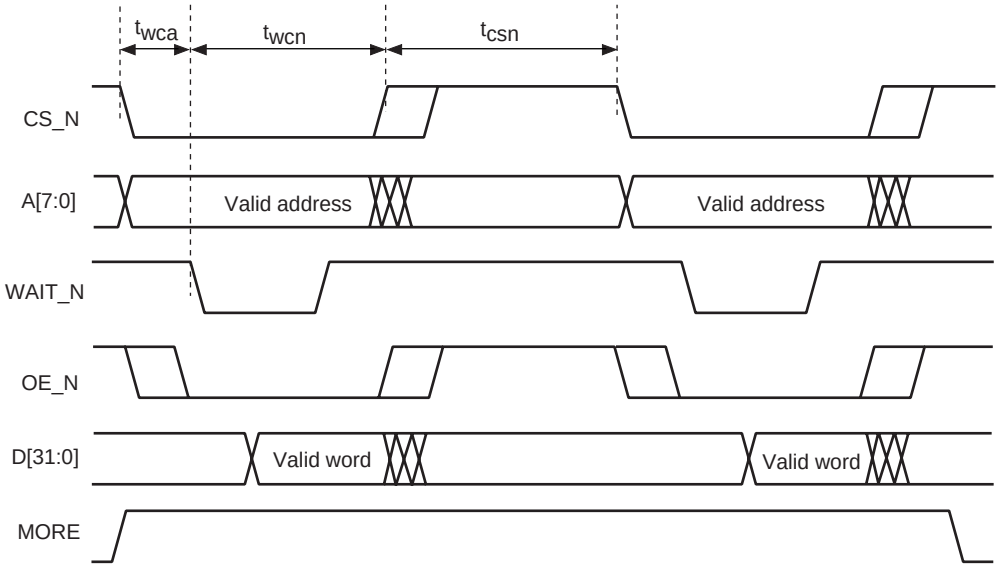
PIO Read

The following sequence illustrates the PIO read operation by the system processor to read the AT43USB370 register(s). To perform more than one read operation in one PIO transaction, the system processor asserts the MORE line before the first read operation. The AT43USB370 polls this line every time a read operation is completed.

1. The system processor initiates the PIO Read operation by asserting the chip select signal (CS_N).
2. The system processor places the address of the AT43USB370 register on the address bus.
3. The system processor asserts the MORE signal to request multiple register reads during this PIO Read operation.
4. The AT43USB370 asserts the WAIT_N signal.
5. The system processor asserts the OE_N signal.
6. The AT43USB370 reads the register address from the address bus and puts the contents of the register on the data bus.
7. The AT43USB370 de-asserts the WAIT_N signal.
8. The system processor reads the data present on the data bus.
9. The system processor de-asserts the OE_N signal.
10. The system processor de-asserts the CS_N signal. This completes a single PIO Read operation.
11. The AT43USB370 scans the MORE signal. If de-asserted, the AT43USB370 exits the PIO scan mode otherwise the AT43USB370 remains in the PIO scan mode and the PIO Read process is repeated.

Figure 7 shows two consecutive PIO Read operations. For timing specifications of the PIO Transfer, please see Table 4 on page 44.

Figure 7. PIO Read Operation



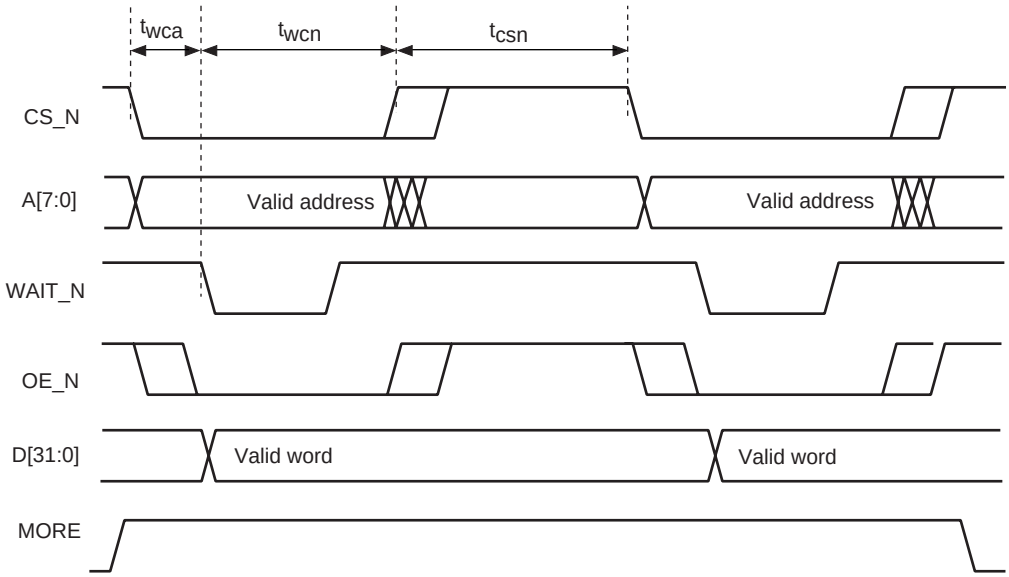
PIO Write

The following sequence illustrates the PIO write operation by the system processor to write the AT43USB370 register(s). To perform multiple write operations within one PIO transaction, the system processor asserts the MORE line before the first write operation. The AT43USB370 polls this line every time a write operation is completed.

1. To start the PIO transaction, the system processor issues an interrupt by asserting INTR_IN.
2. The system processor asserts the chip select signal (CS_N).
3. The system processor puts the address of the AT43USB370 register on the address bus.
4. The system processor puts the data on the data bus.
5. The system processor asserts the MORE signal to request multiple write operations during this PIO transaction.
6. The system processor asserts the WE_N signal.
7. The AT43USB370 reads the register address from the address bus and copies the contents of the data bus in the target register.
8. The system processor de-asserts the WE_N signal.
9. The system processor de-asserts the CS_N signal. This completes the first PIO write operation.
10. The AT43USB370 scans the MORE signal. If de-asserted, the AT43USB370 exits PIO scan mode otherwise the AT43USB370 remains in the PIO scan mode and the process is repeated.

Figure 8 shows two consecutive PIO Write operations. For timing specifications of the PIO Transfer, please see Table 4 on page 44.

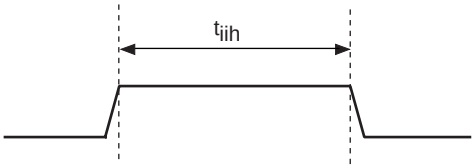
Figure 8. PIO Write Operation



Interrupt_I

To write to an AT43USB370's system processor interface register, the system processor issues an interrupt to the AT43USB370 on the INTR_IN line. Figure 9 shows the timing of INTR_I signal. For timing specifications of the INTR_I signal, please see Table 4 on page 44.

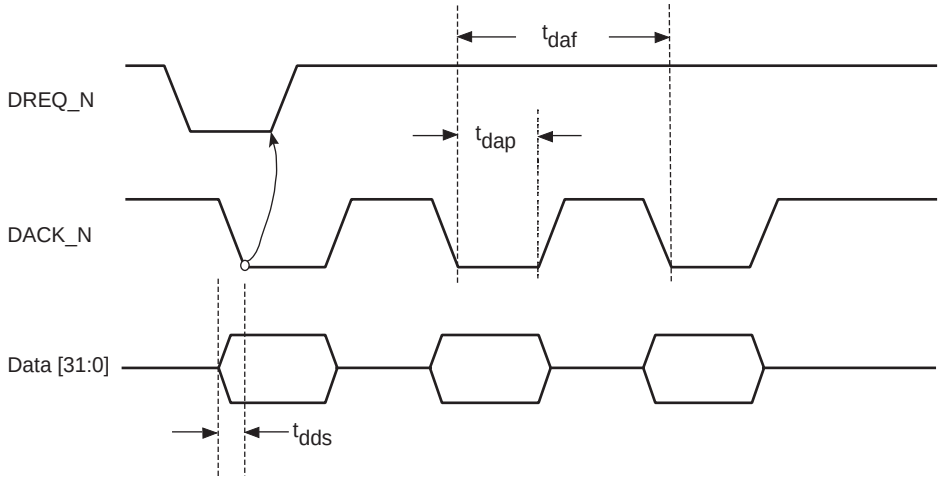
Figure 9. INTR_I Timing



DMA Interface

The DMA interface is used for data transfer between AT43USB370's internal FIFO and the system processor's memory. The AT43USB370 generates a request to initiate the DMA process by asserting the DREQ_N signal. It uses the block mode to transfer data through DMA. In this mode, all requested data are transferred upon the assertion of a single DMA request. The DREQ_N signal is de-asserted by AT43USB370 after the DACK_N signal has been asserted by the system processor. The DMA transfer is completed when the Transfer Count reaches zero in the DMA controller of the system processor. The DMA engine of the AT43UBS370 manages the count of the DMA transfers itself. Figure 10 shows the DMA Read/Write operations. The AT43USB370 can only operate as a DMA slave. For timing specifications of the DMA, please see Table 4 on page 44.

Figure 10. DMA Read/Write Operation



Direct FIFO Interface

The system processor can directly read from or write to the AT43USB370's on-chip FIFO through the Direct FIFO interface. The Direct FIFO interface for the AT43USB370 can be configured by the system processor by writing 0xFF on the address bus. The data can be pushed into the FIFO or read from it by the system processor using any normal memory read/write operations.

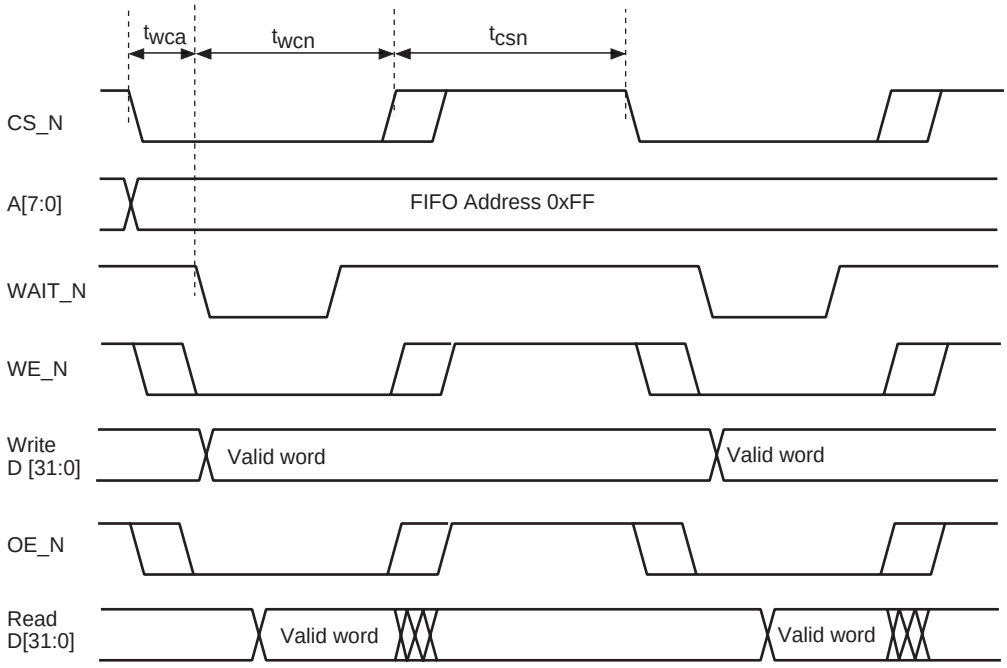
Direct FIFO Read

Figure 11 shows the timing of a FIFO read operation performed by the system processor using the Direct FIFO Interface. For timing specifications of Direct FIFO read operation, please see Table 4 on page 44.

Direct FIFO Write

Figure 11 shows the timing of a FIFO write operation performed by the system processor using the Direct FIFO Interface. For timing specifications of Direct FIFO write operation, please see Table 4 on page 44.

Figure 11. FIFO Read/Write Operation



Firmware Architecture

The AT43USB370 firmware model is supported by a set of USB firmware embedded on-chip and a set of system software with associated APIs running on the system processor. The APIs are used to support the development of USB device drivers of any type.

The AT43USB37 requires the host firmware when running in the host mode, and the function (or device) firmware when running in the function mode. The following sections describe in detail the firmware architecture of the AT43USB370 host/function processor.

Host Firmware

The AT43USB370 host firmware consists of the Host USB Controller Driver (HUSBCD) and Host System Interface Controller Driver (HSICD).

Host USB Controller Driver (HUSBCD)

The HUSBCD runs on the USBC when the AT43USB370 operates in the host mode. This driver performs the following tasks:

Autonomous Hub Support

The HUSBCD embeds a complete Hub Class driver to provide an autonomous Hub support.

Device Enumeration

The HUSBCD enumerates the newly connected device or hub.

Frame Management

Frame management involves calculating the time required for the next transaction and transaction completion prediction as described in USB 2.0 Specifications. It also includes the determinations the HUSBCD has to make at the time of enumeration to ensure that the requirements of the newly connected device can be met within the current power and bandwidth budget of the host.

Transaction Scheduling

The HUSBCD automatically schedules the transactions using the information that it receives from the devices during enumeration. Isochronous and Interrupt transactions are given up to 90% of the frame time. Bulk and Control transfers are guaranteed at least 10% of the bandwidth and are also allocated any available bandwidth not consumed by the Isochronous and Interrupt transfers.

Bus Reclamation

The HUSBCD implements the Bus Reclamation mechanism that allows the AT43USB370 host to maximize the bus utilization by using all the time left after servicing pending transactions to transfer bulk/control data.

Status Handling

After a transaction has been completed, the HUSBCD posts the transaction status to the HSICD. The HUSBCD also enables and disables the concerned FIFOs for data and control transfers.

Host System Interface Controller Driver (HSICD)

The HSICD runs on the System Interface Controller when the AT43USB370 is operating in the host mode. This driver performs the following tasks:

Data Transfer Management

The HSICD handles the data transfer between the USB function and the system processor memory.

High Level API Management

A set of C APIs and associated USB host system software library constitutes the basic building blocks of USB device drivers of any type. This USB host system software resides on the system processor. The HSICD manages the information exchange between the embedded AT43USB370 firmware stack and the host system software running on the system processor through the host system interface APIs. For detailed descriptions of the APIs, refer to *AT43USB370 Software Development Guide*.

Descriptor Management

The HSICD gathers the USB descriptors from the USB devices and reports back to system processor through API function calls.

USB Host System Library

The USB host system library is comprised of the AT43USB370 host system interface APIs and the underlying software library. All application-level system software communicates with the AT43USB370 through this library.

AT43USB370 USB Host System Library and APIs

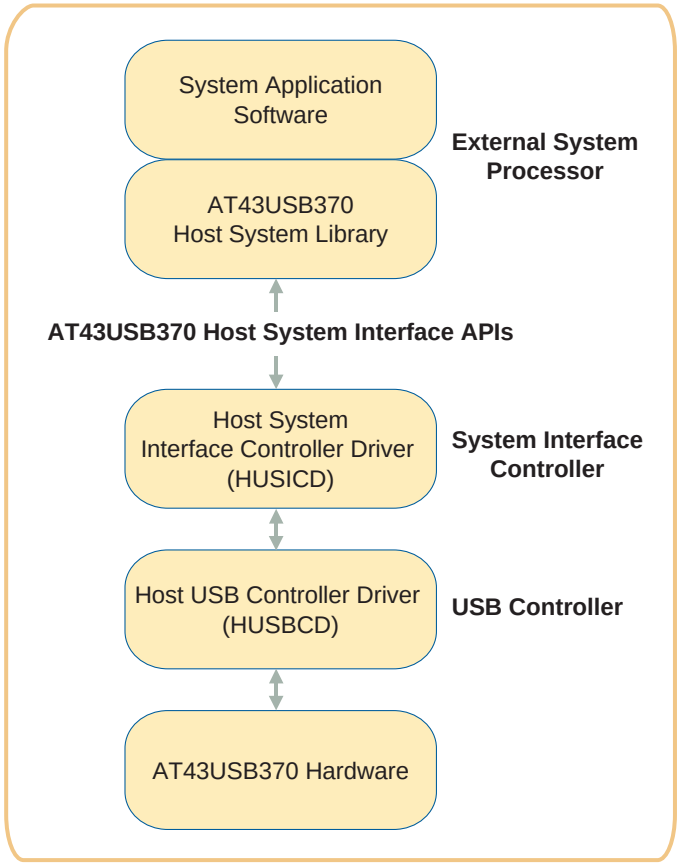
The USB host system library provides access to the AT43USB370 USB host functionality by the system processor. The corresponding host system interface API set encapsulates the complete USB functionality. It is ANSI C compliant and is used for all USB device drivers and applications development. Refer to *AT43USB370 Software Development Guide* for detailed descriptions of the AT43USB370 APIs.

System Software

System software is application specific and resides in the system processor. It communicates with the AT43USB370 through the AT43USB370 Host System Interface APIs directly or through the standard or application specific USB device drivers built on top the AT43USB370 APIs.

Figure 12 shows the AT43USB370 host firmware architecture.

Figure 12. AT43USB370 Host Firmware Architecture



Function or Device Firmware

The AT43USB370 function or device firmware includes the Device USB Controller Driver (DUSBCD) and Device System Interface Controller Driver (DSICD).

Device USB Controller Driver

The DUSBCD runs on the USB Controller. This driver interacts with the AT43USB370 hardware and performs USB protocol management relating to the function operation more specifically, the DUSBCD performs the following functions:

Device Configuration

The DUSBCD automatically configures the AT43USB370 function for the required features through a descriptor table specified by the system processor. The DUSBCD parses the USB standard and class-specific descriptors from this table and stores them in the program memory of the controller. The following features of the AT43USB370 function can be configured through the descriptor table.

- **Number of Endpoints** - Maximum of 6 data (3 IN and 3 OUT) endpoints can be supported. A bi-directional control endpoint is supported by default
- **Type of Endpoint** - Any of the Interrupt, Bulk or Isochronous endpoint may be specified
- **Maximum Packet Size** - for every endpoint including the control endpoint
- **FIFO Size** - for every endpoint
- **Remote Wake-up Support**

The format for providing the descriptor table is specified in the *AT43USB370 Software Development Guide*.

FIFO Configuration

The DUSBCD configures the FIFO according to the maximum packet sizes and endpoint types of the endpoints specified in the descriptor table. It also configures the Control and Status Registers.

Device Enumeration and Standard Request Handling

The DUSBCD generates the connect status on USB after parsing the descriptor table and automatically enumerates AT43USB370 as a device when it is connected to a USB Host. It also handles other standard USB requests issued by the USB Host.

Suspend Detection

The DUSBCD detects the suspend condition when no bus activity is reported from the SIE Controller for 3 ms.

Transaction Handling

The DUSBCD automatically handles incoming packets for OUT endpoints for expected Isochronous, Bulk and Interrupt transactions which are ultimately reported to the external system processor. Similarly, it supplies the USB Host required data from IN endpoints after getting it from the external system processor.

Device System Interface Controller Driver

The DSICD runs on the System Interface Controller. This driver is responsible for the following functions:

Data Transfer Management

The DSICD handles the data transfer between the AT43USB370 Device and the external system processor's memory. It also provides an interface to specify the descriptor table.

High Level API Management

The DSICD provides a generic interface for the system processor in order to achieve maximum ease in the Device operation at a high level. The DSICD manages all the information exchange with the external system processor through this interface. In this way, the complexity in transferring data over the USB is hidden from the external system processor. For more details about the API, refer to the *AT43USB370 Software Development Guide*.

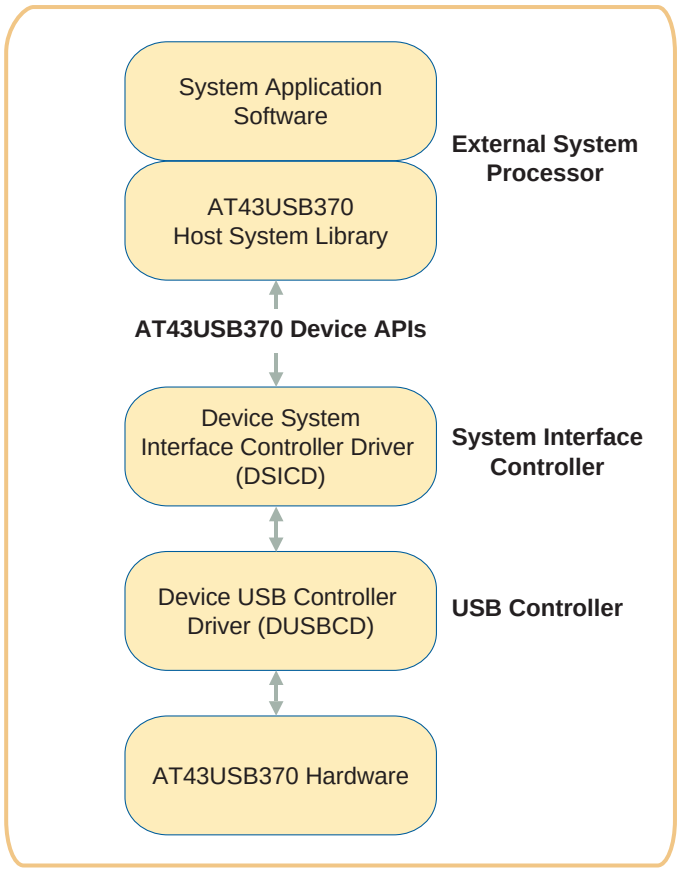
USB Device System Library and APIs

The USB Device System Library runs on the external system processor. It provides access to USB functionality of the AT43USB370 to the system application running on the system processor. The system library interfaces to the system application through a set of high level, ANSI C compliant APIs. The API set encapsulates the USB functionality and is used as the

building blocks of any USB application. Please refer to the *AT43USB370 Software Development Guide* for detailed descriptions of the AT43USB370 device APIs.

Figure 13 shows the device firmware architecture of the AT43USB370.

Figure 13. AT43USB370 Device Firmware Architecture



System Processor Connection

The AT43USB370 is typically attached to a system processor through its 32-bit bi-directional data path with additional control lines and an 8-bit address bus. The required interface signals are grouped into the following categories:

General Interface Signals

- **DATA BUS (D [31:0])** - The 32-bit bi-directional data bus is used to transfer data to and from AT43USB370. The AT43UBS370 is little-endian compatible.
- **ADDRESS BUS (A [7:0])** - This is an 8-bit address bus used to address the System Processor Interface Register set of the AT43USB370.
- **CHIP SELECT (CS_N)** - The CHIP SELECT signal is active low.
- **OUTPUT ENABLE (OE_N)** - This is the Read signal driven by the system processor to read a register or memory location. This signal is active low.
- **WRITE ENABLE (WE_N)** - This is the Write signal driven by the system processor to write an address, register or memory location. This signal is active low.
- **WAIT (WAIT_N)** - This signal is used by the AT43USB370 to assert wait states. This signal is active low.

- **BUSY (BUSY)** - This signal is used by the AT43USB370 to signal the system processor not to interrupt the AT43USB370. This signal is active high.

Interrupt Signals

- **Interrupt In (INTR_IN)** - This is an interrupt signal from the system processor to AT43USB370. This signal is active high.
- **Interrupt Out (INTR_OUT)** - This is an interrupt signal from AT43USB370 to the system processor. This signal is active high.

Programming Signals

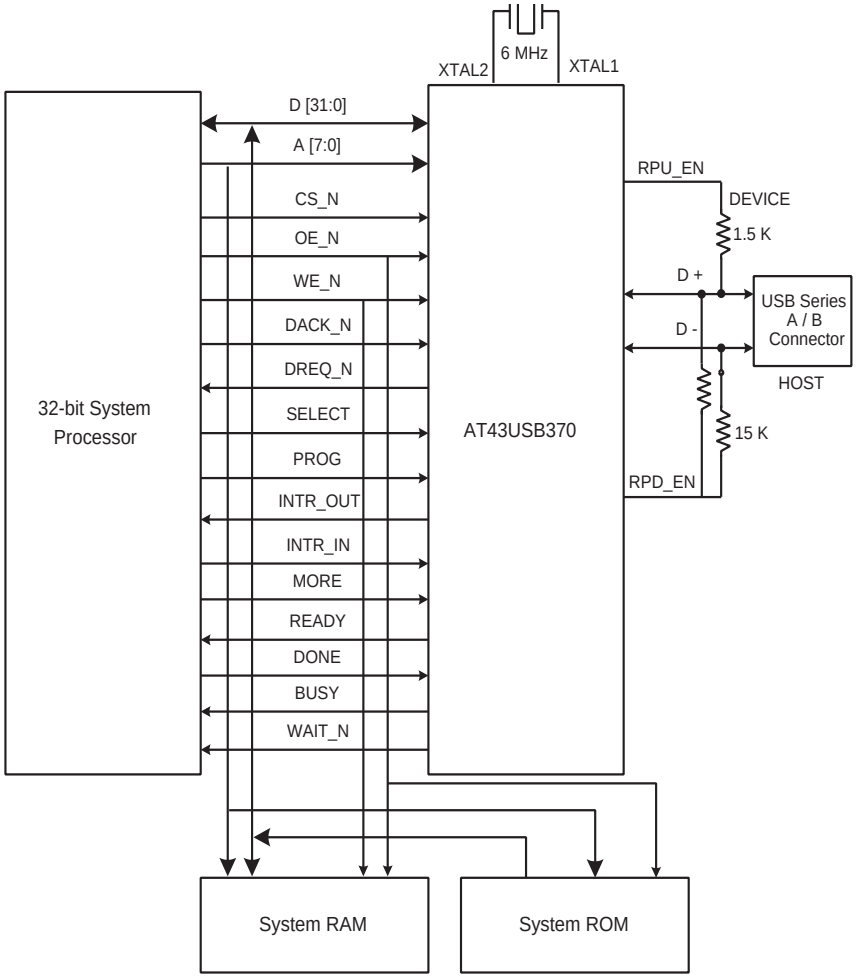
PROG, READY, DONE, SELECT - These signals are only required for programming the AT43USB370 controllers (i.e. the USB Controller and System Interface Controller) through the external system processor. The signals can be directly connected to the processor's GPIOs. These signals are active high.

DMA Signals

DREQ_N, DACK_N - These are the standard DMA control signals used by the AT43USB370 for DMA transfers with the system processor. These signals are active low.

The AT43USB370 requires external 3.3V and 1.8V power supplies. All of the AT43USB370's I/O pins are +3.3V tolerant. Figure 14 shows typical connection of AT43USB370 to a 32-bit system processor.

Figure 14. Typical AT43USB370 System Processor Connection



Electrical Specification

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings*

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	3.3V Power Supply		3.0	3.6	V
V_{IN} (3.8V)	DC Input Voltage		V_{CC} -0.3V	V_{CC} +0.3V	V
V_{IN} (1.8V)	DC Input Voltage		1.65	1.95	V
T_{ORP}	Operating Temperature		0	70	°C
T_{STG}	Storage Temperature		-40	125	°C

*Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Table 3. Power Supply

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Power Supply		3.0	3.6	V
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
VT	Switching Threshold				V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage		3.3		V
I_{OZ}	Tri-state Output Leakage Current				µA
C_{IN}	Input Pin Capacitance			7.24	pf
C_{OUT}	Output Pin Capacitance			6.07	pf
C_{IO}	I/O Capacitance			7.27	pf

AC Electrical Characteristics

System Processor Interface Timing

Table 4. AT43USB370 - System Processor Interface Timing

Symbol	Parameter	Condition	Min	Max	Units
t_{dh}	DONE Active Time		83		ns
t_{iih}	INTR_I Active Time		500		ns
t_{daf}	DMA ACK Active Time		83		ns
t_{dap}	DMA ACK Hold		104		ns
t_{dds}	Data Setup Time		21		ns
t_{wca}	CS Active to WAIT Active		125	166	ns
t_{wcn}	WAIT Inactive to CS Inactive			146	ns
t_{csn}	CS Inactive		42		ns

Reset Timing

Table 5. Reset Timing

Symbol	Parameter	Condition	Min	Max	Units
T_r	RESET Width		200		ns

Table 6. Oscillator Signals XTAL1, XTAL2

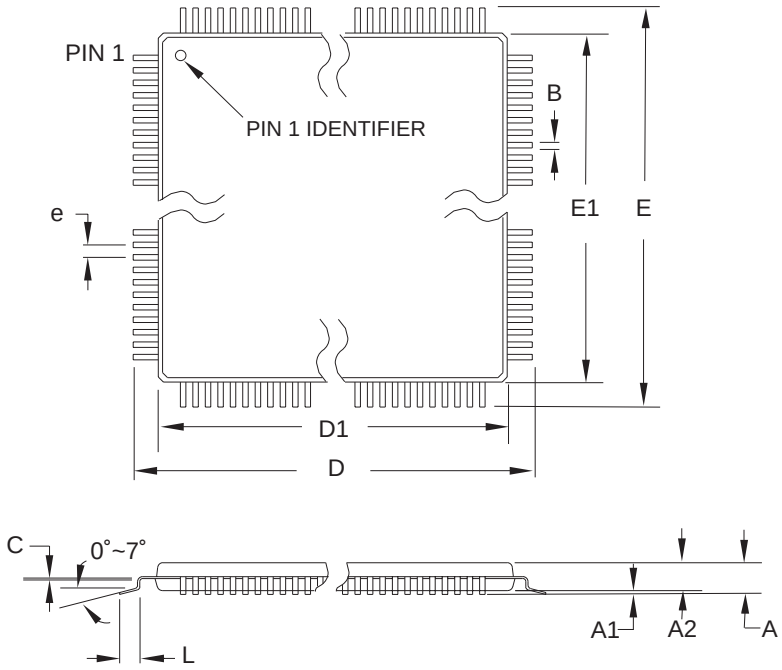
Symbol	Parameter	Condition	Min	Max	Units
V_{LH}	OSC1 Switching Level		0.47	1.20	V
V_{HL}	OSC2 Switching Level		0.67	1.44	V
CX1	Input Capacitance XTAL1			10	pf
TCX2	Output Capacitance, XTAL 2			10	pf
C12	Oscillator Capacitance			5	pf
T_{su}	Start-up Time	6 MHz, fundamental		2	ms
DL	Drive Level			50	UW

Ordering Information

Program Memory	Ordering Code	Package	Operation Range
			Commercial (0°C to 70°C)
			Commercial (0°C to 70°C)

Packaging Information

100-lead – LQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	1.35	1.40	1.45	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

04/29/2002

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100AA,** 100-lead, 14 x 14 mm Body Size, 1.4 mm Body Thickness, 0.5 mm Lead Pitch, Low Profile Quad Flat Pack (LQFP)	100AA	C

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