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Revision History

Rev 0.0	12Jul05
Rev 0.1	10Nov05
Rev 1.0	03MAR06

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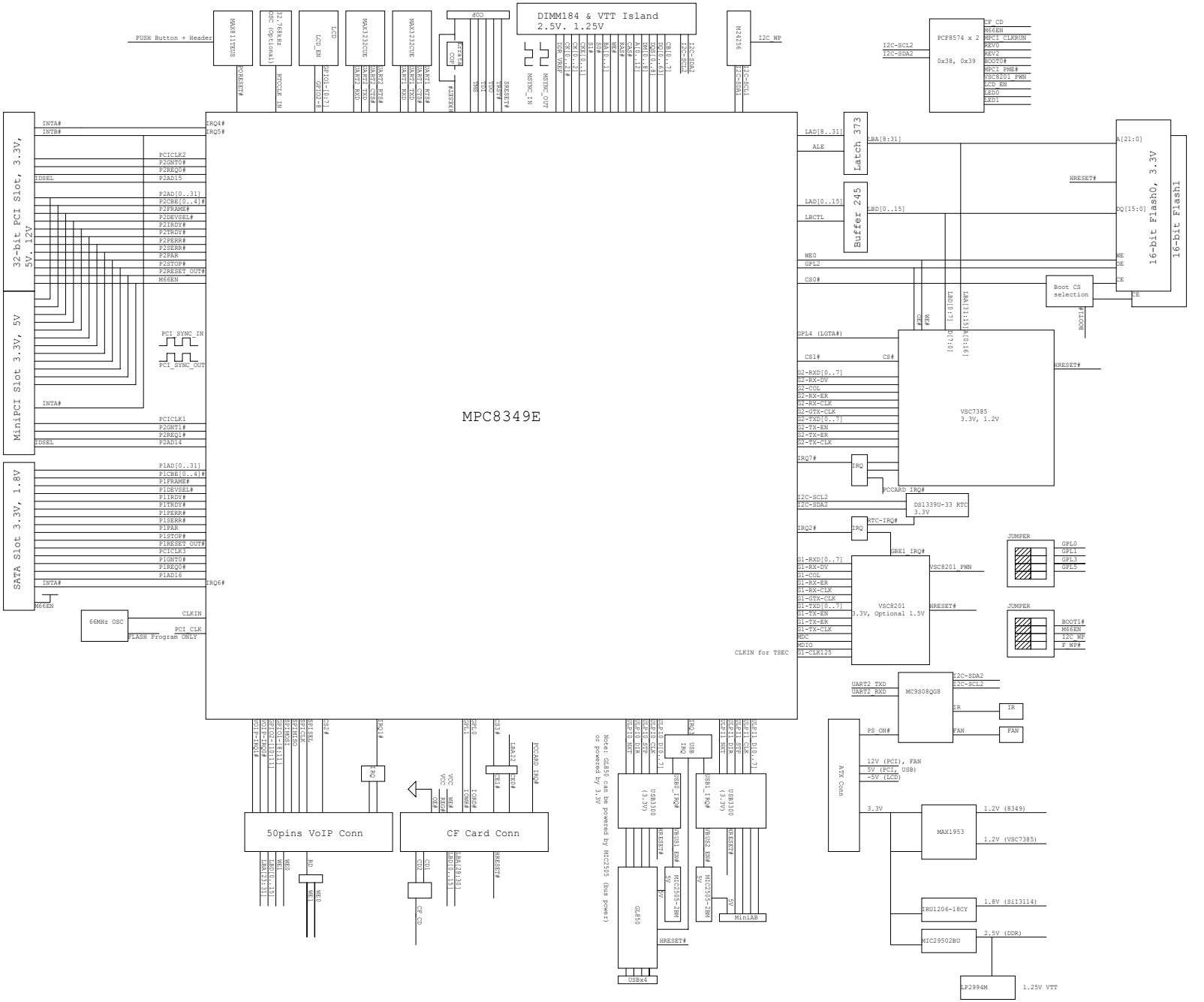
MPC8349E
DIMM184 & VTT Island
2.5V. 1.25V
32-bit PCI Slot, 3.3V, 5V. 12V
MiniPCI Slot 3.3V, 5V
SATA Slot 3.3V, 1.8V
Latch 373
Buffer 245
16-bit Flash0, 3.3V
16-bit Flash1
VSC7385
3.3V, 1.2V
VSC8201
3.3V, Optional 1.5V
DS1339U-33 RTC
3.3V
MC9S08QG8
PCF8574 x 2
0x38, 0x39
Boot CS selection
66MHz OSC
FLASH Program ONLY
50pins VoIP Conn
CF Card Conn
USB3300
(3.3V)
CH450
USBx4
ATX Conn
MAX1953
1.2V (8349)
1.2V (VSC7385)
TRU1206-18CY
1.8V (Sii3114)
MIC29502BU
2.5V (DDR)
LP2994M
1.25V VTT
MiniLAB
MIC2505-2BM
PUSH Button + Header
MAX811TEUS
12.768kHz OSC (Optional)
LCD
LCD_EN
MAX3232CUE
I2C WP
M24256
I2C-SCL2
I2C-SDA2
0x38, 0x39
CF_CD
M66EN
MPCI_CLKRUN
REV0
REV2
BOOT0#
MPCI_PME#
VSC8201_PWN
LCD_EN
LED0
LED1
HRESET#
SRESET#
PCI_SYNC_IN
PCI_SYNC_OUT
CLKIN
PCI_CLK
CLKIN for TSEC
M66EN
INTA#
INTB#
IRQ4#
IRQ5#
IRQ6#
IDSEL
P2AD15
P1AD16
PCICLK2
P2GNT0#
P2REQ0#
P2AD[0..31]
P2CBE[0..4]#
P2FRAME#
P2DEVSEL#
P2IRDY#
P2TRDY#
P2PERR#
P2SERR#
P2PAR
P2STOP#
P2RESET_OUT#
PCICLK1
P2GNT1#
P2REQ1#
P2AD14
P1AD[0..31]
P1CBE[0..4]#
P1FRAME#
P1DEVSEL#
P1IRDY#
P1TRDY#
P1PERR#
P1SERR#
P1PAR
P1STOP#
P1RESET_OUT#
PCICLK3
P1GNT0#
P1REQ0#
P1AD16
LAD[8..31]
ALE
LBA[8:31]
LAD[0..15]
LBCTL
LBD[0..15]
WE0
GPL2
CS0#
GPL4 (LGTA#)
CS1#
CS#
WR#
OE#
D[7:0]
LBA[13:15]
A[10:16]
BOOT#
G2-RXD[0..7]
G2-RX-DV
G2-COL
G2-RX-ER
G2-RX-CLK
G2-GTX-CLK
G2-TXD[0..7]
G2-TX-EN
G2-TX-ER
G2-TX-CLK
IRQ7#
IRQ
PCCARD_IRQ#
I2C-SCL2
I2C-SDA2
RTC-IRQ#
IRQ2#
GBE1_IRQ#
G1-RXD[0..7]
G1-RX-DV
G1-COL
G1-RX-ER
G1-RX-CLK
G1-GTX-CLK
G1-TXD[0..7]
G1-TX-EN
G1-TX-ER
G1-TX-CLK
MDC
MDIO
G1-CLK125
VSC8201_PWN
JUMPER
GPL0
GPL1
GPL3
GPL5
BOOT1#
M66EN
I2C_WP
F_WP#
UART2_TXD
UART2_RXD
IR
FAN
PS_ON#
12V (PCI), FAN
5V (PCI, USB)
-5V (LCD)
3.3V
IRQ1#
IRQ3
IRQ8
IRQ9
IRQ10
IRQ11
CS2#
CS3#
CS4#
CS5#
PCCARD_IRQ#
IORD#
IOWR#
VCC
OE#
WE#
CD1
CD2
CF_CD
LBA[28:30]
LBA[18:31]
LBD[0..15]
WE1
RD
WR1
USB0_IRQ#
USB1_IRQ#
VBUS1_EN#
VBUS2_EN#
5V
HRESET#
Note: CH450 can be powered by MIC2505 (bus powe) or powered by 3.3V
Title
Block Diagram
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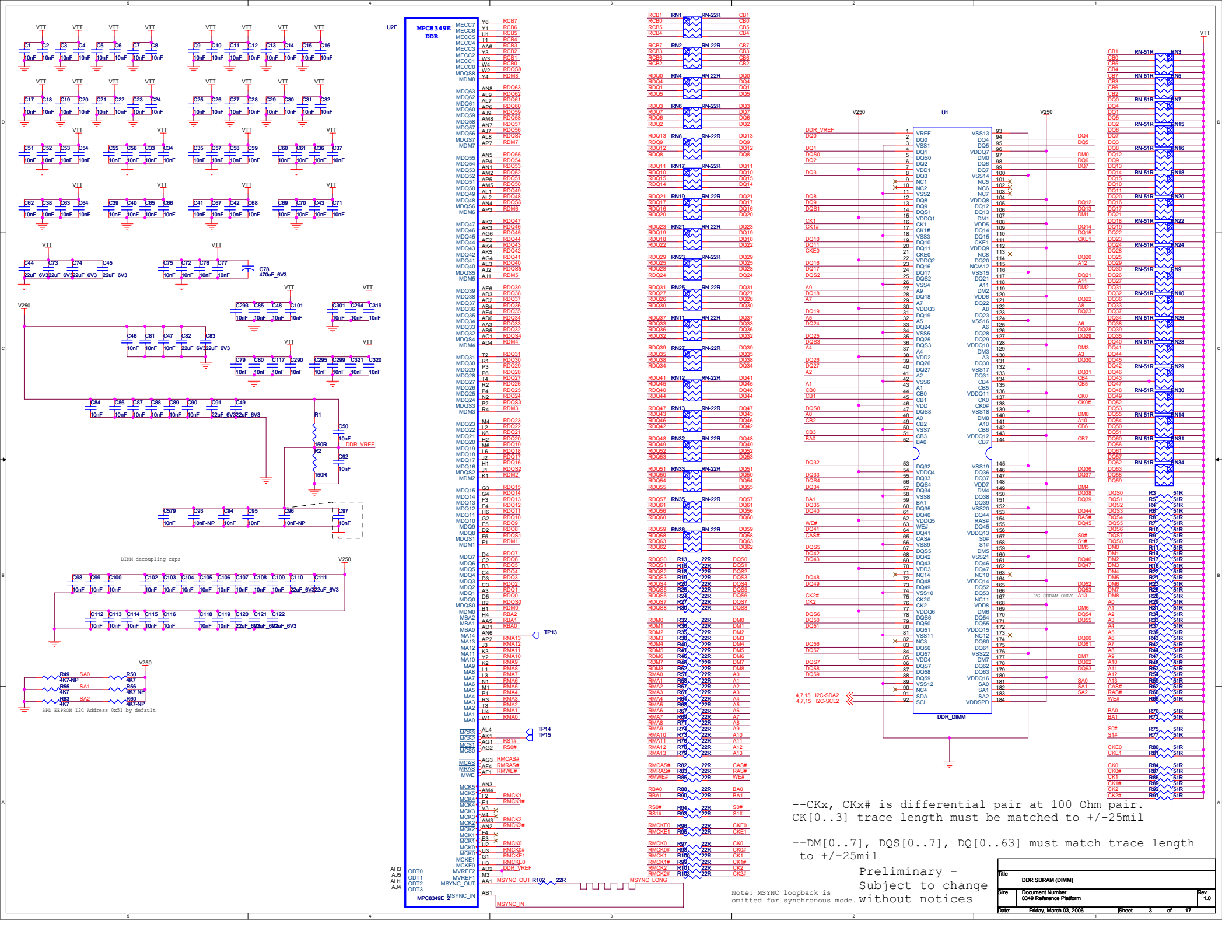
MPC8349E
DDR
U2F
MPC8349E_2
U1
DDR_DIMM
DIMM decoupling caps
SPD EEPROM I2C Address 0x51 by default
2G SDRAM ONLY
--CKx, CKx# is differential pair at 100 Ohm pair.
CK[0..3] trace length must be matched to +/-25mil
--DM[0..7], DQS[0..7], DQ[0..63] must match trace length to +/-25mil
Preliminary - Subject to change without notices
Note: MSYNC loopback is omitted for synchronous mode.
Title
DDR SDRAM (DIMM)
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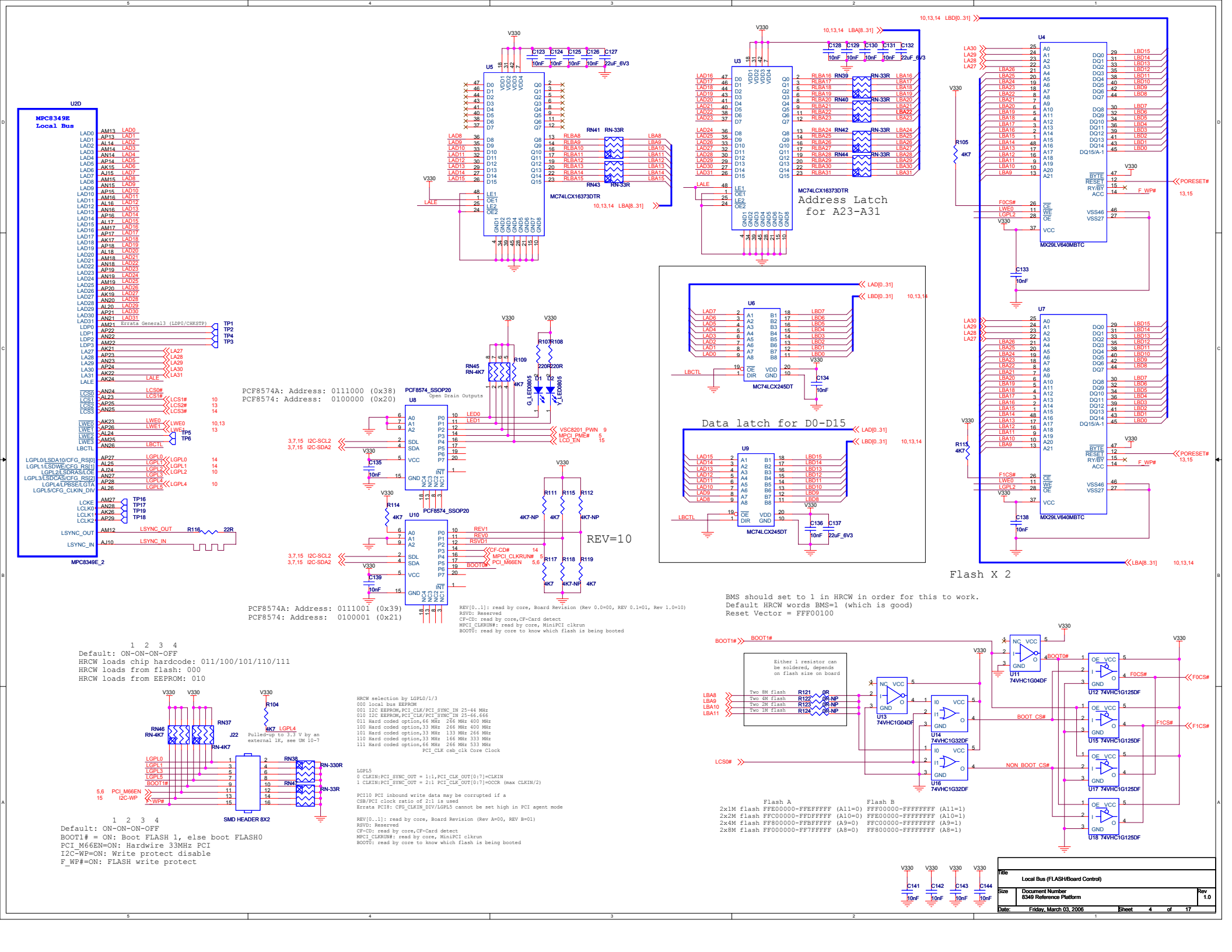
U2D
MPC8349E
Local Bus
MPC8349E_2
Errata General13 (LDP0/CHKSTP)
Address Latch
for A23-A31
MC74LCX16373DTR
Data latch for D0-D15
MC74LCX245DT
MX29LV640MBTC
Flash X 2
PCF8574A: Address: 0111000 (0x38)
PCF8574: Address: 0100000 (0x20)
PCF8574_SSOP20
Open Drain Outputs
PCF8574A: Address: 0111001 (0x39)
PCF8574: Address: 0100001 (0x21)
REV=10
REV[0..1]: read by core, Board Revision (Rev 0.0=00, REV 0.1=01, Rev 1.0=10)
RSVD: Reserved
CF-CD: read by core,CF-Card detect
MPCI_CLKRUN#: read by core, MiniPCI clkrun
BOOT0: read by core to know which flash is being booted
BMS should set to 1 in HRCW in order for this to work.
Default HRCW words BMS=1 (which is good)
Reset Vector = FFF00100
1 2 3 4
Default: ON-ON-ON-OFF
HRCW loads chip hardcode: 011/100/101/110/111
HRCW loads from flash: 000
HRCW loads from EEPROM: 010
SMD HEADER 8X2
1 2 3 4
Default: ON-ON-ON-OFF
BOOT1# = ON: Boot FLASH 1, else boot FLASH0
PCI_M66EN=ON: Hardwire 33MHz PCI
I2C-WP=ON: Write protect disable
F_WP#=ON: FLASH write protect
HRCW selection by LGPL0/1/3
000 local bus EEPROM
001 I2C EEPROM,PCI_CLK/PCI_SYNC_IN 25-44 MHz
010 I2C EEPROM,PCI_CLK/PCI_SYNC_IN 25-66.666
011 Hard coded option,66 MHz 266 MHz 400 MHz
100 Hard coded option,33 MHz 266 MHz 400 MHz
101 Hard coded option,33 MHz 133 MHz 266 MHz
110 Hard coded option,33 MHz 166 MHz 333 MHz
111 Hard coded option,66 MHz 266 MHz 533 MHz
PCI_CLK csb_clk Core Clock
LGPL5
0 CLKIN:PCI_SYNC_OUT = 1:1,PCI_CLK_OUT[0:7]=CLKIN
1 CLKIN:PCI_SYNC_OUT = 2:1 PCI_CLK_OUT[0:7]=OCCR (max CLKIN/2)
PCI10 PCI inbound write data may be corrupted if a
CSB/PCI clock ratio of 2:1 is used
Errata PCI8: CFG_CLKIN_DIV/LGPL5 cannot be set high in PCI agent mode
REV[0..1]: read by core, Board Revision (Rev A=00, REV B=01)
RSVD: Reserved
CF-CD: read by core,CF-Card detect
MPCI_CLKRUN#: read by core, MiniPCI clkrun
BOOT0: read by core to know which flash is being booted
Either 1 resistor can
be soldered, depends
on flash size on board
Flash A
Flash B
2x1M flash FFE00000-FFEFFFFF (A11=0) FFF00000-FFFFFFFF (A11=1)
2x2M flash FFC00000-FFDFFFFF (A10=0) FFE00000-FFFFFFFF (A10=1)
2x4M flash FF800000-FFBFFFFF (A9=0) FFC00000-FFFFFFFF (A9=1)
2x8M flash FF000000-FF7FFFFF (A8=0) FF800000-FFFFFFFF (A8=1)
Title
Local Bus (FLASH/Board Control)
Size
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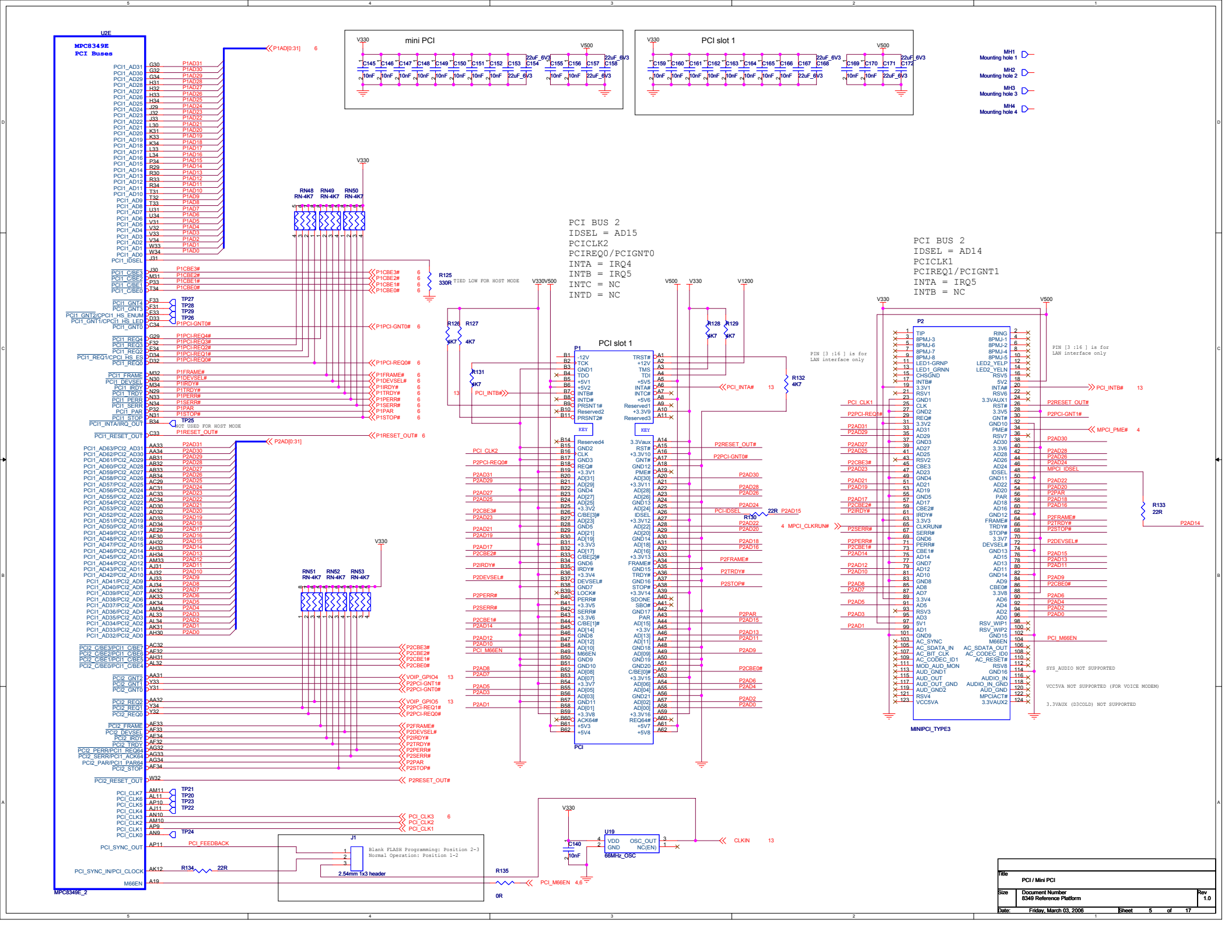
U2E
MPC8349E
PCI Buses
mini PCI
PCI slot 1
MH1 Mounting hole 1
MH2 Mounting hole 2
MH3 Mounting hole 3
MH4 Mounting hole 4
PCI BUS 2
IDSEL = AD15
PCICLK2
PCIREQ0/PCIGNT0
INTA = IRQ4
INTB = IRQ5
INTC = NC
INTD = NC
PCI BUS 2
IDSEL = AD14
PCICLK1
PCIREQ1/PCIGNT1
INTA = IRQ5
INTB = NC
PCI slot 1
P2
MINIPCI_TYPE3
J1
Blank FLASH Programming: Position 2-3
Normal Operation: Position 1-2
2.54mm 1x3 header
U19
66MHz_OSC
MPC8349E_2
PCI / Mini PCI
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PCI BUS 1
IDSEL = AD16
PCICLK3
PCIREQ0/PCIGNT0
INTA = IRQ6

U20

sil3114

Sata Connector-internal

P3

P4

P6

P8

TOP View of SATA Connector

Not populated, 25MHz provided by VSC7385 OSC

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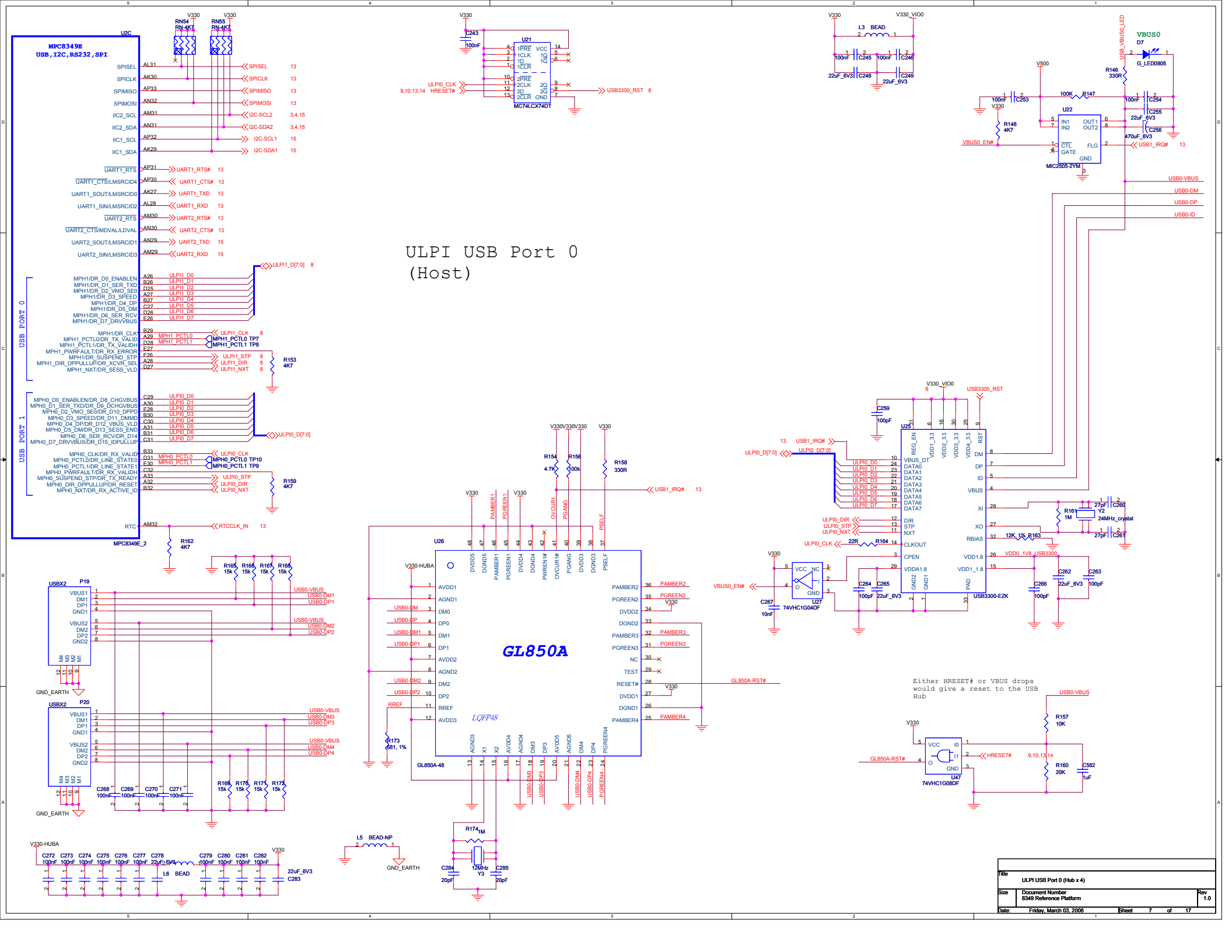
ULPI USB Port 0
(Host)
MPC8349E
USB,I2C,RS232,SPI
U2C
MPC8349E_2
USB_PORT_0
USB_PORT_1
GL850A
LQFP48
GL850A-48
U26
U25
USB3300-EZK
U21
MC74LCX74DT
U22
MIC2505-2YM
U27
74VHC1G04DF
U47
74VHC1G08DF
Y2
24MHz_crystal
Y3
12MHz
VBUS0
G_LED0805
USBX2 P19
USBX2 P20
GND_EARTH
V330-HUBA
Either HRESET# or VBUS drops would give a reset to the USB Hub
Title
ULPI USB Port 0 (Hub x 4)
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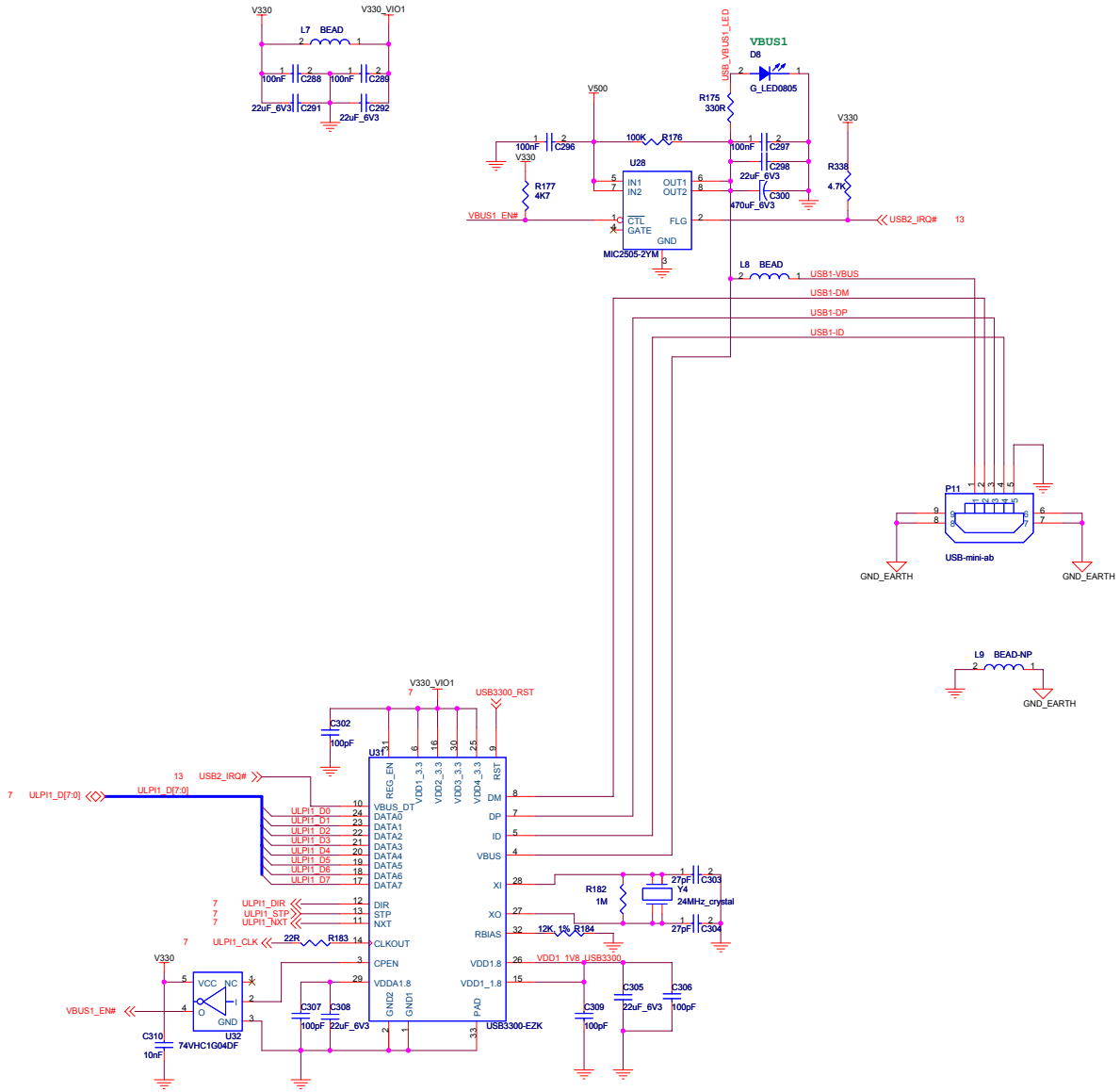

ULPI USB Port 1 (Host/Device/OTG)

Title	ULPI USB Port 1 (host/device/otg)	
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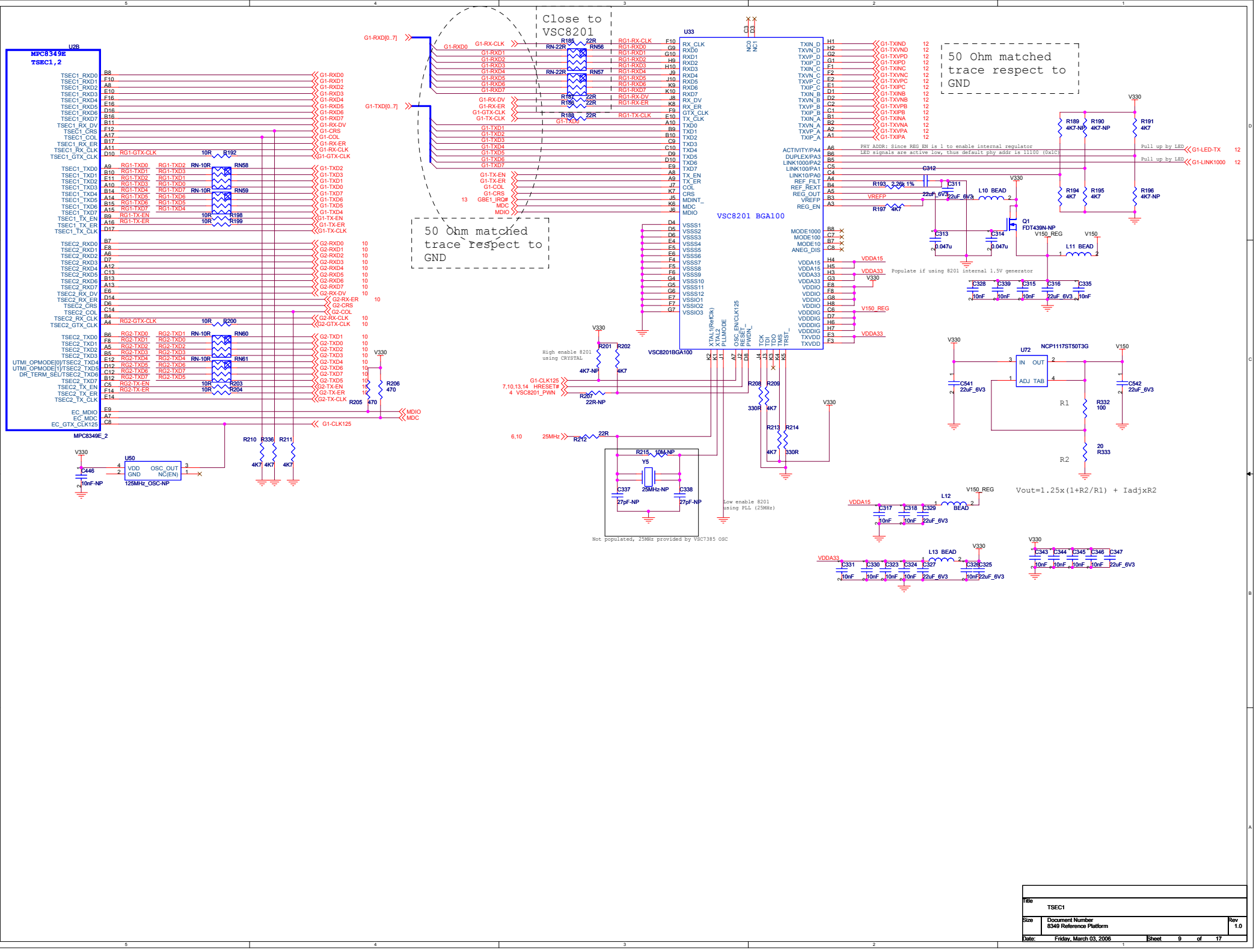
Close to VSC8201
50 Ohm matched trace respect to GND
50 Ohm matched trace respect to GND
MPC8349E TSEC1,2
MPC8349E_2
VSC8201 BGA100
VSC8201BGA100
NCP1117ST50T3G
Vout=1.25x(1+R2/R1) + IadjxR2
High enable 8201 using CRYSTAL
Low enable 8201 using PLL (25MHz)
Not populated, 25MHz provided by VSC7385 OSC
PHY ADDR: Since REG_EN is 1 to enable internal regulator
LED signals are active low, thus default phy addr is 11100 (0x1C)
Populate if using 8201 internal 1.5V generator
125MHz_OSC-NP
Title
TSEC1
Size
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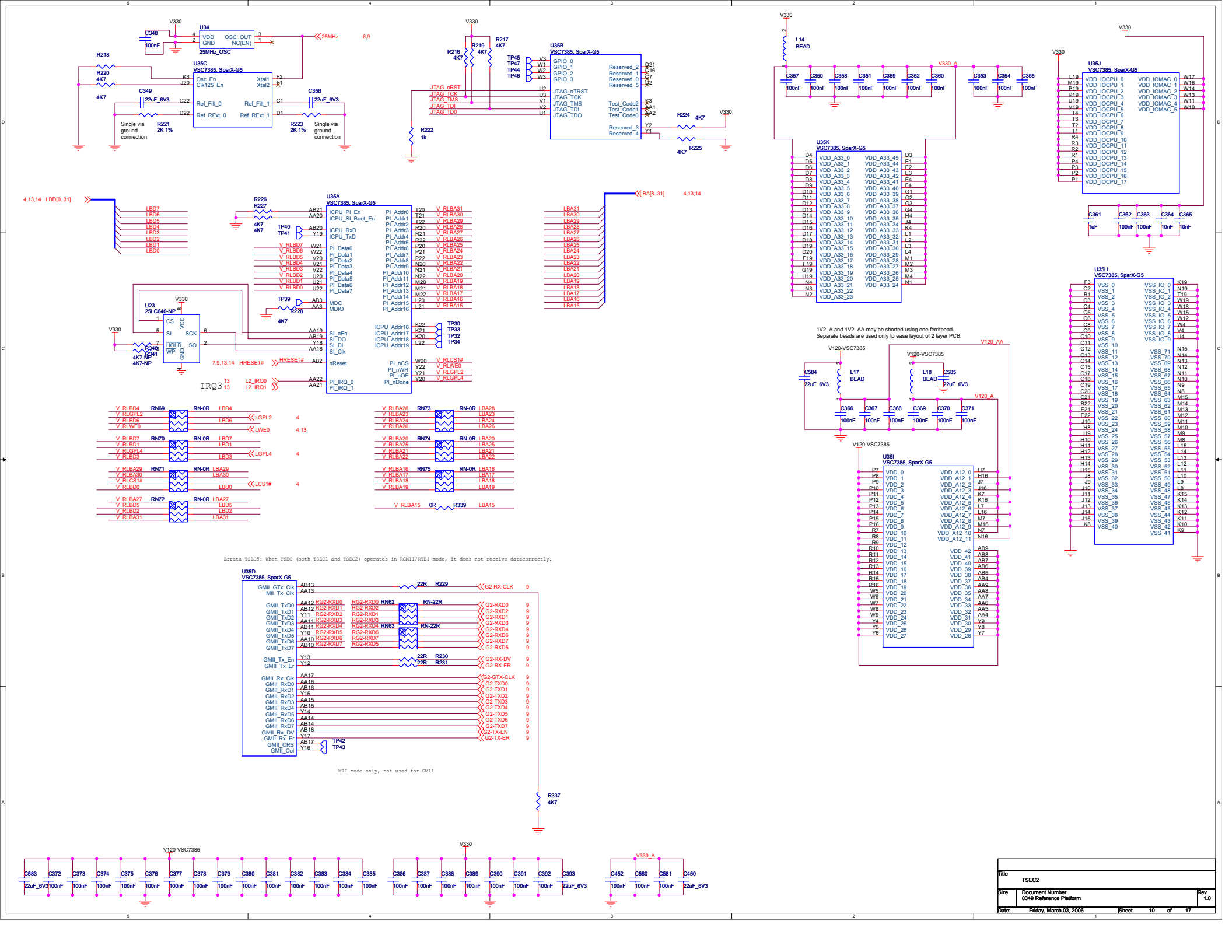
U34
VSC7385, SparX-G5
25MHz_OSC
U35C
U35B
U35A
U35D
U35K
U35J
U35H
U35I
L14 BEAD
L17 BEAD
L18 BEAD
U23 25LC640-NP
Errata TSEC5: When TSEC (both TSEC1 and TSEC2) operates in RGMII/RTBI mode, it does not receive datacorrectly.
MII mode only, not used for GMII
1V2_A and 1V2_AA may be shorted using one ferritbead.
Separate beads are used only to ease layout of 2 layer PCB.
Title
TSEC2
Size
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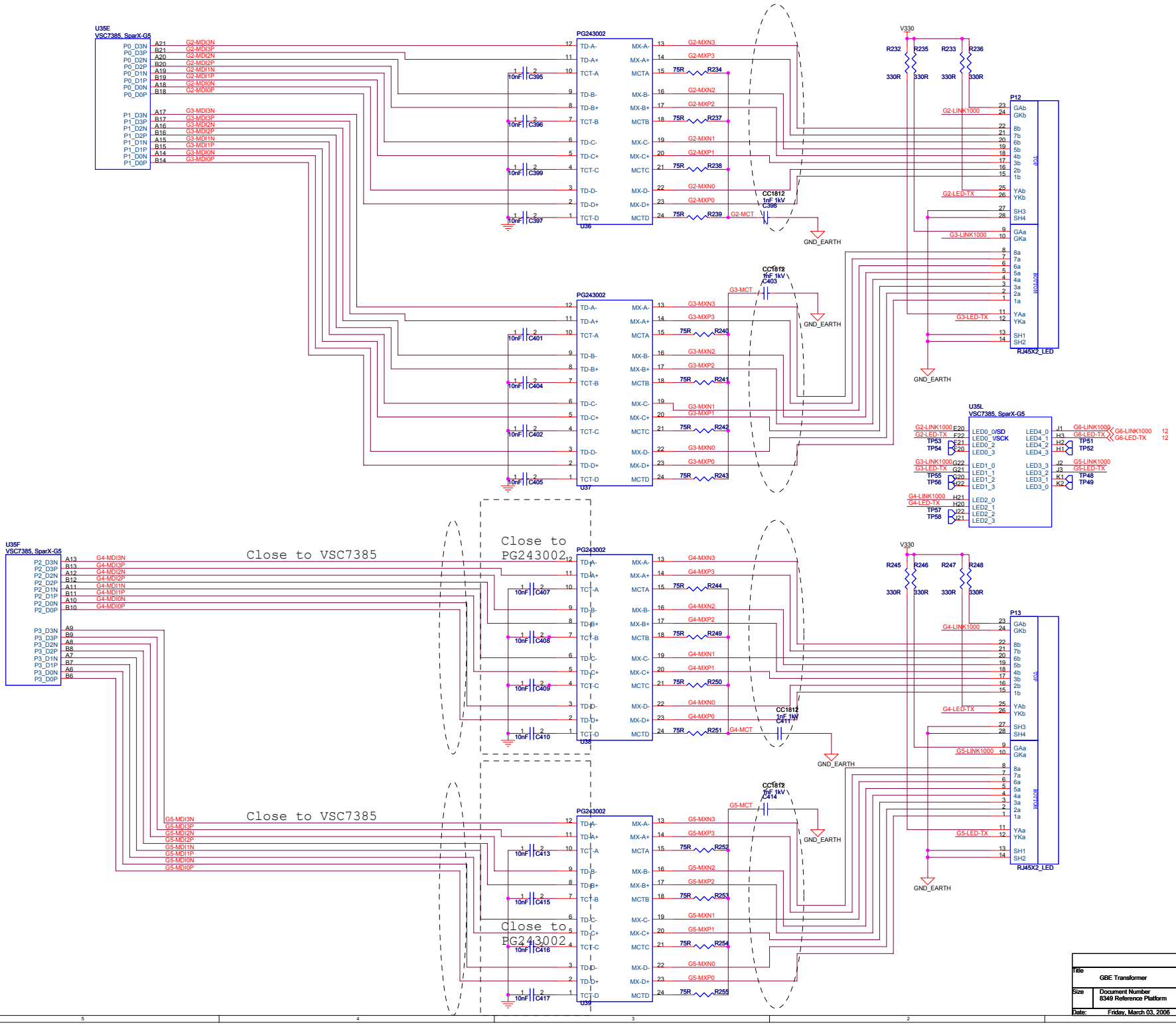
U35E
VSC7385, SparX-G5
P0_D3N
P0_D3P
P0_D2N
P0_D2P
P0_D1N
P0_D1P
P0_D0N
P0_D0P
P1_D3N
P1_D3P
P1_D2N
P1_D2P
P1_D1N
P1_D1P
P1_D0N
P1_D0P
G2-MDI3N
G2-MDI3P
G2-MDI2N
G2-MDI2P
G2-MDI1N
G2-MDI1P
G2-MDI0N
G2-MDI0P
G3-MDI3N
G3-MDI3P
G3-MDI2N
G3-MDI2P
G3-MDI1N
G3-MDI1P
G3-MDI0N
G3-MDI0P
PG243002
TD-A-
TD-A+
TCT-A
TD-B-
TD-B+
TCT-B
TD-C-
TD-C+
TCT-C
TD-D-
TD-D+
TCT-D
MX-A-
MX-A+
MCTA
MX-B-
MX-B+
MCTB
MX-C-
MX-C+
MCTC
MX-D-
MX-D+
MCTD
G2-MXN3
G2-MXP3
G2-MXN2
G2-MXP2
G2-MXN1
G2-MXP1
G2-MXN0
G2-MXP0
G2-MCT
75R
R234
R237
R238
R239
10nF
C395
C396
C399
C397
U36
CC1812
1nF 1kV
C398
GND_EARTH
V330
R232
R235
R233
R236
330R
P12
RJ45X2_LED
G2-LINK1000
G2-LED-TX
G3-LINK1000
G3-LED-TX
G3-MCT
C403
C401
C404
C402
C405
U37
G3-MXN3
G3-MXP3
G3-MXN2
G3-MXP2
G3-MXN1
G3-MXP1
G3-MXN0
G3-MXP0
R240
R241
R242
R243
U35L
VSC7385, SparX-G5
LED0_0/SD
LED0_1/SCK
LED0_2
LED0_3
LED1_0
LED1_1
LED1_2
LED1_3
LED2_0
LED2_1
LED2_2
LED2_3
LED4_0
LED4_1
LED4_2
LED4_3
LED3_3
LED3_2
LED3_1
LED3_0
G6-LINK1000
G6-LED-TX
G5-LINK1000
G5-LED-TX
G4-LINK1000
G4-LED-TX
TP53
TP54
TP55
TP56
TP57
TP58
TP51
TP52
TP48
TP49
U35F
VSC7385, SparX-G5
P2_D3N
P2_D3P
P2_D2N
P2_D2P
P2_D1N
P2_D1P
P2_D0N
P2_D0P
P3_D3N
P3_D3P
P3_D2N
P3_D2P
P3_D1N
P3_D1P
P3_D0N
P3_D0P
G4-MDI3N
G4-MDI3P
G4-MDI2N
G4-MDI2P
G4-MDI1N
G4-MDI1P
G4-MDI0N
G4-MDI0P
G5-MDI3N
G5-MDI3P
G5-MDI2N
G5-MDI2P
G5-MDI1N
G5-MDI1P
G5-MDI0N
G5-MDI0P
Close to VSC7385
Close to PG243002
Close to VSC7385
Close to PG243002
G4-MXN3
G4-MXP3
G4-MXN2
G4-MXP2
G4-MXN1
G4-MXP1
G4-MXN0
G4-MXP0
G4-MCT
R244
R249
R250
R251
C407
C408
C409
C410
C411
U38
G5-MXN3
G5-MXP3
G5-MXN2
G5-MXP2
G5-MXN1
G5-MXP1
G5-MXN0
G5-MXP0
G5-MCT
R252
R253
R254
R255
C413
C415
C416
C417
C414
U39
R245
R246
R247
R248
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GBE Transformer
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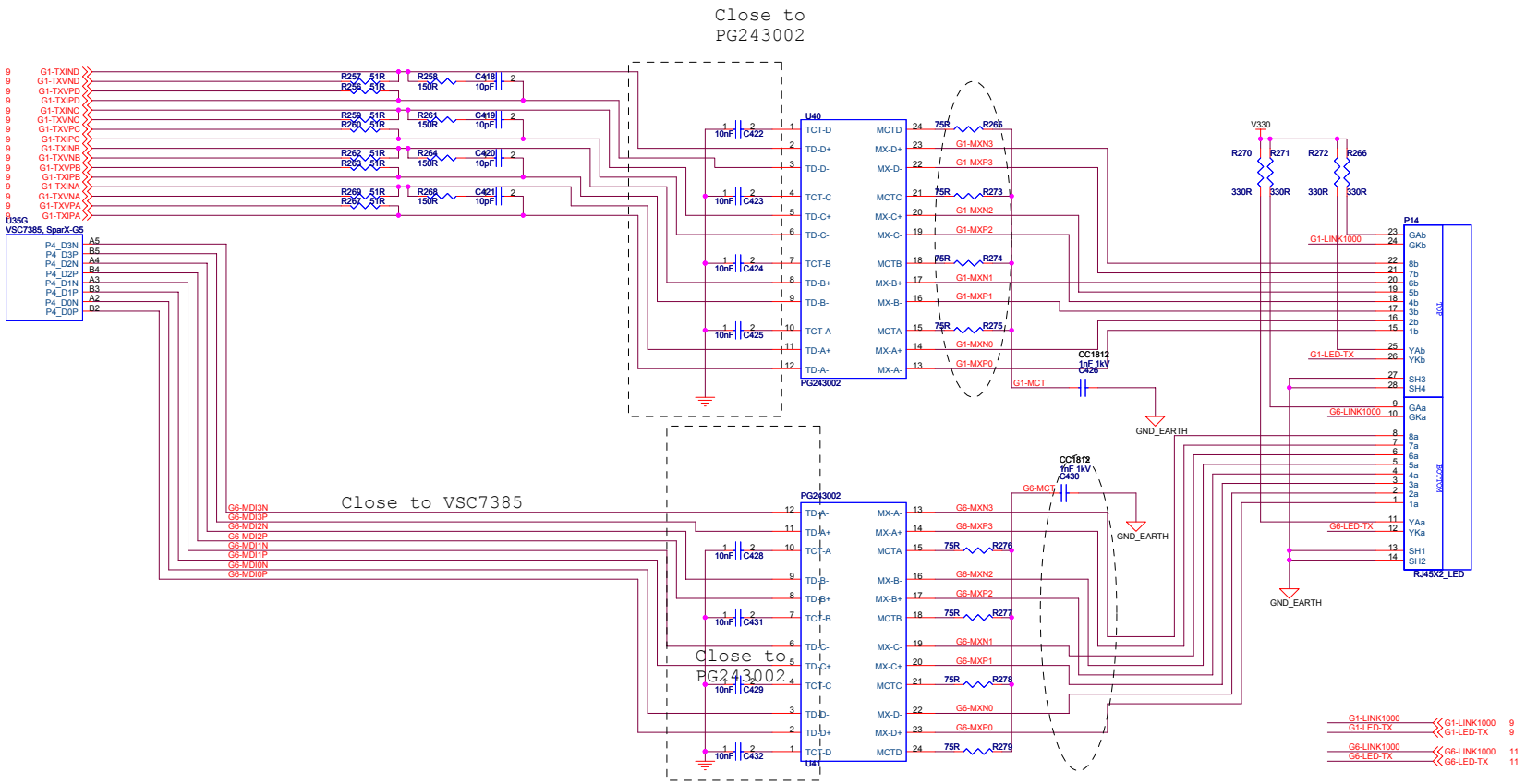

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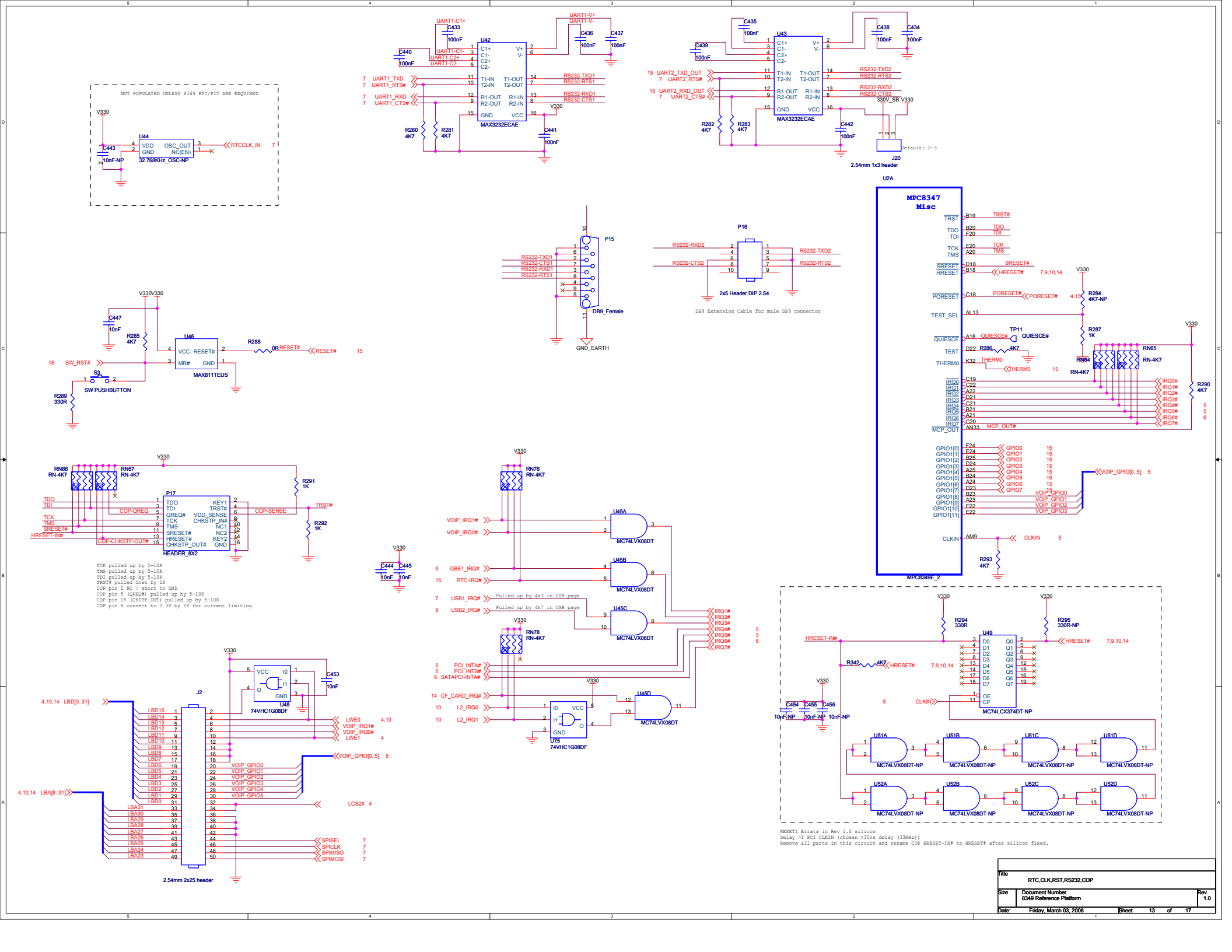
NOT POPULATED UNLESS 8349 RTC/PIT ARE REQUIRED
V330
U44
VDD
GND
OSC_OUT
NC(EN)
RTCCLK_IN
C443
10nF-NP
32.768KHz_OSC-NP
UART1-C1+
UART1-C1-
UART1-C2+
UART1-C2-
C433
C440
100nF
U42
C1+
C1-
C2+
C2-
V+
V-
T1-IN
T2-IN
T1-OUT
T2-OUT
R1-OUT
R2-OUT
R1-IN
R2-IN
GND
VCC
MAX3232ECAE
UART1-V+
UART1-V-
C436
C437
UART1_TXD
UART1_RTS#
UART1_RXD
UART1_CTS#
RS232-TXD1
RS232-RTS1
RS232-RXD1
RS232-CTS1
R280
4K7
R281
4K7
C441
C435
C439
C438
C434
U43
UART2_TXD_OUT
UART2_RTS#
UART2_RXD_OUT
UART2_CTS#
RS232-TXD2
RS232-RTS2
RS232-RXD2
RS232-CTS2
R282
4K7
R283
4K7
C442
330V_SB
V330
J20
Default: 2-3
2.54mm 1x3 header
U2A
MPC8347
Misc
TRST
TDO
TDI
TCK
TMS
SRESET
HRESET
PORESET
TEST_SEL
QUIESCE
TEST
THERM0
IRQ0
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
MCP_OUT
CLKIN
TRST#
TDO
TDI
TCK
TMS
SRESET#
HRESET#
PORESET#
QUIESCE#
TP11
R286
4K7
THERM0
R284
4K7-NP
R287
1K
RN65
RN64
RN-4K7
IRQ0#
IRQ1#
IRQ2#
IRQ3#
IRQ4#
IRQ5#
IRQ6#
IRQ7#
R290
4K7
GPIO1[0]
GPIO1[1]
GPIO1[2]
GPIO1[3]
GPIO1[4]
GPIO1[5]
GPIO1[6]
GPIO1[7]
GPIO1[8]
GPIO1[9]
GPIO1[10]
GPIO1[11]
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
VOIP_GPIO0
VOIP_GPIO1
VOIP_GPIO2
VOIP_GPIO3
VOIP_GPIO[0..5]
AM9
R293
4K7
MPC8349E_2
P15
DB9_Female
GND_EARTH
RS232-TXD1
RS232-CTS1
RS232-RXD1
RS232-RTS1
P16
RS232-RXD2
RS232-CTS2
RS232-TXD2
RS232-RTS2
2x5 Header DIP 2.54
DB9 Extension Cable for male DB9 connector
V330
C447
10nF
R285
4K7
U46
VCC
MR#
RESET#
GND
MAX811TEUS
R288
0R
RESET#
SW_RST#
S3
SW PUSHBUTTON
R289
330R
RN66
RN-4K7
RN67
RN-4K7
P17
TDO
TDI
TCK
TMS
SRESET#
HRESET-IN#
COP-QREQ
COP-CHKSTP-OUT#
KEY1
TRST#
QREQ#
VDD_SENSE
CHKSTP_IN#
NC1
NC2
KEY2
CHKSTP_OUT#
COP-SENSE
HEADER_8X2
R291
1K
R292
1K
TCK pulled up by 5-10K
TMS pulled up by 5-10K
TDI pulled up by 5-10K
TRST# pulled down by 1K
COP pin 2 NC / short to GND
COP pin 3 (QREQ#) pulled up by 5-10K
COP pin 15 (CKSTP_OUT) pulled up by 5-10K
COP pin 6 connect to 3.3V by 1K for current limiting
C444
C445
10nF
10nF
RN76
RN-4K7
VOIP_IRQ1#
VOIP_IRQ0#
U45A
U45B
U45C
U45D
MC74LVX08DT
GBE1_IRQ#
RTC-IRQ#
USB1_IRQ#
USB2_IRQ#
Pulled up by 4k7 in USB page
RN78
RN-4K7
PCI_INTA#
PCI_INTB#
SATAPCI-INTA#
CF_CARD_IRQ#
L2_IRQ0
L2_IRQ1
U75
74VHC1G08DF
C453
10nF
U48
74VHC1G08DF
J2
4,10,14 LBD[0..31]
4,10,14 LBA[8..31]
LBD15
LBD14
LBD13
LBD12
LBD11
LBD10
LBD9
LBD8
LBD7
LBD6
LBD5
LBD4
LBD3
LBD2
LBD1
LBD0
LBA31
LBA30
LBA29
LBA28
LBA27
LBA26
LBA25
LBA24
LBA23
LWE0
VOIP_IRQ1#
VOIP_IRQ0#
LWE1
VOIP_GPIO0
VOIP_GPIO1
VOIP_GPIO2
VOIP_GPIO3
VOIP_GPIO4
VOIP_GPIO5
LCS2#
SPISEL
SPICLK
SPIMISO
SPIMOSI
2.54mm 2x25 header
R294
330R
R295
330R-NP
HRESET-IN#
R342
4K7
HRESET#
U49
MC74LCX374DT-NP
C454
C455
C456
10nF-NP
U51A
U51B
U51C
U51D
U52A
U52B
U52C
U52D
MC74LVX08DT-NP
RESET1 Errata in Rev 1.0 silicon
Delay >1 PCI CLKIN (chosen >30ns delay (33MHz))
Remove all parts in this circuit and rename COP HRESET-IN# to HRESET# after silicon fixed.
Title
RTC,CLK,RST,RS232,COP
Size
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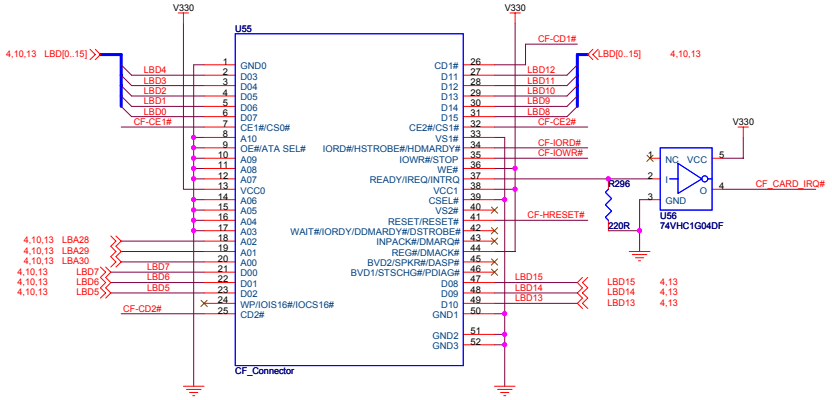
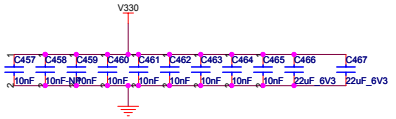
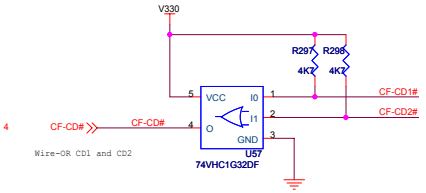
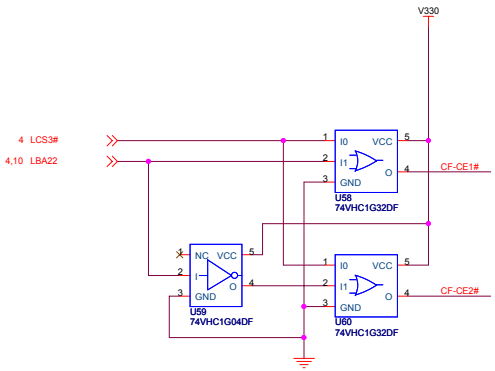






CF in True IDE Mode

83xx	CF
LBCS3#	CE1#
LBCS3#	CE2#
LBD[7:0]	D[0:7]
LBD[15:8]	D[8:15]
LBA[30..28]	A[0..2]
VCC	REG#
VCC	WE#
GND	ATA_SEL#/OE#
IRQ7#	CF_CARD_IRQ#
LBGPL0	IORD#
LBGPL1	IOWR#




```
CE2# CE1# Addr.  Read (IORD# = L) Write (IOWR# = L)
=============================================================
1 0 0xnnnnn000 Data Register (16 bit) Data Register (16 bit)
1 0 0xnnnnn002 Error Register  Feature Register
1 0 0xnnnnn004 Sector Count Register Sector Count Register
1 0 0xnnnnn006 Sector Number Register Sector Number Register
1 0 0xnnnnn008 Cylinder Low Register Cylinder Low Register
1 0 0xnnnnn00a Cylinder High Register Cylinder High Register
1 0 0xnnnnn00c Drive Head Register Drive Head Register
1 0 0xnnnnn00e Status Register  Command Register
0 1 0xnnnnn20c Alt. Status Register Device Control Register
0 1 0xnnnnn20e Drive Address Register Reserved
```

Title	Compact Flash		
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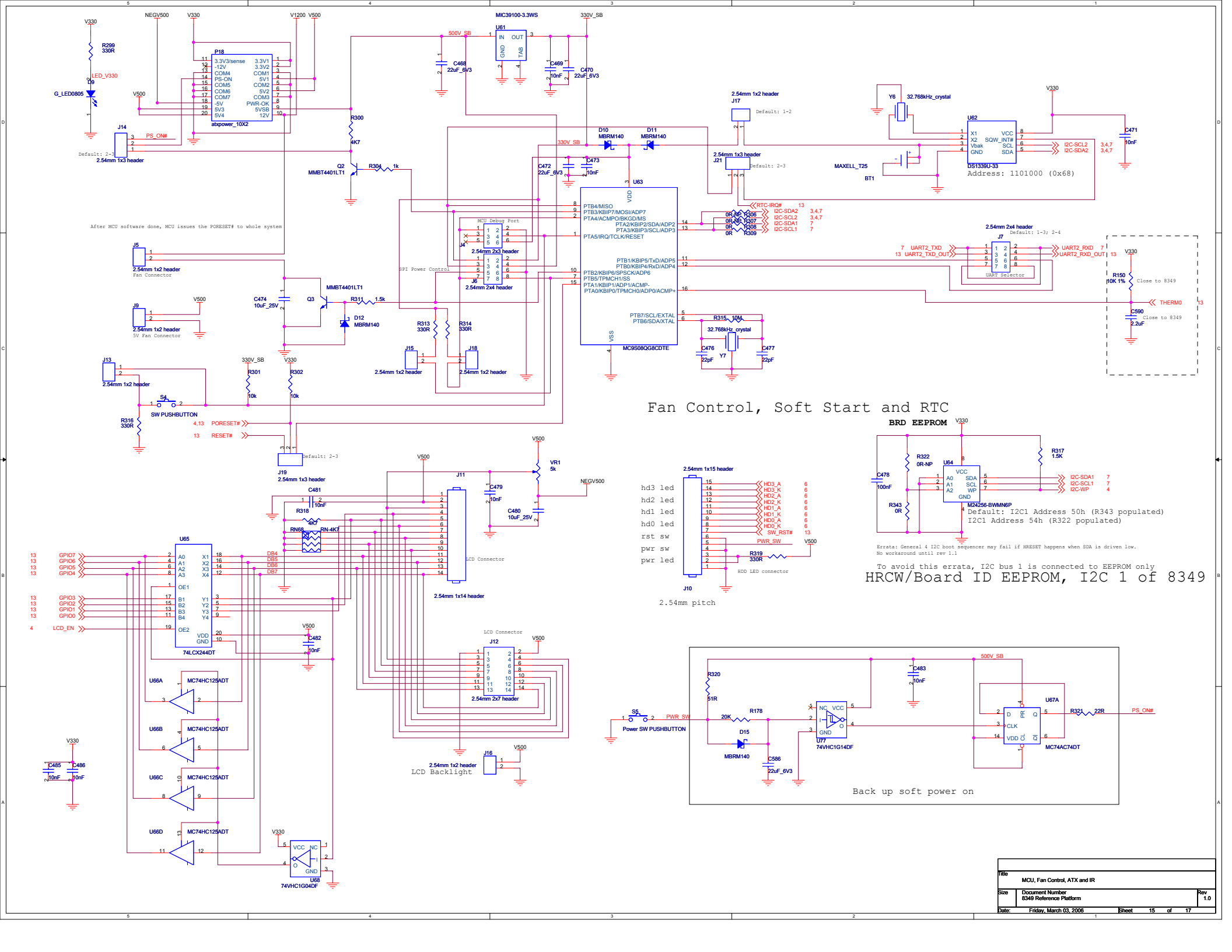
Fan Control, Soft Start and RTC
HRCW/Board ID EEPROM, I2C 1 of 8349
Back up soft power on
2.54mm pitch
Address: 1101000 (0x68)
Default: I2C1 Address 50h (R343 populated)
I2C1 Address 54h (R322 populated)
To avoid this errata, I2C bus 1 is connected to EEPROM only
Errata: General 4 I2C boot sequencer may fail if HRESET happens when SDA is driven low.
No workaround until rev 1.1
After MCU software done, MCU issues the PORESET# to whole system
Close to 8349
Title
MCU, Fan Control, ATX and IR
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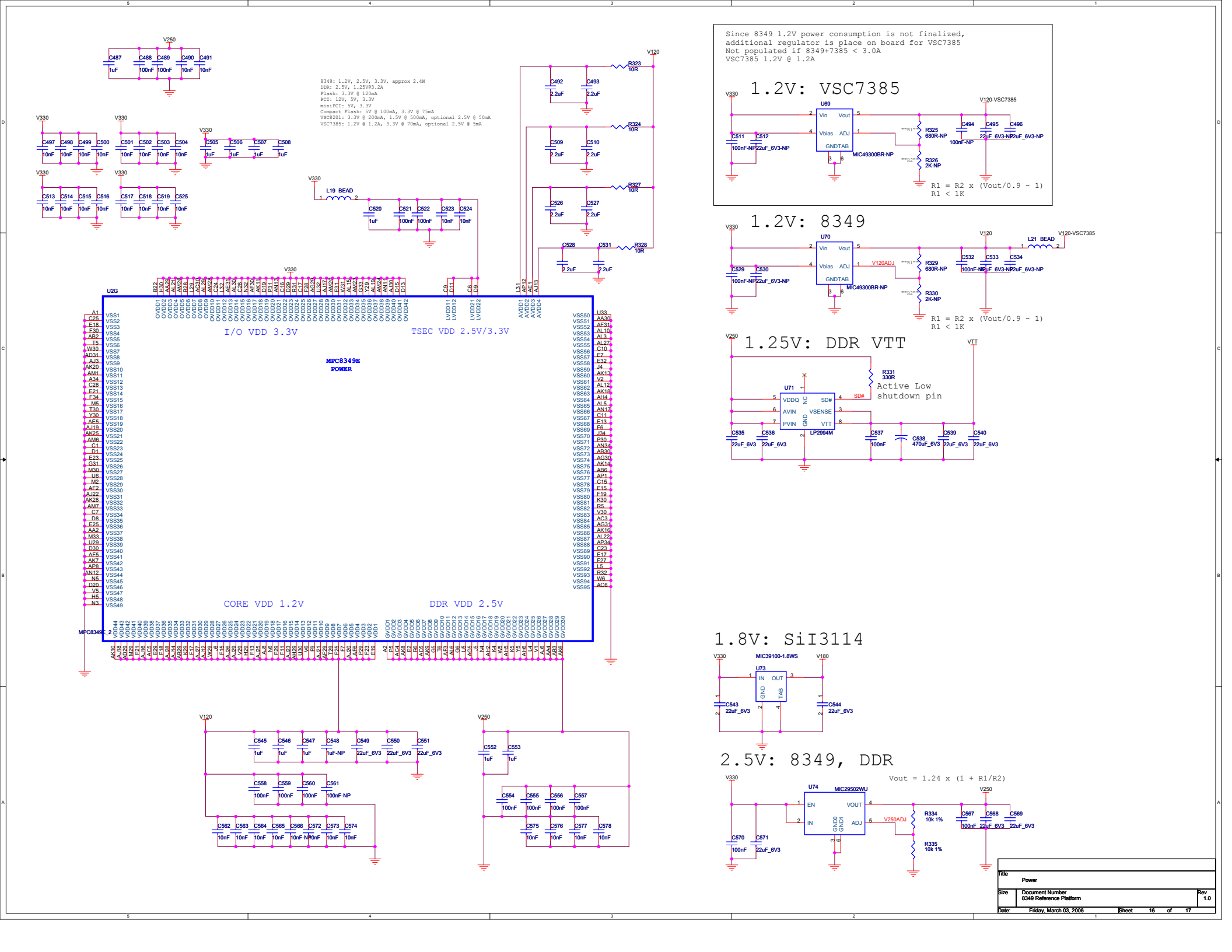
Since 8349 1.2V power consumption is not finalized,
additional regulator is place on board for VSC7385
Not populated if 8349+7385 < 3.0A
VSC7385 1.2V @ 1.2A
1.2V: VSC7385
U69
MIC49300BR-NP
R1 = R2 x (Vout/0.9 - 1)
R1 < 1K
1.2V: 8349
U70
MIC49300BR-NP
R1 = R2 x (Vout/0.9 - 1)
R1 < 1K
1.25V: DDR VTT
U71
LP2994M
R331
330R
Active Low
shutdown pin
8349: 1.2V, 2.5V, 3.3V, approx 2.4W
DDR: 2.5V, 1.25V@3.2A
Flash: 3.3V @ 120mA
PCI: 12V, 5V, 3.3V
miniPCI: 5V, 3.3V
Compact Flash: 5V @ 100mA, 3.3V @ 75mA
VSC8201: 3.3V @ 200mA, 1.5V @ 500mA, optional 2.5V @ 50mA
VSC7385: 1.2V @ 1.2A, 3.3V @ 70mA, optional 2.5V @ 5mA
U2G
MPC8349E
POWER
I/O VDD 3.3V
TSEC VDD 2.5V/3.3V
CORE VDD 1.2V
DDR VDD 2.5V
1.8V: SiI3114
U73
MIC39100-1.8WS
2.5V: 8349, DDR
U74
MIC29502WU
Vout = 1.24 x (1 + R1/R2)
Power
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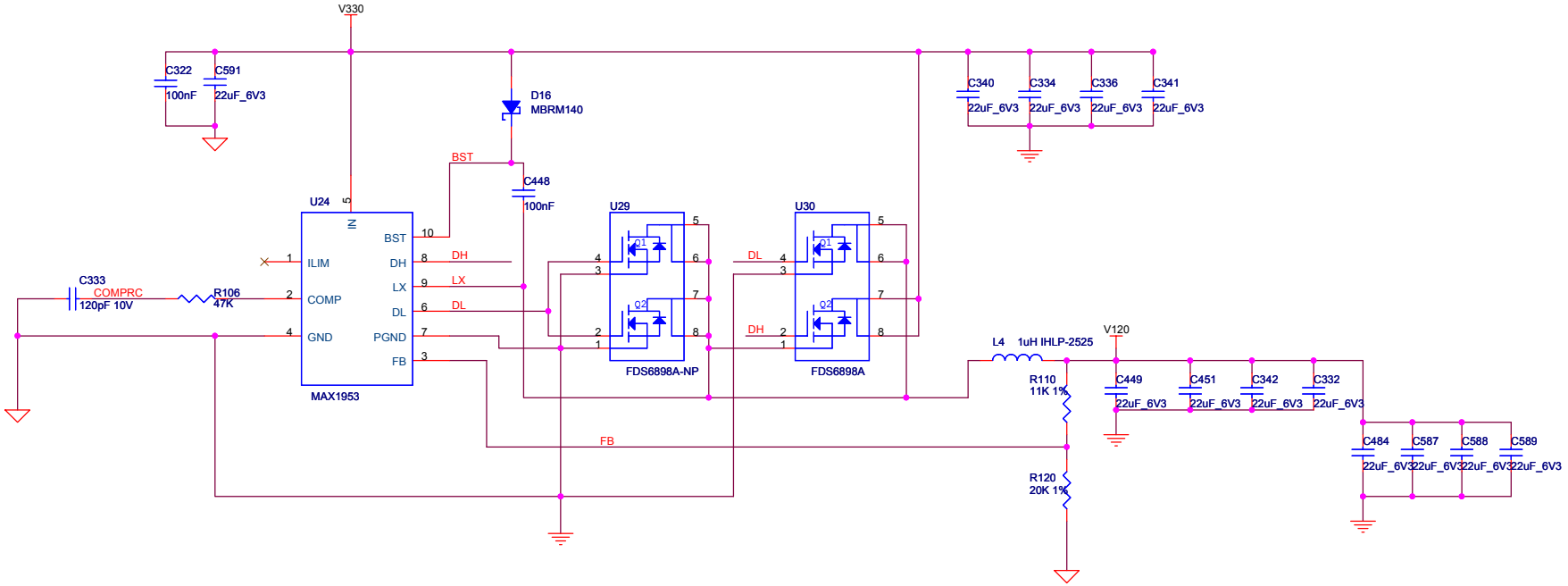

Vout = (R1/R2 +1) X 0.8

Title: Power		
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