CMOS RFIC ARCHITECTURES FOR IEEE 802.15.4 NETWORKS

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ABSTRACT

While the wireless industry has been focusing on increasing high data throughput, the emerging IEEE 802.15.4 (ZigBee) protocol targets a set of applications that require simple wireless connectivity, relaxed throughput, very low power consumption, and lower module cost. This article will summarize the 2.4 GHz radio physical layer (PHY) technical specifications, examine alternative modem implementations, and compare possible architectures for the receiver and the transmitter in terms of performance, estimated chip area, and production cost.

1. INTRODUCTION

The rapid growth experienced by the wireless communication sector in recent years is conspicuous. Wireless networking technologies have followed suit owing to the adoption of services where data is shared and exchanged, with the requirements for such technologies driven by the need for larger data throughput. This however has left a number of low-rate, low-power sensing and monitoring applications, including those in the agricultural, industrial, public safety, residential, vehicular, and related sectors, underserved by the proliferation of wireless technology that is expensive, protocol-rich and power-hungry. The 802.15.4 protocol aims to provide a low cost, standards-based (Ethernet) solution to low-rate wireless network connectivity [1] [2], and potentially could become a unifying element in the telemetry market analogous to the success of 802.11 networks in the WLAN arena.

Also known as ZigBee, the specifications of the physical (PHY) and media access control (MAC) layers for low-rate personal area networks (LR-PAN), have been under review by Task Group 4 of the IEEE 802.15 Wireless Personal Area Network Working Group since December 2000. The current draft standard proposes twenty-seven frequency channels available across three bands, with this discussion focused on the link parameters of the 2.4 GHz PHY.

The radio air interface uses a direct sequence spread spectrum (DSSS) method operating in the 2.4 GHz Industrial, Scientific, and Medical (ISM) band. The 2.4 GHz PHY allocates 16 channels from 2.405 to 2.480 GHz, with 5 MHz channel spacing specified for relaxed transmit and receive filter requirements. The occupied spectrum is 2 MHz per channel with a transmission rate of 250 kb/s. While there is no frequency hopping, hooks are provided to implement dynamic channel selection.

The modulation selected for ZigBee is Offset Quadrature Phase Shift Keying (O-QPSK) with half-sine pulse shaping which is equivalent to Minimum Shift Keying (MSK) [3] [4]. The benefit of this constant envelope modulation is the flexibility to use simple, low-cost, and less linear power amplifiers in the transmit chain. Binary data is coded into 4-bit symbols (16-ary) where each symbol contains a nearly orthogonal 32-bit pseudo-noise (PN) sequence transmitted at a 2.0 Mchips/s rate.

2. MODULATION/DEMODULATION APPROACHES

Key to offering the architectural options proposed in this paper is a detailed understanding of the IEEE 802.15.4 carrier modulation format (O-QPSK with half-sine shaping, aka MSK) and how it relates to Frequency Shift Keying (FSK), and, specifically the FSK implementation of MSK where the modulation index, m, is set to a value of 0.5. All of these modulation formats are essentially equivalent, but are not identical. A coding step is necessary to make the FSK equivalent of MSK identical to the IEEE 802.15.4 implementation of O-QPSK with half-sine shaping. In this section, we examine the Zigbee modulation format as specified and show how to encode FSK to produce an identical carrier signal.

2.1 O-QPSK With Half-Sine Shaping

Figure 1 shows the minimum IQ symbol set {00, 01, 10, 11} with the requisite half-sine shaping over the symbol interval, the carrier phase state, $\Delta\phi_c$, at the end of the bit intervals (s0-s7), the change in carrier frequency, Δf_c, during the bit interval, and a phase transition map showing the allowed phase states and transitions for the ZigBee modulation.

The phase transition diagram indicates the allowed transition paths from each phase state to the next state for each bit interval and shows the value of the carrier frequency shift for each transition. The outer ring applies to transitions during even bit clock intervals (s0, s2, s4, s6), and the inner ring applies to transitions during odd bit clock intervals (s1, s3, s5, s7). For instance, if the current phase state is 1, (the phase state at the end of an odd clock bit interval) then during the following even clock bit interval, the phase could transition to either state 0 or state 2 along the outer ring, depending on the IQ bit pattern {01 or 11}, with the resulting change in carrier frequency. Similarly, if the current phase state is 0, (the phase state at the end of an even clock bit interval) the phase could transition along the inner ring depending on the IQ bit pattern {11' or 10'}, with the resulting change in carrier frequency. The prime notation (') indicates the transition is occurring during an odd bit clock cycle. The first chip transmitted by a ZigBee modulator is designated c0, so we define the first chip clock interval as an even bit clock interval, the second chip clock interval as an odd clock interval and so forth.

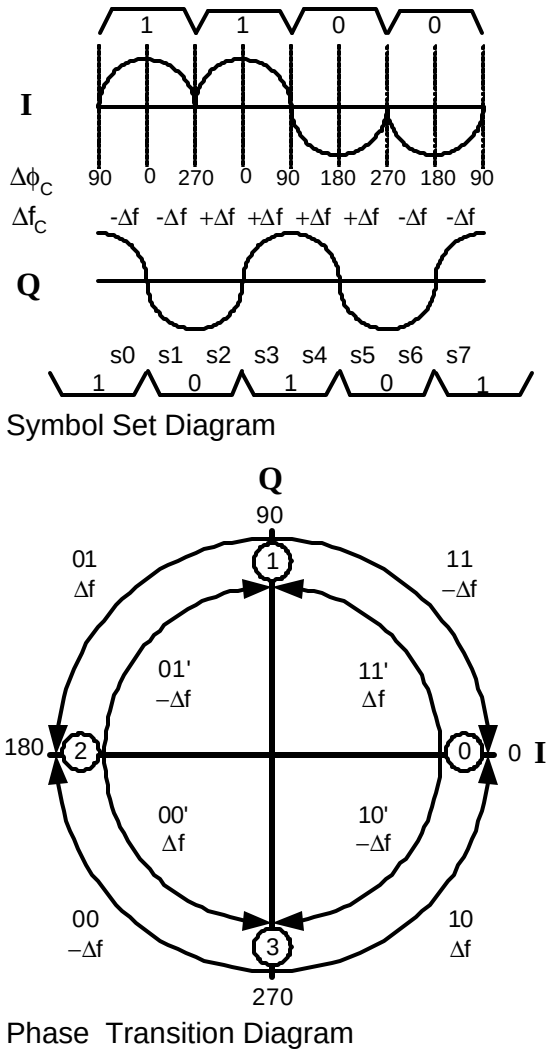

Figure 1: Symbol Set and Phase Transition Diagrams For ZigBee Modulation.

Figure 1 clarifies the relationship between the phase and frequency occurrences during each bit interval, and leads to a solution for direct frequency modulation of the carrier as an alternative to offset quadrature phase modulation.

2.2 O-QPSK (MSK) Implemented As FSK

MSK examined as frequency modulation consists of a sequence of positive or negative frequency shifts, each frequency shift having the value $\Delta f_c = 1/(4T_b)$, where T_b is the bit (or chip) interval. The resulting modulation index is m = 0.5. This can obviously be implemented as FSK with an FM modulator driven by a serial digital bit stream. To be completely compatible with the IEEE 802.15.4 specification, the FSK modulator has to produce frequency transitions that are identical to the frequency modulations produced by the canonic O-QPSK modulator as defined in the specification. To do this requires a coding step.

If we examine Figure 1 carefully, we see that the sign of Δf during a bit interval depends on the values of I and Q, and whether the interval is an even or an odd bit clock interval. For even bit clock intervals, the sign of Δf is determined by the value given by

$$k = \text{I } \textbf{xor } \text{Q} \quad (1)$$

and for odd bit clock intervals, the sign of Δf is determined by the value of

$$k = \textbf{not } (\text{I } \textbf{xor } \text{Q}) \quad (2)$$

If k = 0, then $\Delta f_c = -\Delta f$, and if k = 1, then $\Delta f_c = +\Delta f$. By encoding the ZigBee chip stream in this way, the frequency change for each bit will match the O-QPSK signaling specification exactly.

In designing a ZigBee transmitter, one approach would be to implement the chip table per the IEEE 802.15.4 specification and then run the serial data stream through the encoder described above prior to FM modulation. But, the chip codes are really coding phase, not frequency, so after FM demodulation, the data stream would not represent the chip codes directly. A simpler approach is to encode the chip table itself, and use the resulting FSK spreading code table to transmit and receive data.

3. RECEIVER ARCHITECTURES

While there are many approaches to receiver design for MSK style modulations, two which fit the basic themes for IEEE 802.15.4 systems, namely low-cost and low-power, are the well known Low IF and direct conversion (Zero IF) architectures. The Low IF approach uses a classic limiter discriminator to extract the baseband data stream from the modulated carrier. The Zero IF approach uses an IQ demodulator to extract the in-phase and quadrature components of the modulation, which are then digitized and processed to extract the data. Figure 2 shows simplified block diagrams for both of these approaches.

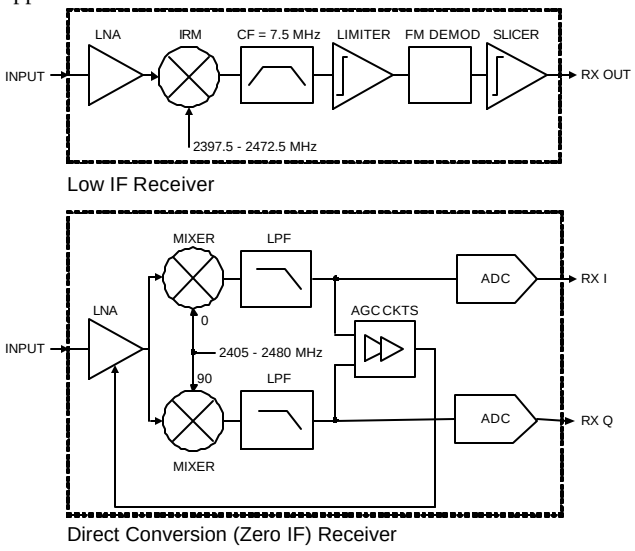

Figure 2. Receiver Architectures.

3.1 Low IF

Receiver system complexity and the associated circuit block complexity is often mitigated by implementing a Low IF architecture. The limiting IF avoids the need for automatic gain control (AGC) circuits and offers fast response to rapidly changing signal levels due to link fading conditions. The discriminator and slicing circuits are straightforward to design, are tolerant of frequency errors between the transmitter and receiver synthesizers, do not require carrier phase synchronization, and do not require high supply currents or chip area to implement.

The primary disadvantage of the Low IF architecture is a loss of about 3 dB in sensitivity [3] relative to a coherent demodulation scheme like the Zero IF receiver. Additionally, a channel filter is required to extract the desired carrier, reject nearby interfering signals, and set the receiver predetection noise bandwidth. Fortunately, the IEEE 802.15.4 2.4 GHz PHY channel assignment scheme sets channels at 5 MHz intervals, which, with a 2 MHz signal spectrum width and modest adjacent channel selectivity requirements, keeps the filter complexity requirements low. Finally, an image reject mixer (IRM) is required to reject signals at or near the receiver image frequency.

Frequency planning for the Low IF receiver for ZigBee requires some careful thought. The ZigBee chip rate for the 2.4 GHz PHY is 2 Mchips/s, leading to a modulated spectrum width of about 2 MHz. If the IF is too low, the channel filter percentage bandwidth is high, and the filter is difficult to implement. In addition, it becomes difficult to filter out the IF carrier ripple at the demodulator output, increasing the complexity of the baseband data filter. On the other hand, an active, on chip, IF filter that's too high in frequency requires large gain bandwidth product amplifiers to achieve adequate performance.

The Low IF receiver (Figure 2) uses a 7.5 MHz IF, which results in an achievable 27% filter bandwidth to center frequency ratio. In addition, the low side adjacent channel (f_c – 5 MHz) and alternate adjacent low side channel (f_c – 10 MHz) end up centered at 2.5 MHz at the output of the IRM, a full channel spacing away from the desired IF signal, considerably simplifying the IF filter rejection and the IRM image rejection requirements.

3.2 Zero IF

The Zero IF approach offers four notable architectural advantages compared to the Low IF approach for ZigBee at the expense of a considerable increase in complexity. First of all, unlike the Low IF approach which requires a 7.5 MHz frequency hop between transmit and receive, the Zero IF approach does not require the transceiver local oscillator (LO) to change frequency when transitioning between transmit and receive modes. Since the turn-around time between transmit and receive modes for ZigBee is specified as less than 12 symbol intervals, for the 2.4 GHz PHY the LO must make the 7.5 MHz frequency shift in less than 192 µs. Secondly, the Zero IF approach does not require an image reject mixer, since the homodyne architecture does not create an image frequency [5] [6]. Third, the Zero IF architecture utilizes a pair of simpler to implement low pass filters (as compared to an equivalent bandwidth IF bandpass filter) to set the I and Q output SNR [5] [6]. Finally, the Zero IF architecture supports optimum demodulation with matched filter and synchronous detection techniques.

Offsetting these advantages, Zero IF receivers require circuit blocks that Low IF receivers do not: AGC, post-mixer DC offset cancellation [5] [6], two analog-to-digital converters (ADCs) or one shared ADC to digitize the signal, and additional circuitry, usually located in a separate baseband chip, to implement synchronous demodulation and optimum baseband filtering. In general, this leads to higher receiver currents and greater power dissipation in return for superior performance. In addition, some care has to be taken to preserve amplitude balance and quadrature phase shift for the I and Q channels.

4. TRANSMITTER ARCHITECTURES

Two transmitter architectures which are appropriate for ZigBee implement classic modulator structures as illustrated in Figure 3. The IQ modulator implements the O-QPSK (or MSK) approach [7], while the 2-point ΔΣ Fractional-N modulator implements direct carrier frequency modulation via a frequency stabilized voltage controlled oscillator (VCO) [8]. Either modulation approach can be paired with either receiver approach previously described to create a complete transceiver.

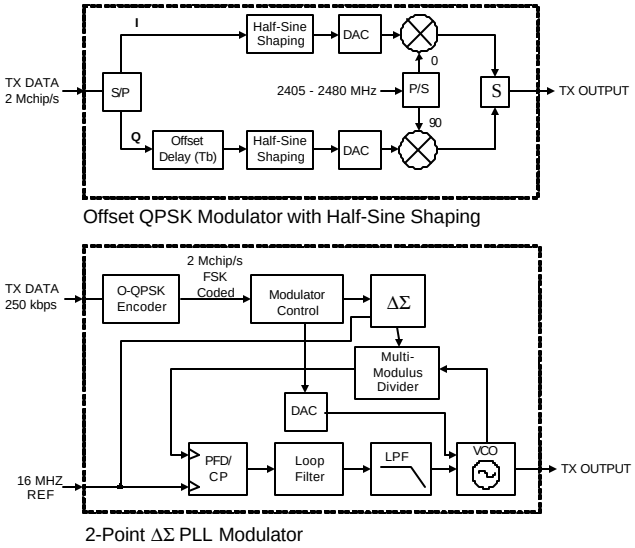

Figure 3. Transmitter Architectures.

4.1 IQ Modulator

The IQ modulator approach reverses the Zero IF receiver architecture, so baseband signals drive the IQ modulator inputs, and the modulator RF output is the sum of the quadrature I and Q channels. The I and Q signals, including half-sine shaping, are generated with digital logic and converted to analog signals using two digital-to-analog converters (DACs) with output data reconstruction filters (not shown) to drive the quadrature mixers. While simple in concept, the requirement for dual DAC's, dual up-converting mixers, and quadrature phase shifted LO signals leads to a relatively complex, high current design resulting in an implementation requiring a larger silicon area [8] [9].

4.2 2-Point DS Fractional-N Modulation

The 2−point approach combines the LO frequency synthesis circuits with modulation circuits to achieve compact MSK modulation with a minimum number of analog components. The implementation as shown in Figure 3 is based on a phase locked loop (PLL) using a multi-modulus divider driven by a multi-bit ΔΣ modulator to provide channel frequency selection and digital frequency modulation control, combined with a DAC to provide the analog modulation control. The 2-point modulator decouples the PLL bandwidth from the modulation bandwidth by using the fine resolution digital frequency control provided by the ΔΣ modulator to cancel the analog frequency modulation created by the DAC so there is no net change to the average divider frequency output. The result is that the average loop amplifier output remains constant over each modulation bit interval, and the loop response is not excited by the modulation waveform. The modulation bandwidth is only dependent on the frequency response of the analog frequency modulation path [8] [9].

2−point modulation adds complexity primarily in the digital circuit domain, which for most modern IC processes adds little to die size. The only additional analog components beyond those necessary for the PLL itself are one DAC and an additional low pass filter to reject the spurious signals associated with the ΔΣ modulator.

5. TRANSCEIVER TRADE-OFFS

Estimated areas for the receiver and transmitter implementations discussed in this paper paired in one possible set of transceiver configurations are listed in Table 1. The area estimates were arrived at by applying scaling factors to the block areas of similarly fabricated PAN systems implemented in a 0.18 µm CMOS process. An estimated cost of $ 0.10/mm^2 for production quantities is used in the cost calculations.

COST PARAMETER	*Low IF RX*	*Zero IF RX*
RF Front-End Area	.9 mm^2	1.75 mm^2
IF Chain Area	1.6 mm^2	2.5 mm^2
RX Chip Area	2.5 mm^2	4.25 mm^2
RX Die Cost	$ 0.25	$ 0.425
	2-point DS Fractional-N Modulator TX	***IQ Modulator TX***
Synthesizer	1.5 mm^2	2.75 mm^2
Transmitter	1.8 mm^2	1.8 mm^2
TX Chip Area	3.3 mm^2	4.55 mm^2
TX Die Cost	$ 0.33	$ 0.455
RX & TX Area	5.8 mm^2	8.8 mm^2
RX & TX Die Cost	$ 0.58	$ 0.88

Table 1. Production cost comparison between receiver, transmitter, and transceiver architectures.

6. CONCLUSION

The aspects of the 2.4 GHz radio PHY technical specification for 802.15.4 applicable to system design have been detailed with specific attention paid to the modulation/demodulation format and an alternative implementation. Possible receiver and transmitter architectures were proposed and examined, and two possible transceiver systems were briefly reviewed. Specifically, an 802.15.4 receiver could be implemented using either a Low IF or Zero IF architecture, the trade-off being low circuit complexity versus performance and die size. When considering transmitters for ZigBee, an obvious candidate architecture was shown to be the classic IQ modulator implementing O-QPSK modulation per the working group specification. This paper also proposed a less obvious but elegant modulation approach utilizing a 2-point ΔΣ Fractional-N synthesizer that would require less current, area, and lower circuit block complexity. The presented receiver and transmitter architectures can be paired in any combination. Given these options, the low-power, low-cost goal of a LR-PAN as defined by the 2.4 GHz ZigBee PHY is within reach.

7. REFERENCES

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