CX1540

CompXs

Very Low Power RF Transceiver for Wireless Radio Control Communication

▪ Outline

The CX1540 IC enables short distance wireless control in the 2.4 GHz band (IEEE 802.15.4), and includes the RF, IF, MODEM, PHY, MAC and MCU data interface functions.
The low data transmission rate and low power consumption result in long battery life.
The IC includes a fully functional 802.15.4 MAC layer, and can be used with a ZigBee™ network layer which facilitates the building of Zig Bee™ Networks.
The CX1540 is suitable for sensors, tags, toys, remote controls and domestic appliances.

▪ Special Features

- Fully compliant to IEEE 802.15.4 – 2003
- 16 channel 2.4 GHz band wireless
- Maximum data transmission speed is 250kbps
- CSMA-CA channel access
- IEEE 802.15.4 2.4 GHz PHY
- IEEE 802.15.4 MAC
- O-QPSK modulation function
- Synchronous communication interface (SCI)
- Simplified ZigBee™ Network due to Zig Bee™ NWK layer software
- Power supply voltage:

  (1) Standard power supply voltage 3.0V (eg. two Manganese/Alkali batteries, Lithium battery)
  I/O 3.0V power supply (VDD: Typ 3.0V Min 2.7V Max 3.3V)
  CORE, RF 2.5V power supply (VDD: Typ 2.5V Min 2.25V Max 2.75V)

  (2) Standard power supply voltage 2.4V (eg. two nickel hydrogen batteries)
  I/O 2.4V power supply (VDD: Typ 2.4V Min 2.0V Max 2.7V)
  CORE, RF 2.4V power supply (Vdd: Typ 2.4V Min 2.0V Max 2.7V)

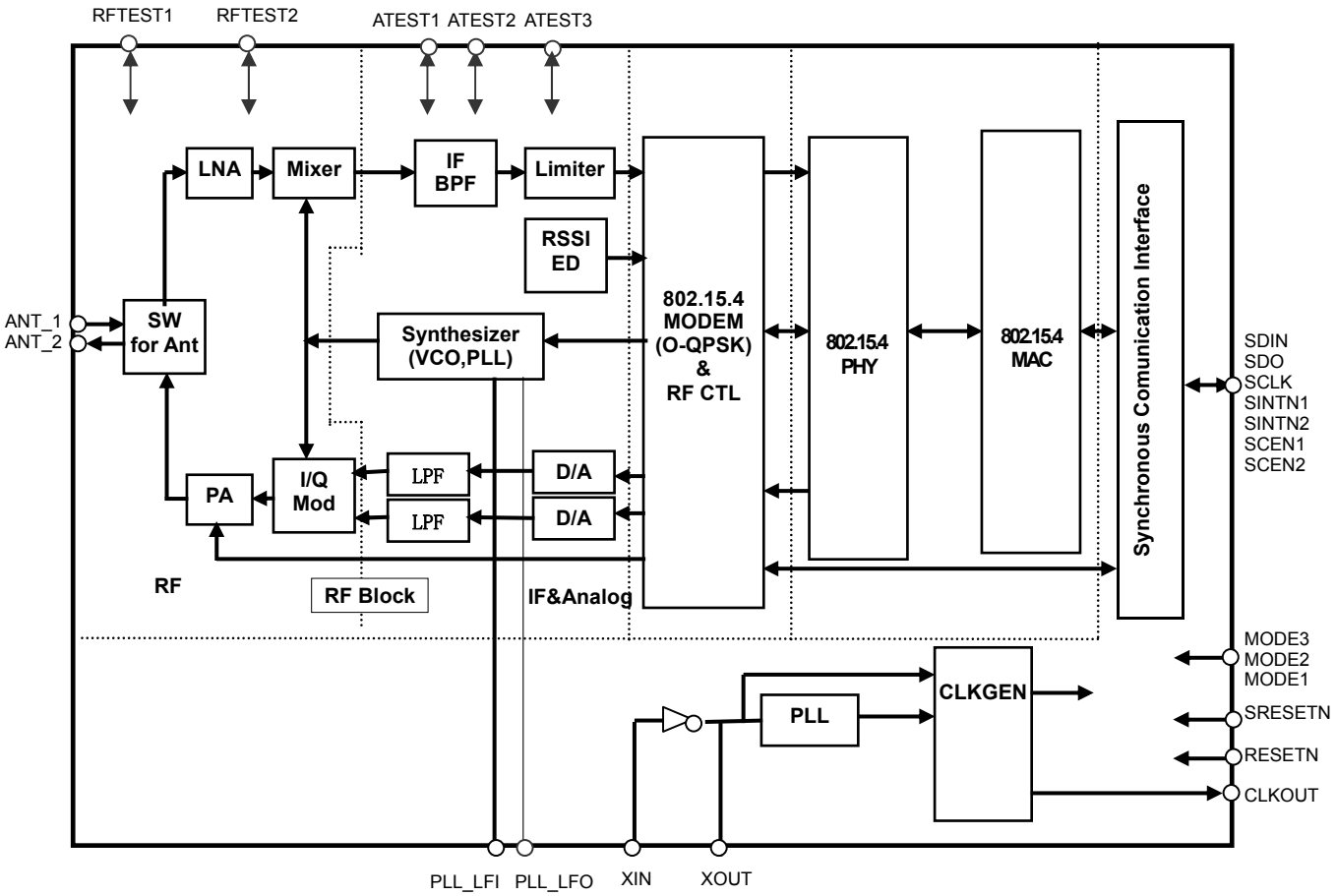
- Current

Standby	1 µA	(Typ.)
Transmit	56 mA	(Typ.)
Receive	57 mA	(Typ.)

- Package

  48 pins VQFN 48 0.5mm pitch

▪ Block Diagram



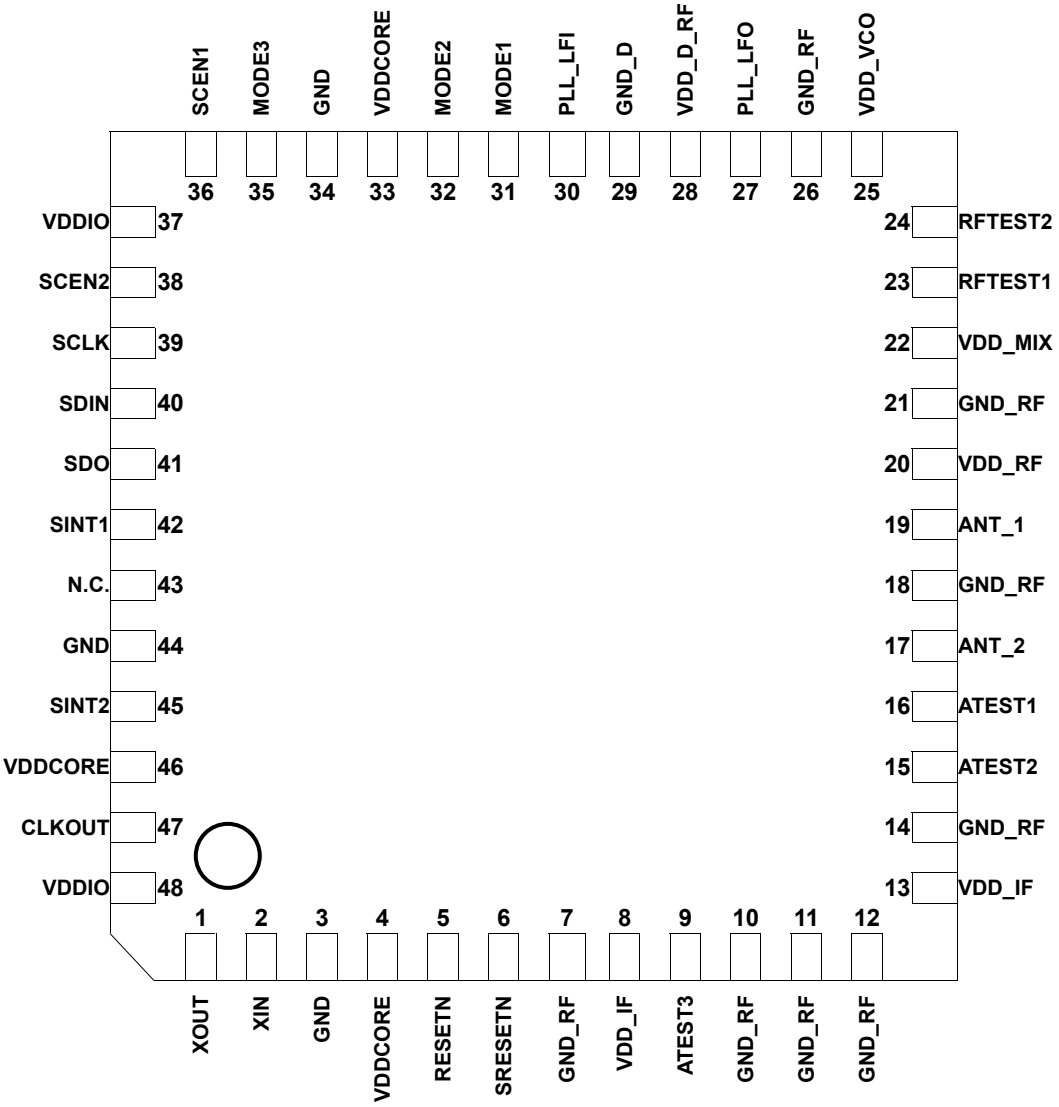
Functional Blocks

The CX1540 consists of the following key blocks:

- RF block
  - consists of RF, IF and Analogue circuits
  - wireless control messages for transmitting and receiving at 2.4 GHz
- MODEM block and RF CTL block
  - O-QPSK modulation circuit
  - includes RF block control circuit
- PHY block
  - PHY logic conforming to IEEE 802.15.4
- MAC block
  - MAC logic conforming to IEEE 802.15.4
- SPI Interface block
  - synchronous communication with any MCU

- **Pin Connections**

48 pins VQFN



TOP VIEW

▪ Pin Descriptions

RF Pins

Pin No.	Pin Name	Reset	I/O	Active Level	Pin Functions
19	ANT_1	I	I_{RF}/O_{RF}	-	RF antenna pin
17	ANT_2	I	I_{RF}/O_{RF}	-	RF antenna pin
27	PLL_LFO	O	O_A	-	External loop filter output pin (VCO side) for external connection refer to applied logic
30	PLL_LFI	I	I_A	-	External loop filter input pin (PLL side) for external connection refer to applied logic

I/ODefinitions

I_{RF} : RF input pin
I_A : Analogue input pin
I : Normal input pin
I_S : Schmidt trigger input pin
I_U : Input pin with pull up function
I_{SU} : Input pin with Schmidt trigger and pull up
I_{OS} : Oscillator circuit input pin
O_{RF} : RF control output pin
O_A : Analogue output pin
O : Normal output pin
O_{OS} : Oscillator circuit output pin

Synchronous Communication Interface Pins

Pin No.	Pin Name	Reset	I/O	Active Level	Pin Functions
40	SDIN	H	I	-	Synchronous communication interface data input pin
41	SDO	L	O	-	Synchronous communication interface data output pin
39	SCLK	I	I	P or N	Synchronous communication interface clock input pin
42	SINT1	H	IuO	L	Synchronous communication interface interrupt output pin (for the 802.15.4 MAC function).
36	SCEN1	H	Iu	-	Synchronous communication interface chip enable pin (for the 802.15.4 MAC function)
45	SINT2	H	IuO	L	Synchronous communication interface interrupt output pin (for the IC Control Function)
38	SCEN2	H	Iu	-	Synchronous communication interface chip enable pin (for the IC Control Function)

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Other Pins

Pin No.	Pin Name	Reset	I/O	Active Level	Pin Function
5	RESETN	I	Is	L	Hardware reset pin
6	SRESETN	I	Isu	L	Software reset (unless in sleep mode) Reset Pin from MCU Sleep mode cancellation pin (when in sleep mode) Only effective when RESETN=1 (unasserted)
2	XIN	H	I - osc	-	10 MHz Crystal Oscillator connection pin 1 External clock input pin
1	XOUT	H	O - osc	-	10 MHz Crystal Oscillator connection pin 2 Open if XIN functions as external clock input pin
47	CLKOUT	L	O	-	System clock output pin able to supply to MCU
31	MODE1	I	IO	-	Pin to determine mode 1
32	MODE2	I	I	-	Pin to determine mode 2
35	MODE3	I	I	-	Pin to determine mode 3

Other Pins

Pin No.	Pin Name	Reset	I/O	Active Level	Pin Function
23	RFTEST1	Hi-Z	I_{RF}/O_{RF}	-	RFCircuit Test Pin
24	RFTEST2	Hi-Z	I_{RF}/O_{RF}	-	
16	ATEST1	Hi-Z	I_A/O_A	-	IF and Analogue circuit test pin
15	ATEST2	Hi-Z	I_A/O_A	-	
9	ATEST3	Hi-Z	I_A/O_A	-	

(Note) The pads for RFTEST1, 2, ATEST 1, 2 and 3 are only used for test purposes

Power Supply Pins

Pin No.	Pin Name	Reset	I/O	Active Level	Pin Function
20	VDD_RF	-	-	-	For PA, LNA, SW, IQMOD Power supply pin
25	VDD_VCO	-	-	-	Power supply pin for Synthesizer VCO
22	VDD_MIX	-	-	-	Power supply pin for Mixer, Synthesizer Local Gen
8	VDD_IF	-	-	-	Power supply pin
13					BPF, Limiter, RSSI, DAC
28	VDD_D_RF	-	-	-	Power supply pin for Synthesizer Charge Pump
37	VDD_IO	-	-	-	Power supply pin
48					For digital IO
4	VDD_CORE	-	-	-	Power supply pin
33					For Digital CORE
46					
7	GND_RF	-	-	-	RF and IF ground pin
10					
11					
12					
14					
18					
21					
26					
29	GND_D	-	-	-	Ground pin for Synthesizer Charge Pump
3	GND	-	-	-	Digital ground pin
34					Common ground for IO and CORE
44					

Handling of Unused Pins

This section indicates how unused pins should be handled. Unused pins do not affect the functioning of the CX1540.

Pin Name	Recommendation
XOUT	Open (provided XIN is external clock input)
MODE1	In accordance with mode (see below)
MODE2	In accordance with mode (see below)
MODE3	In accordance with mode (see below)
CLKOUT	Open
SRESETN	VDD
RFTEST1	Open
RFTEST2	Open
ATEST1	Open
ATEST2	Open
ATEST3	Open

Note:

If high impedance input pins are left open, there may be issues with high current states. It is therefore recommended that unused input and output pins be driven with pull-up or pull-down resistors.

▪ Absolute Maximum Values

Parameter	Symbol	Conditions	Min/Max values	Unit
Power Supply Voltage (I/O) (*1)	V_{DDIO}	Ta=+25C VSS=0V	-0.3 to +4.6	V
Power Supply Voltage (CORE) (*2)	V_{DDCORE}		-0.3 to +3.6	V
Power Supply Voltage (RF) (*3)	V_{DDRF}		-0.3 to +3.6	V
Power Supply Voltage (Analogue) (*4)	V_{DDANA}		-0.3 to +3.6	V
Digital Input Voltage	V_{DIN}		-0.3 to V_{DDIO}+0.3	V
RF Input Voltage	V_{RFIN}		-0.3 to V_{DDRFIO}+0.3	V
Analogue Input Voltage	V_{AIN}		-0.3 to V_{DDIO}+0.3	V
Digital Output Voltage	V_{DO}		-0.3 to V_{DDIO}+0.3	V
RF Output Voltage	V_{RFO}		-0.3 to V_{DDIO}+0.3	V
Analogue Output Voltage	V_{AO}		-0.3 to V_{DDIO}+0.3	V
Digital Input Current	I_{DI}		-10 to +10	mA
RF Input Current	I_{RF}		-2 to +2	mA
Analogue Input Current	I_{AI}		-2 to +2	mA
Digital Output Current	I_{DO}		-10 to +10	mA
RF Output Current	I_{RFO}		-2 to +2	mA
Analogue Output Current	I_{AO}		-2 to +2	mA
Storage Temperature	T_{stg}	-	-55 to +150	℃

(*1) VDD_IO Pin

(*2) VDD_CORE Pin

(*3) VDD_RF Pin, VDD_MIX Pin

(*4) VDD_IF Pin, VDD_VCO Pin, VDD_D_RF Pin

▪ Recommended Operating Conditions

(1) Power Supply Voltage (standard power supply voltage 3.0v)

Parameter	Symbol	Reference	Min	Typical	Max	Unit
Power Supply Voltage (I/O)	V_{DDIO}	VDD_IO Pin (*6)	2.7	3.0	3.3	V
Power Supply Voltage (CORE)	V_{DDCORE}	VDD_CORE Pin (*6)	2.25	2.5	2.75	V
Power Supply Voltage (RF)	V_{DDRF}	VDD_RF Pin, VDD_MIX Pin (*7)	2.25	2.5	2.75	V
Power Supply Voltage (ANALOGUE)	V_{DDANA}	VDD_IF Pin, VDD_VCO Pin, VDD_D_RF Pin (*7)	2.25	2.5	2.75	V
Operation Temperature	T_a	-	-25	+25	+70	℃
Digital Input Rise Time	t_{IR1}	Digital Input Pin (*8)	-	-	20	ns
Digital Input Fall Time	t_{IF1}	Digital Input Pin (*8)	-	-	20	ns
Digital Output Load	C_{DL}	All Digital Output Pin	-	-	20	pF
Master Clock 10 MHz	F_{MCK1}	XIN Pin, XOUT Pin	-40ppm	10	+40ppm	MHz
Master Clock External Input Frequency	F_{MCK2}	External Input from XOUT Pin	-40ppm	10	+40ppm	MHz
Master Clock Duty Ratio	D_{MCK}	External Input from XOUT Pin	45	50	55	%
Clock Output Frequency	F_{CLKOUT}	CLKOUT Pin	-	-	16	MHz
Clock Output Duty Ratio	D_{CLKOUT}	CLKOUT Pin	45	50	55	%
SCI Clock Input Frequency	F_{SCLK}	SCLK Pin	1	-	2	MHz
SCI Clock Input Duty Ratio	D_{SCLK}	SCLK Pin	45	50	55	%
RF Channel Freq (*9)	F_{RF}	ANT_1 Pin,ANT_2 Pin	2405	-	2480	MHz
RF Maximum Input Level	P_{RFIN}	±40ppm、PER<1%	-20	-	0	dBm

(*6) $V_{DDIO} > V_{DDCORE}$

(*7) $V_{DDCORE} = V_{DDRF} = V_{DDANA}$

(*8) Pin for which I/O type is I, Is, Iu and Isu

(*9) IEEE802.15.4 regulated under IEEE 802.15.4 F_{RF}=2405+5x(k-11) MHz k=11,12,…,26

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Parameter	Symbol	Reference	Min	Typical	Max	Unit
Power Supply Voltage (I/O)	V_{DDIO}	VDD_IO Pin (*10)	2.0	2.4	2.7	V
Power Supply Voltage (CORE)	V_{DDCORE}	VDD_CORE Pin (*10)	2.0	2.4	2.7	V
Power Supply Voltage (RF)	V_{DDRF}	VDD_RF Pin, VDD_MIX Pin (*10)	2.0	2.4	2.7	V
Power Supply Voltage (ANALOGUE)	V_{DDANA}	VDD_IF Pin, VDD_VCO Pin, VDD_D_RF Pin (*10)	2.0	2.4	2.7	V
Operation Temperature	T_a	-	-25	+25	+70	℃
Digital Input Rise Time	t_{IR1}	Digital Input Pin (*8)	-	-	20	ns
Digital Input Fall Time	t_{IF1}	Digital Input Pin (*8)	-	-	20	ns
Digital Output Load	C_{DL}	All Digital Output Pin	-	-	20	pF
Master Clock 10 MHz Crystal Vibrator Frequency	F_{MCK1}	XIN Pin, XOUT Pin	-40ppm	10	+40ppm	MHz
Master Clock External Input Frequency	F_{MCK2}	External Input from XOUT Pin	-40ppm	10	+40ppm	MHz
Master Clock Duty Ratio	D_{MCK}	External Input from XOUT Pin	45	50	55	%
Clock Output Frequency	F_{CLKOUT}	CLKOUT Pin	-	-	16	MHz
Clock Output Duty Ratio	D_{CLKOUT}	CLKOUT Pin	45	50	55	%
SCI Clock Input Frequency	F_{SCLK}	SCLK Pin	1	-	2	MHz
SCI Clock Input Frequency	F_{SCLK}	SCLK Pin	1	-	2	MHz
SCI Clock Duty Ratio	D_{SCLK}	SCLK Pin	45	50	55	%
RF Channel Freq(*9)	F_{RF}	ANT_1 Pin, ANT_2 Pin	2405	-	2480	MHz
RF Maximum Level	P_{RFIN}	±40ppm, PER<1%	-20	-	0	dBm

(*8) Pin which has I/O type I, Is, Iu or Isu

(*9) IEEE802.15.4regulated under IEEE 802.15.4 $F_{RF}=2405+5x(k-11)$ MHz for k=11,12,…,26

(*10) $V_{DDIO}=V_{DDCORE}=V_{DDRF}=V_{DDANA}$

▪ Electrical Characteristics

- DC Characteristics

(1)Power Supply Voltage 1 (standard power supply voltage 3.0v)
1.V_{DDIO} =2.7V-3.3V, V_{DDCORE}=V_{DDRF}=V_{DDANA} =2.25V-2.75V Ta=-25 to 70ºC

Parameter	Symbol		Min	Typical	Max	Unit
Power Supply Current	I_{DDS}	Stop Mode	-	1		μA
	I_{DD1}	Sleep mode	-	1		μA
	I_{DD2}	Suspend mode	-	1		mA
	I_{DD3}	Idle mode	-	4		mA
	I_{DD4}	Receive Mode	-	57		mA
	I_{DD5}	Transmit Mode	-	56		mA

(*11) Average V_{DDIO} =3.0V V_{DDCORE}=V_{DDRF}=V_{DDANA} =2.5V power supply voltage 1
(*12) Could be higher for some MCU operating conditions and when SCI interface clock SCLK is over 2 MHz.

(Power Supply Voltage 1 : V_{DDIO} =2.7V to 3.3V, V_{DDCORE}=V_{DDRF}=V_{DDANA} =2.25V to 2.75V Ta=-25 to 70ºC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH1}		2.2	-	VDDIO	V
	V_{IH2}	External clock input	V_{DDIO} x 0.9	-	V_{DDIO}	V
Low Level Input Voltage	V_{IL1}		0	-	0.6	V
	V_{IL2}	External clock input	0	-	V_{DDIO} x 0.1	V
Schmidt Trigger	V_{T+}		-	1.5	2.1	V
Schmidt Trigger	V_{T-}		0.7	1.0	-	V
Input leakage current	I_{IH1}	V_{IH}= V_{DDIO}	-2	-	2	μA
	I_{IL1}	V_{IL}=0V	-2	-	2	μA
	I_{IL2}	V_{IL}=0V	-200	-40	-10	μA
Tristate leakage	I_{OZH}	V_{OH}= V_{DDIO}	-2	-	2	μA
Output leakage current	I_{OZL}	V_{OL}=0V	-200	-40	-10	μA
High Level Output Voltage	V_{OH1}	I_{OH}=-100μA	V_{DDIO} -0.2	-	V_{DDIO}	V
	V_{OH2}	I_{OH}=-4mA	2.2	-	V_{DDIO}	V
	V_{OH3}	I_{OH}=-150μA	V_{DDIO} -0.2	-	V_{DDIO}	V
Low Level Output Voltage	V_{OL1}	I_{OL}=100μA	0	-	0.2	V
	V_{OL2}	I_{OL}=4mA	0	-	0.4	V
	V_{OL3}	I_{OL}=130μA	0	-	0.2	V
Input Capacitance	C_{IN}	Input Pin	-	6	-	pF
	COUT	Output Pin	-	9	-	pF
	CRFIO	RF Input/Output	-	TBD	-	pF
	CA	Analogue Input Pin	-	TBD	-	pF

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(2) Power supply voltage 2 (standard power supply voltage 2.4v)

(V_{DDIO} =V_{DDCORE}=V_{DDRF}=V_{DDANA} =2.0V to 2.7V Ta= -25 to +70ºC)

Parameter	Symbol		Min	Typ	Max	Unit
Power Supply Current	I_{DDS}	Stop Mode	-	TBD	-	µA
	I_{DD1}	Suspend Mode	-	TBD	-	µA
	I_{DD2}	Sleep Mode	-	TBD	-	mA
	I_{DD4}	Receive Mode	-	TBD	-	mA
	I_{DD5}	Transmit Mode	-	TBD	-	mA

(*23) Average V_{DDIO} =V_{DDCORE}=V_{DDRF}=V_{DDANA} =2.4V Power Supply Voltage 2

(*12) Could be higher for some MCU operating Modes and when SCI interface Clock SCLK is over 2 MHz.

(Power Supply Voltage 2 : V_{DDIO} =V_{DDCORE}=V_{DDRF}=V_{DDANA} =2.0V to 2.7V Ta=-25 to +70ºC)

Parameter	Symbol	Mode	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH1}		V_{DDIO} x 0.7	-	V_{DDIO}	V
	V_{IH2}	External clock input	V_{DDIO} x 0.9	-	V_{DDIO}	V
Low Level Input Voltage	V_{IL1}		0	-	V_{DDIO} x 0.3	V
	V_{IL2}	External clock input	0	-	V_{DDIO} x 0.1	V
Schmidt Trigger	V_{T+}		-	1.2	1.8	V
Schmidt Trigger	V_{T-}		0.4	0.8	-	V
Input Leakage Current	I_{IH1}	VIH= V_{DDIO}	-2	-	2	µA
	I_{IL1}	VIL=0V	-2	-	2	µA
	I_{IL2}	VIL=0V	-100	-25	-5	µA
Tristate Output	I_{OZH}	VOH= V_{DDIO}	-2	-	2	µA
Output Leakage Current	I_{OZL}	VOL=0V	-100	-25	-5	µA
High Level Output Voltage	V_{OH1}	IOH=-100µA	V_{DDIO} -0.2	-	V_{DDIO}	V
	V_{OH2}	IOH=-4mA	V_{DDIO} x 0.8	-	V_{DDIO}	V
	V_{OH3}	IOH=-150µA	V_{DDIO} x 0.8	-	V_{DDIO}	V
Low Level Output Voltage	V_{OL1}	IOL=100µA	0	-	0.2	V
	V_{OL2}	IOL=4mA	0	-	V_{DDIO} x 0.2	V
	V_{OL3}	IOL=130µA	0	-	V_{DDIO} x 0.2	V
Input Capacitance	C_{IN}	Input Pin	-	6	-	pF
	C_{OUT}	Output Pin	-	9	-	pF
	C_{RFIO}	RF Input/Output Pin	-	TBD	-	pF
	C_A	Analogue Input Pin	-	TBD	-	pF

- **RF Characteristics**

(1) Power Supply Voltage 1 (standard power supply voltage 3.0v)

(V_{DDIO} =2.7V to 3.3V, V_{DDCORE}=V_{DDRF}=V_{DDANA} =2.25V to 2.75V Ta =-25 to +70ºC)

Parameter	Symbol	Mode	Min	Typ	Max	Unit
Transmitter						
Transmit Power			-3	-	3	dBm
Center Frequency Tolerance		Clock Tolerance < 40ppm	-40	-	40	ppm
Power Spectral Density Absolute		|f-fc| > 3.5MHz	-	-	-30	dBm
Power Spectral Density Relative			-	-	-20	dB
EVM			-	-	35	%
RF Output Impedance	Z_{OUT}	ANT_1, ANT_2 Internal TX/RX SW used	-	50	-	ohm
Receiver						
Receiver Sensitivity	R_{IN}	±40ppm, PER < 1%	-	-90	-85	dBm
Receiver Jamming Resistance Adjacent Channel		PER < 1% Requirement is -82dBm	0	-	-	dB
Receiver Jamming Resistance Alternate Channel		PER < 1% Requirement is -82dBm	30	-	-	dB
Maximum Input Level		±40ppm、PER < 1%	-20	-	-	dBm
Energy Detection Accuracy			-	-	6	dB
Energy Detection Range			-80	-	-40	dBm
Spurious Emmission		30MHz to 1GHz	-	-	-57	dBm
		1GHz to 12.75GHz	-	-	-47	dBm
Transceiver						
Out of Band Spurious Emission		30MHz to 1GHz	-	-	-36	dBm
		1GHz to 12.75GHz	-	-	-30	dBm
		1.8GHz to 1.9GHz	-	-	-47	dBm
		5.15GHz to 5.3GHz	-	-	-47	dBm

Notes

Frequency Range F=2450+5x(k-11) MHz for k = 11 to 26

TOP BPF is not included

2.5MHz Low IF

● Synchronous Communication Interface (SPI) Characteristics

(Power Supply Voltage 1,2 Ta= -25 to +70ºC)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
SCLK Clock Frequency	F_{SCLK1}	except suspend	Load Capacitance C_L= 50pF	0.032	2	8	MHz
	F_{SCLK2}	at suspend		0.032	0.5	1	MHz
SCEN* Input Setup Time	T_{CESU}			15	-	-	ns
SCEN* Input Hold Time	T_{CEH}			15	-	-	ns
SCLK Width Pulse High	T_{WCKH}			50	-	-	ns
SCLK Width Pulse Low	T_{WCKL}			50	-	-	ns
SDIN Input Setup Time	T_{DISU}			5	-	-	ns
SDIN Input Hold Time	T_{DIH}			15	-	-	ns
SDO Output Enable Time	T_{CEEN0}	Positive Clock		0	-	40	ns
	T_{CEEN1}	Negative Clock		0	-	20	ns
SCEN Output Disable	T_{CEDIS}			-	-	25	ns
SCLK Output Delay Time	T_{CKOD}			-	-	40	ns
SDO Output Hold Time	T_{DOH}			5	-	-	ns

Notes:

All timing measurements are taken at 20% of VDDIO and 80% of VDDIO

● Reset Characteristics

Power Supply Voltage 1,2 Ta= -25 to +70ºC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RESETN Delay Time (when power is switched on)	T_{RDL}	All Supply Pins after power on	5	-	-	ms
SRESETN Pulse Period	T_{RPLS}	RESETN=1	200	-	-	ns
SRESETN Delay Time (in operation)	T_{RDOP}		5	-	-	ms
RESETN-SRESETN Setup Time (in operation)	T_{RDOP}		10	-	-	ns

Notes:

All timing measurements are taken at 20% of VDDIO and 80% of VDDIO

- **Clock Output Characteristics**

(Power supply voltage 1,2 Ta= -25 to +70ºC)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CLKOUT Clock settling time	TRCO	Reset unasserted.	-	-	10	ms

Notes:

All timing measurements are taken at 20% of VDDIO and 80% of VDDIO.

- **Power On and Power Down Characteristics**

(Power supply voltage 1,2 Ta= -25 to +70ºC)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power on time.	TPWON	Power applied to all VDD pins.	-	1	5	ms

Notes:

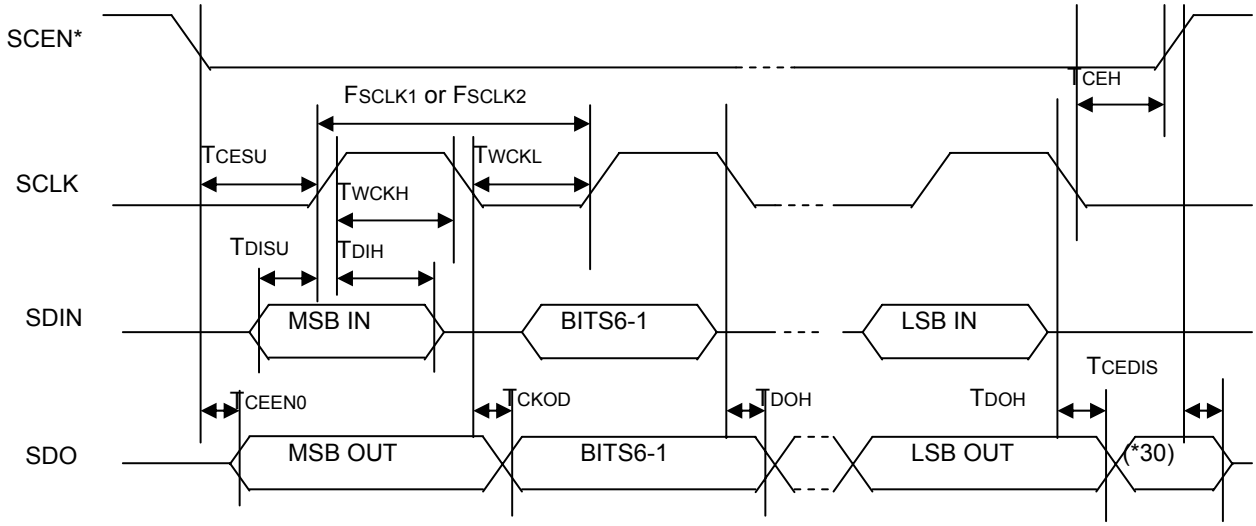
The order in which power pins receive power does not matter. However, after power has been applied, the RESETN pin timing requirements must be met.

The timing is determined for each power supply pin by 20% and 80% of minimum value of power supply voltage.

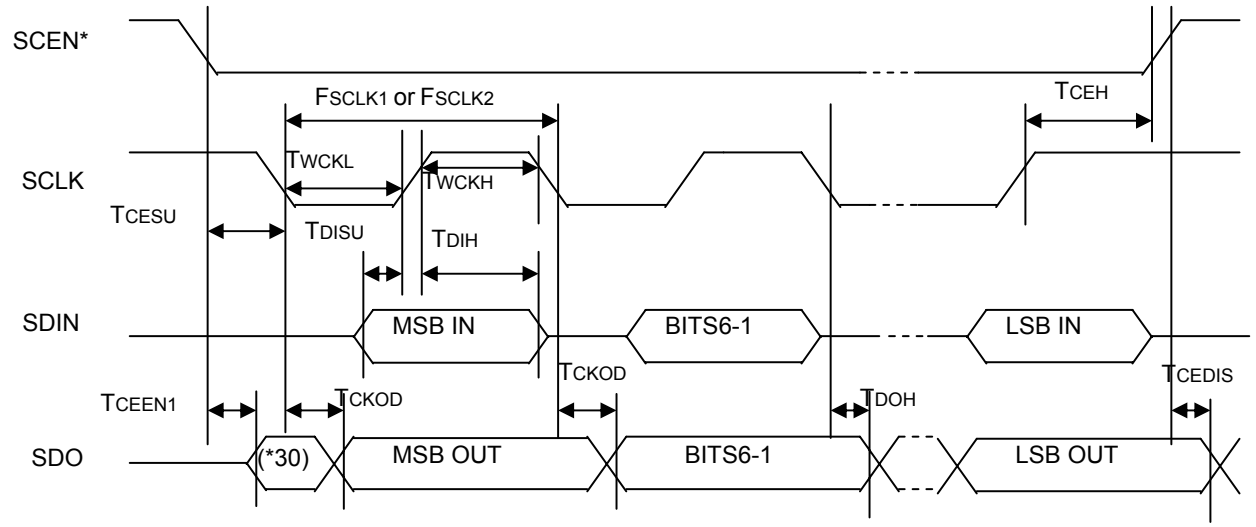
▪ Timing Charts

- **Synchronous Communication Interface (SCI) characteristics**.

For SCLK positive clock



For SCLK negative clock



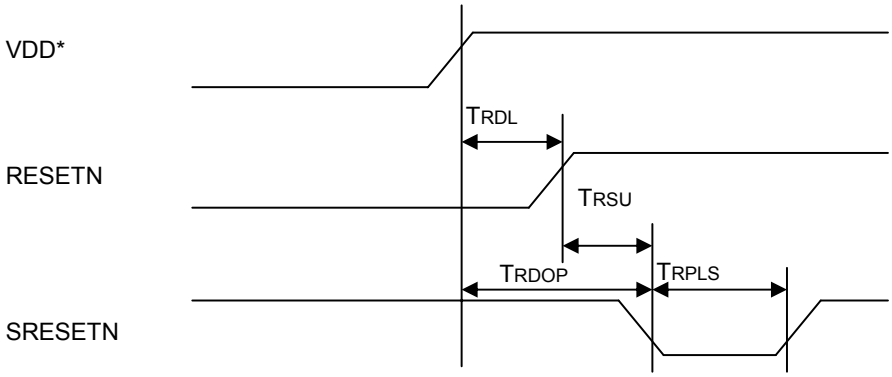
Notes

The timing of the SINT signal does not depend on other related synchronous clock serial interface pins.

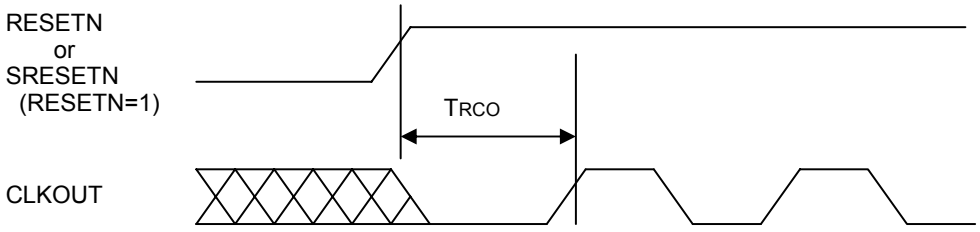
The diagram above is for MSB input and output. This holds for LSB as well, depending on the state of the MODE pin.

(*30) If the Mode pins have selected LSB first, then the data bits will be transmitted in reverse of the order shown here

- **Reset Timing**



- **Clock output interface**



Reset function

The CX1540 has 3 reset functions.

- Reset from RESETN pin.
  - Following the applying of power to the VDD pins, the internal circuits can be reset by asserting RESETN. Please refer to the application circuits for the recommended external circuit for RESETN. This reset may be asserted at any time by driving the RESETN pin to logic '0'. After reset, and once the oscillator and PLL circuits have become stable, the IC will enter normal operating mode.

- Reset from the SRESETN pin.
  - Soft reset can be carried out from the host controller by driving input SRESETN using a controller GPIO pin. This is only enabled when RESETN pin is unasserted. In sleep mode, it becomes the sleep cancellation pin. The internal circuits can be reset by asserting SRESETN pin. After reset, and once the oscillator and PLL circuits have become stable, the IC will enter normal operating mode

- Soft reset by register access
  - Reset of the internal circuits is possible with RST-CTLI command and by setting the SRSTN-INSIDE register. This is not enabled in sleep mode. After reset, and once the oscillator and PLL circuits have become stable, the IC will enter normal operating mode

Power management function

The CX1540 has four other modes in addition to its normal communication mode (receive, transmit).

- Total stop mode
  - Reset pin asserted.
  - Internal circuit set to initial state

- Sleep mode
  (1) All circuits are deactivated. However, the register contents are maintained. In sleep mode, the IC can be returned to normal mode without being reset by asserting SRESETN. This input may only be used in sleep mode.

- Suspend mode
  (2) Only the oscillator circuit is active and provides clock to the SCI logic. the register contents are maintained during suspend. The IC may be returned to normal mode through the SCI interface.

- Idle mode
  (3) Only the RF circuits are disabled. The IC may be returned to normal mode through the SCI interface.

▪ Mode setting

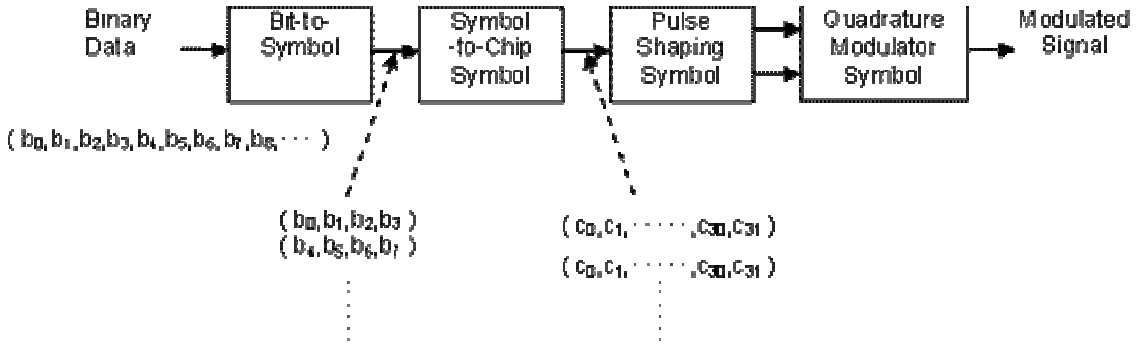
The CX1540 has three active modes as shown below; a normal mode, an option function mode and a test mode.

Other pins

Mode No.	Pin setting			Operation category	Function explanation
	MODE1	MODE2	MODE3		
1	L	L	L	data transmission	SCI： LSB data input and output CLKOUT pin：Disabled
2	H	L	L	data transmission	SCI： MSB data input and output CLKOUT pin：Disabled
3	L	H	L	data transmission	SCI： LSB data input and output CLKOUT pin：Enabled
4	H	H	L	data transmission	SCI： MSB data input and output CLKOUT pin：Enabled
5	-	-	H	Test	Test mode only

IEEE802.15.4 modulation

(3) Modulation circuit block diagram



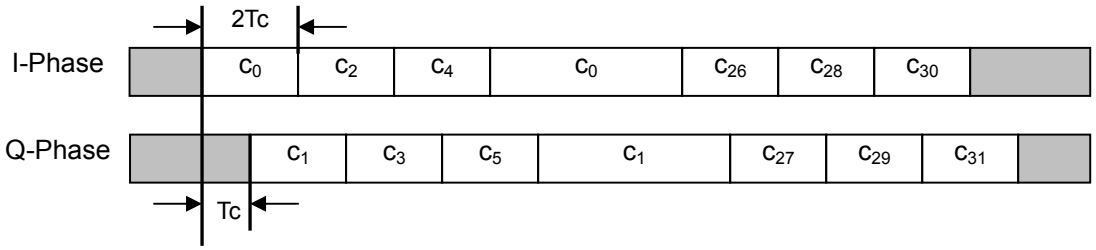
- Any binary data that is to be sent to the modem will be mapped to one of 16 different symbols, ”0” to ”F”, every 4 bits.
- As shown in the table below, each symbol will be mapped to a 32 chip data set.

Symbol-to-Chip Mapping

Data Symbol (Hex)	Data Symbol (Binary) $b_0\ b_1\ b_2\ b_3$	Chip Values ($c_0, c_1, c_2, \cdots\cdots, c_{29}, c_{30}, c_{31}$) (I , Q , I , ····· , Q , I , Q)
0	0 0 0 0	1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1	1 0 0 0	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
2	0 1 0 0	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
3	1 1 0 0	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
4	0 0 1 0	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
5	1 0 1 0	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
6	0 1 1 0	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
7	1 1 1 0	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
8	0 0 0 1	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1
9	1 0 0 1	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1
A	0 1 0 1	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1
B	1 1 0 1	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
C	0 0 1 1	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
D	1 0 1 1	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
E	0 1 1 1	1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
F	1 1 1 1	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0

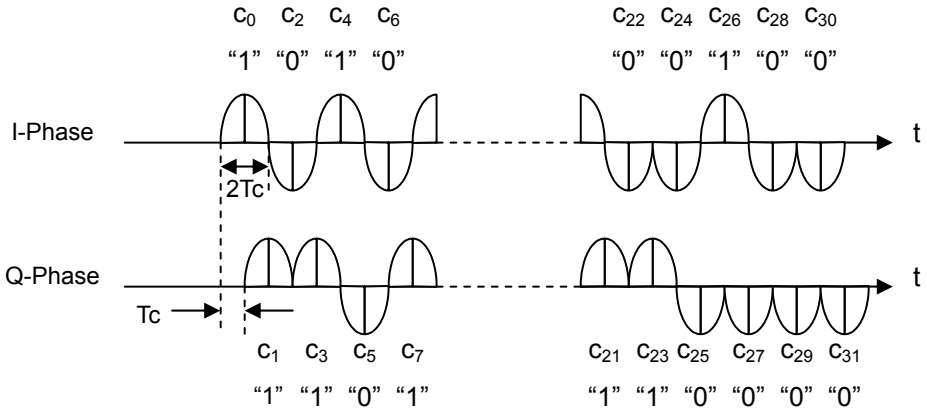
- Chip order

32 chip data is divided into I-phase (even numbers) and Q-phase (odd numbers), which are offset by half a chip number, according to OQPSK modulation requirements.



- Pulse shape

I, Q data wave form is shown in the diagram below (only for first half of direct modulation)

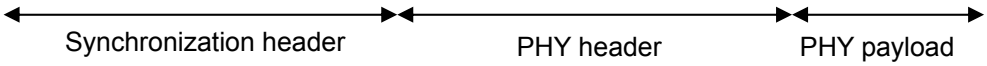


$$p(t) = \begin{cases} \sin(\pi t / 2Tc) & \cdots\cdots\ 0 \le t \le 2Tc \\ 0 & \cdots\cdots\ \text{otherwise} \end{cases}$$

▪ Packet format

General packets which the CX1540 sends are built up as shown below.
For a detailed description of the frame format, please refer to IEEE 802 15.4-2003.

Preamble	**Start of frame Delimiter**	**Frame length (7bit)**	**Reserved (1bit)**	**PSDU**
4 Bytes	1 Byte	1 Byte		max 127 Bytes



(1) Preamble : 0000 0000 0000 0000 0000 0000 0000 0000 (symbols ”0 0 0 0 0 0 0 0”)

(2) Start of frame delimiter

Bit:0	Bit:1	Bit:2	Bit:3	Bit:4	Bit:5	Bit:6	Bit:7
1	1	1	0	0	1	0	1

symbol “A7”

(3) Frame length : Noumber of bytes contained within the PSDU is expressed as a 7 bit value.

(4) PSDU (PHY layer service data unit) : PHY layer data frame

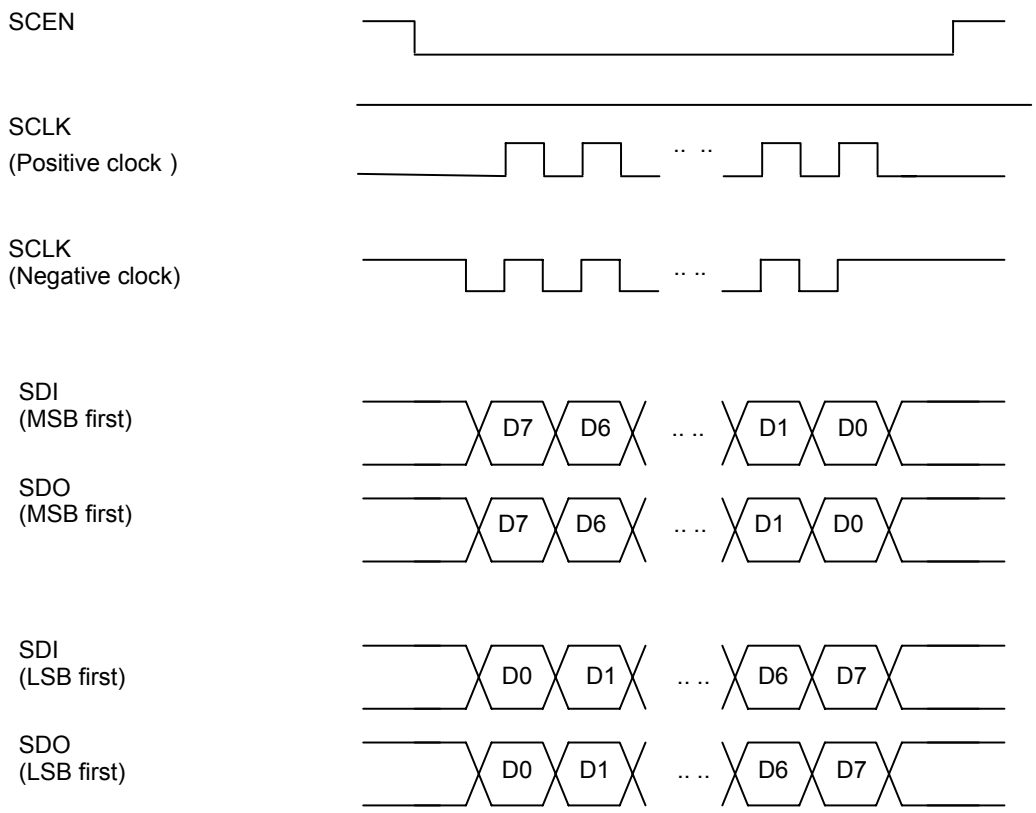
▪ Synchronous communication interface function (SCI)

The CX1540 includes a slave SCI interface for connection to any microcontroller.

The host may determine when there is data to be read from the CX1540 through the SINT pin or by reading a single byte through the SCI interface.

Waveform definition:
The data from the host MCU should be valid for the rising edge of SCLK
The SCI mode may be changed by the setting of the mode pins. Either LSB first or MSB first may be selected.

Note: in suspend mode there are restrictions to the SCLK frequency. Please refer to the SCI characteristics.



SCI clock data transmission waveform

Transaction details：
When the first byte is transmitted, an exchange of request and status is carried out between the host (processor) and the CX1540. If a connection between the host and the CX1540 in at least one direction is possible, then data transmission is carried out for subsequent bytes.

Transmission of the first bytes
When the host sends a request byte to CX1540, a status data byte is simultaneously sent back to the host. For request and status, only bits 1 and 0 are used as shown below. The remaining bits are 'Don't care'.
When bit 1, which is sent by both the host and the CX1540 is "1", data writing (second byte etc) starts from host to CX1540. If bit 0 is "1", data reading (second type etc) of CX1540 from host starts.

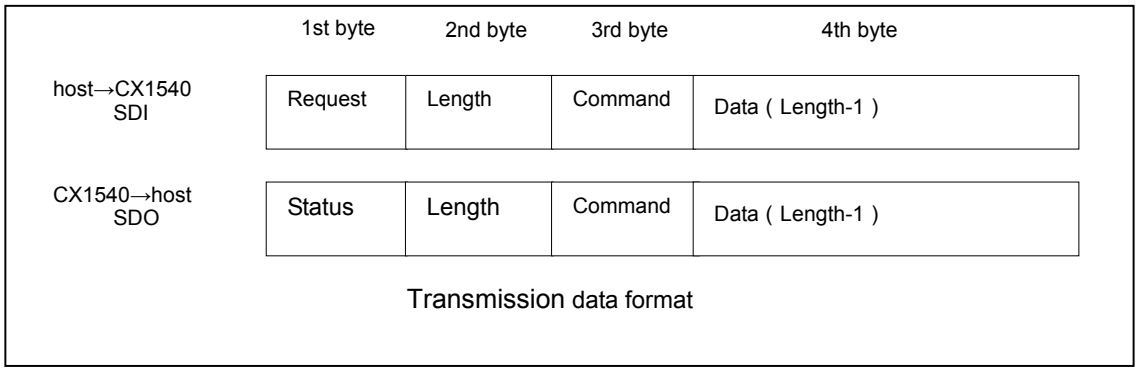
Bit	Request (host → CX1540)	Status (CX1540 → host)
1	Requirement for data writing	Data writing enable
0	Data reading enable	Requirement for data reading

The second byte indicates the number of bytes to be included in this data transfer.

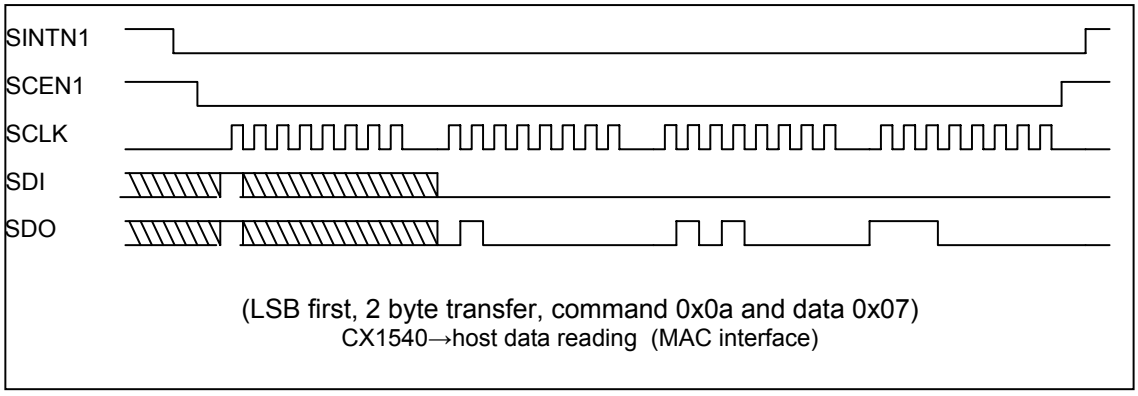
The third and subsequent bytes are the command and data to be sent to, or received from, the 802.15.4 MAC interface.

Transmission data format and the timing charts are shown below.
The CX1540 has two functions, referred to as the 802.15.4 MAC function and The IC control function, the access to each of these are shown below.

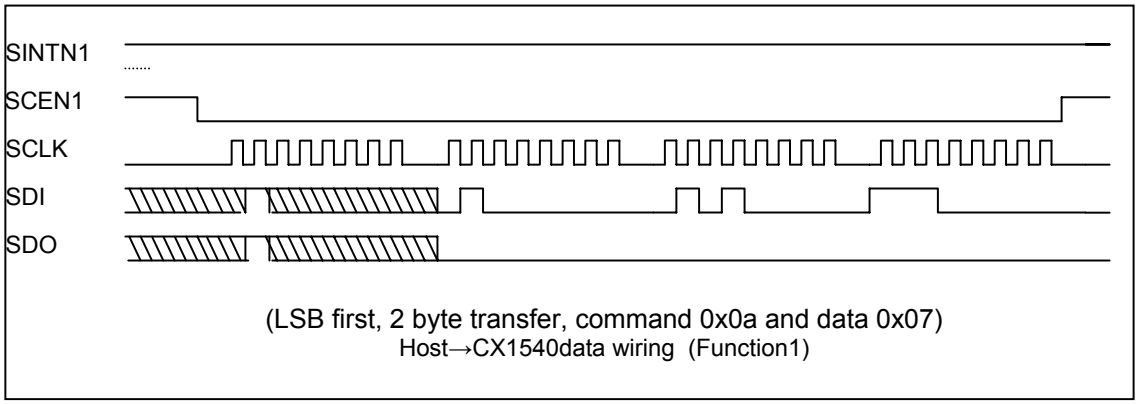
- Transmission data format for the 802.15.4 MAC function.



Transmission data format



(LSB first, 2 byte transfer, command 0x0a and data 0x07)
CX1540→host data reading (MAC interface)



(LSB first, 2 byte transfer, command 0x0a and data 0x07)
Host→CX1540data wiring (Function1)

Note: Unasserting SCEN1 during a transaction is not recommended.

● Transmission data format for the IC control function

As the IC control function is made of two parts, the SCI transmission data format is split into “writing to CX1540” and “reading from CX1540”.

Once a command has been written, an interrupt is generated, and then data may be read from the CX1540. The two steps are described, namely ① writing command, ② command reading.

Step ①：Command writing

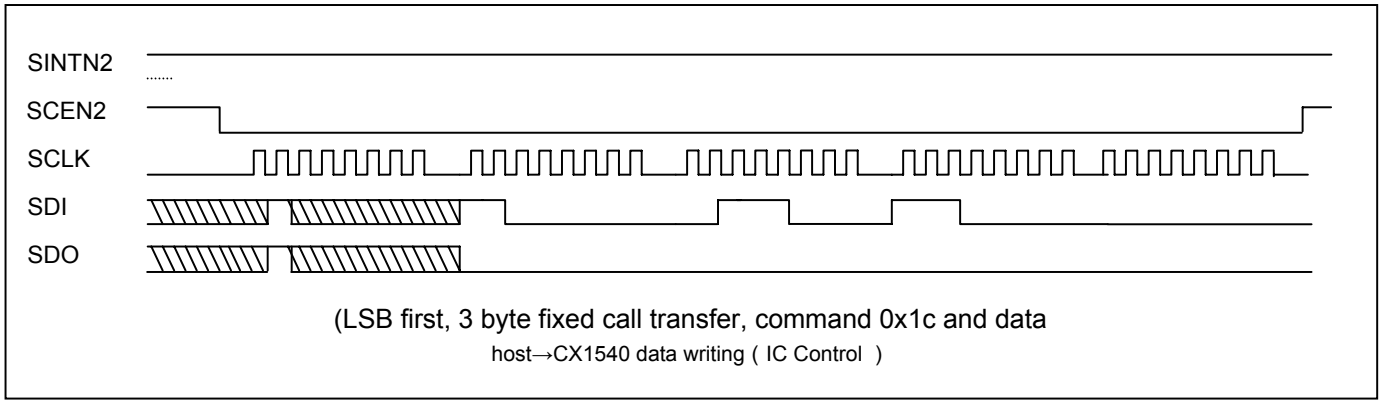
	Byte 1	Byte 2	Byte 3
・host→CX1540 sdi	Request	0x01	Command

Transmission data format（Config parallel command write）

Step ②：Command reading

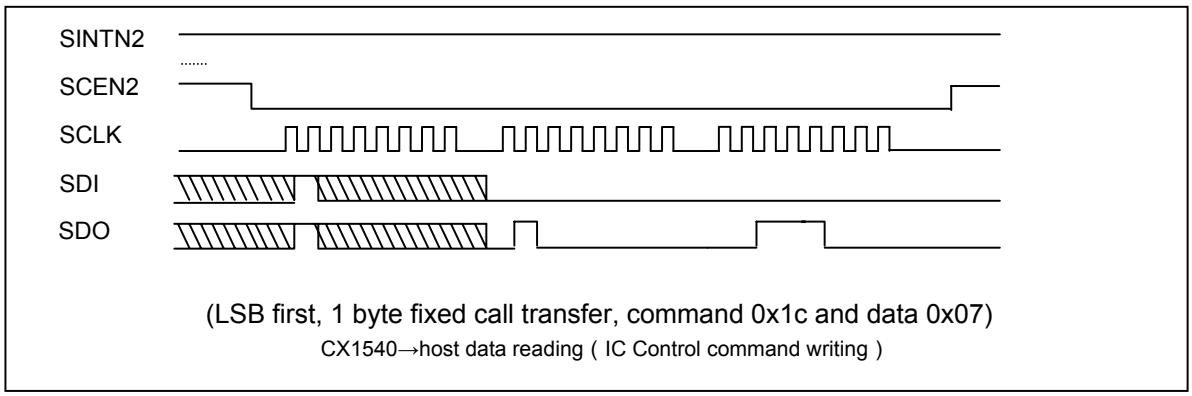
	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
・CX1540→host sdo	Status	0x03	Command	Data [7:0]	Data

Transmission data format（Config parallel read）



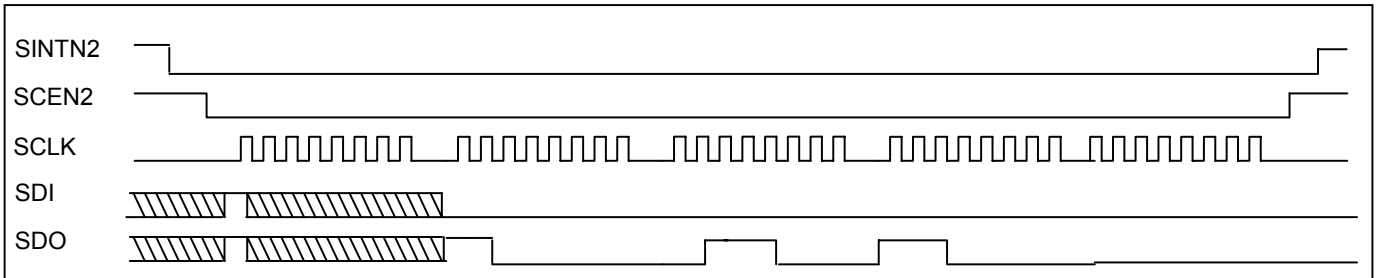
(LSB first, 3 byte fixed call transfer, command 0x1c and data

host→CX1540 data writing (IC Control)



(LSB first, 1 byte fixed call transfer, command 0x1c and data 0x07)

CX1540→host data reading (IC Control command writing)



CX1540→host data reading (IC Control command writing)

(LSB first, 3 byte fixed call transfer, command 0x1c and data 0x07)

▪ Command summary

Cmd	Name	Function	Function*
0x1b	RST_CTL0	Reset control (enable setting)	IC Control
0x1c	RST_CTL1	Reset control (soft reset)	IC Control
0x1d	CLK_CTL0	Clock control (Stop/Execute)	IC Control
0x1e	CLK_CTL1	Clock control (external clock divide)	IC Control
0x40	MCPS_DATA.request	See note.	MAC interface
0x41	MCPS_DATA.confirm	See note.	MAC interface
0x42	MCPS_DATA.indication	See note.	MAC interface
0x43	MCPS_PURGE.request	See note.	MAC interface
0x44	MCPS_PURGE.confirm	See note.	MAC interface
0x45	MLME_ASSOSIATE.request	See note.	MAC interface
0x46	MLME_ASSOSIATE.confirm	See note.	MAC interface
0x47	MLME_ASSOSIATE.indication	See note.	MAC interface
0x48	MLME_ASSOSIATE.responce	See note.	MAC interface
0x49	MLME_DISASSOSIATE.request	See note.	MAC interface
0x4a	MLME_DISASSOSIATE.confirm	See note.	MAC interface
0x4b	MLME_DISASSOSIATE.indication	See note.	MAC interface
0x4c	MLME_BEACON_NOTIFY.indication	See note.	MAC interface
0x4d	MLME_GET.request	See note.	MAC interface
0x4e	MLME_GET.confirm	See note.	MAC interface
0x4f	MLME_GTS.request	See note.	MAC interface
0x50	MLME_GTS.confirm	See note.	MAC interface
0x51	MLME_GTS.indication	See note.	MAC interface
0x52	MLME_ORPHAN.indication	See note.	MAC interface
0x53	MLME_ORPHAN.responce	See note.	MAC interface
0x54	MLME_RESET.request	See note.	MAC interface
0x55	MLME_RESET.confirm	See note.	MAC interface
0x56	MLME_RX_ENABLE.request	See note.	MAC interface
0x57	MLME_RX_ENABLE.confirm	See note.	MAC interface
0x58	MLME_SCAN.request	See note.	MAC interface
0x59	MLME_SCAN.confirm	See note.	MAC interface
0x5a	MLME_COMM_STATUS.indication	See note.	MAC interface
0x5b	MLME_SET.request	See note.	MAC interface
0x5c	MLME_SET.confirm	See note.	MAC interface
0x5d	MLME_START.request	See note.	MAC interface
0x5e	MLME_START.confirm	See note.	MAC interface
0x5f	MLME_SYNC.request	See note.	MAC interface
0x60	MLME_SYNC_LOSS.indication	See note.	MAC interface
0x61	MLME_POLL.request	See note.	MAC interface
0x62	MLME_POLL.confirm	See note.	MAC interface

Note: Please refer to IEEE802.15.4 –2003 for 0x40 to 0x62 commands.
For the IC Control function, addresses other than those listed are reserved and should not be used.

▪ IC Control Function Descriptions

【RST_CTL0】

function : soft reset control
Command : 0x1b
access : IC Control
initial value : 0x000f

Bit	Register name	Function	R/W	Initial value
15-4	Reserved	Reserved	RO	0000_0000_0000
3	OTHR_RSTN_EN	global Soft Reset enable	R/W	1
2	RF_RSTN_EN	enable RF module reset on soft reset	R/W	1
1	MOD_RSTN_EN	enable MODEM reset on soft reset	R/W	1
0	M_P_RSTN_EN	enable MAC and PHY reset on soft reset	R/W	1

【RST_CTL1】

Function : soft reset control
Command : 0x1c
Access : IC Control
Initial value : 0x0000

Bit	Register name	Function	R/W	Initial value
15-8	Reserved	Reserved	RO	0000_0000
7	SRSTN_INSIDE	Soft Reset	R/W	0
6-0	Reserve	Reserved	RO	000_0000

Writing '1' to bit 7 will cause a soft reset. The bit is automatically cleared when the reset is complete.

【CLK_CTL0】

Function : clock control.
Command : 0x1d
Access : IC Control
Initial Value : 0x0000

Bit	Register name	Function	R/W	Initial value
15	SLEEP	Disable all clocks including OSC	R/W	0
14	SUSPEND	Disable all clocks excluding OSC	R/W	0
13	STOP_CLK	Enable MAC clock power saving	RO	0
12-0	Reserved	Reserved	RO	0_000

Returning from sleep mode to normal mode is only possible through the SRRESET pin
Returning from suspend to normal mode is possible by clearing the suspend bit.

【CLK_CTL1】

Function : Clock control
Command : 0x1e
Access : IC Control
Initial value : 0x0020

Bit	Register name	Function	R/W	Initial value
15	OUT_CLK_SEL	Fundamental clock to be chosen 0 : 2MHz 1 : 16MHz	R/W	0
14-8	Reserved	Reserved	RO	000_0000
7-0	CLK_DIV_OUT	Divider value for external clock. Valid range: 1000_0000 – 0000_0000	R/W	0010_0000

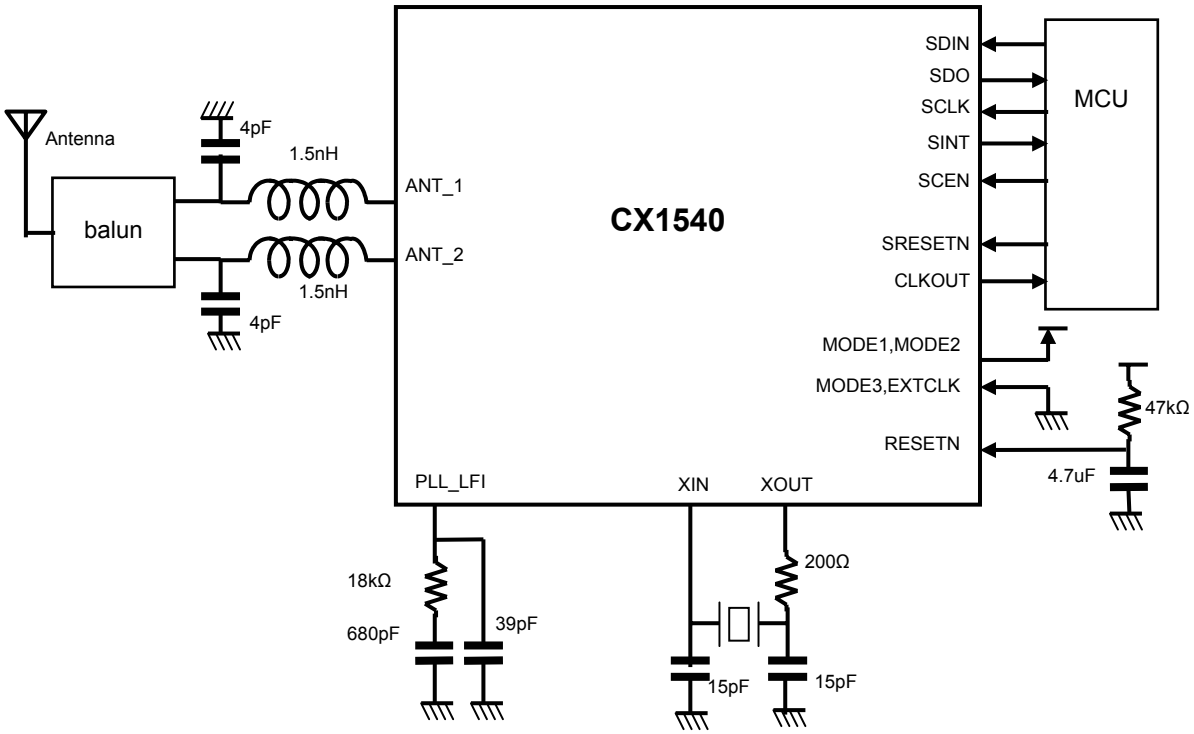
By default the frequency of the external clock is calculated as follows.
CLKOUT = 2MHz／32 division*2＝31.25kHz

If CLK_DIV_OUT is set to 0000_0000, clock division is not carried out and the clock OUT_CLK_SEL will be output to CLKOUT.

The CLK_OUT pin may be programmed to frequencies within the range :
OUT_CLK_SEL = 0 7.8125kHz－2MHz
OUT_CLK_SEL = 1 125kHz－16MHz

▪ Typical Application

For details on the layout of external parts, please refer to the CX1540 application note.



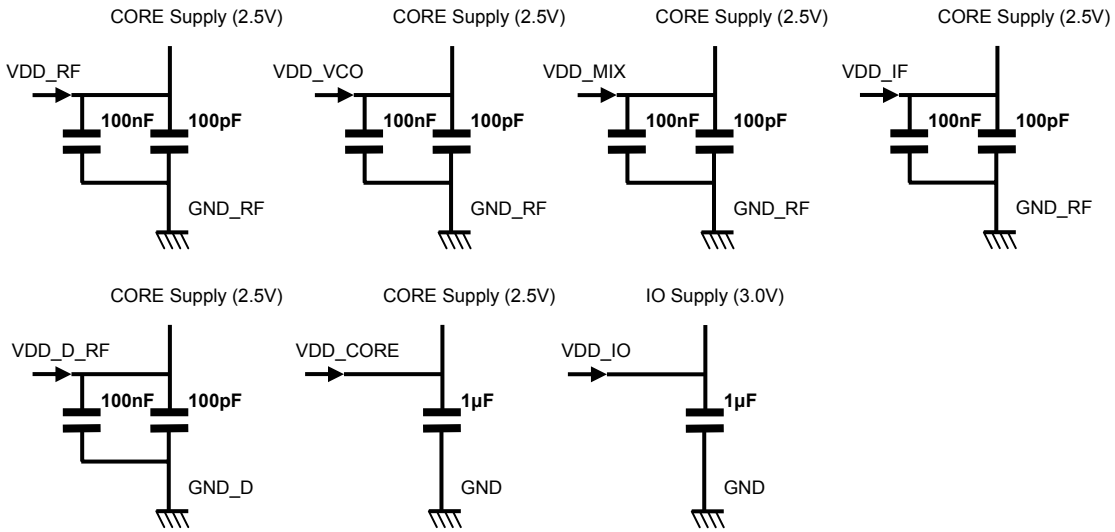
Note:

Power pins VDD_IO are the only ones which may operate at a level greater than 2.7V.
If VDD_IO is operated above 2.7V a regulator may be required for the other power pins.

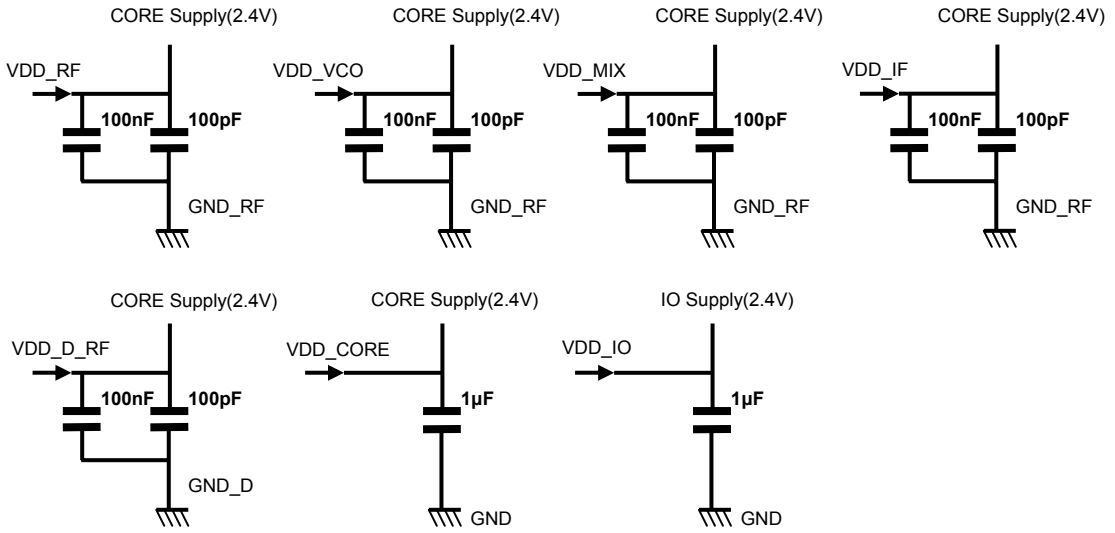
▪ Power Supply Decoupling

It is imperative that as close as possible to each power supply pin.

Supply voltage1 (standard supply voltage 3.0V)

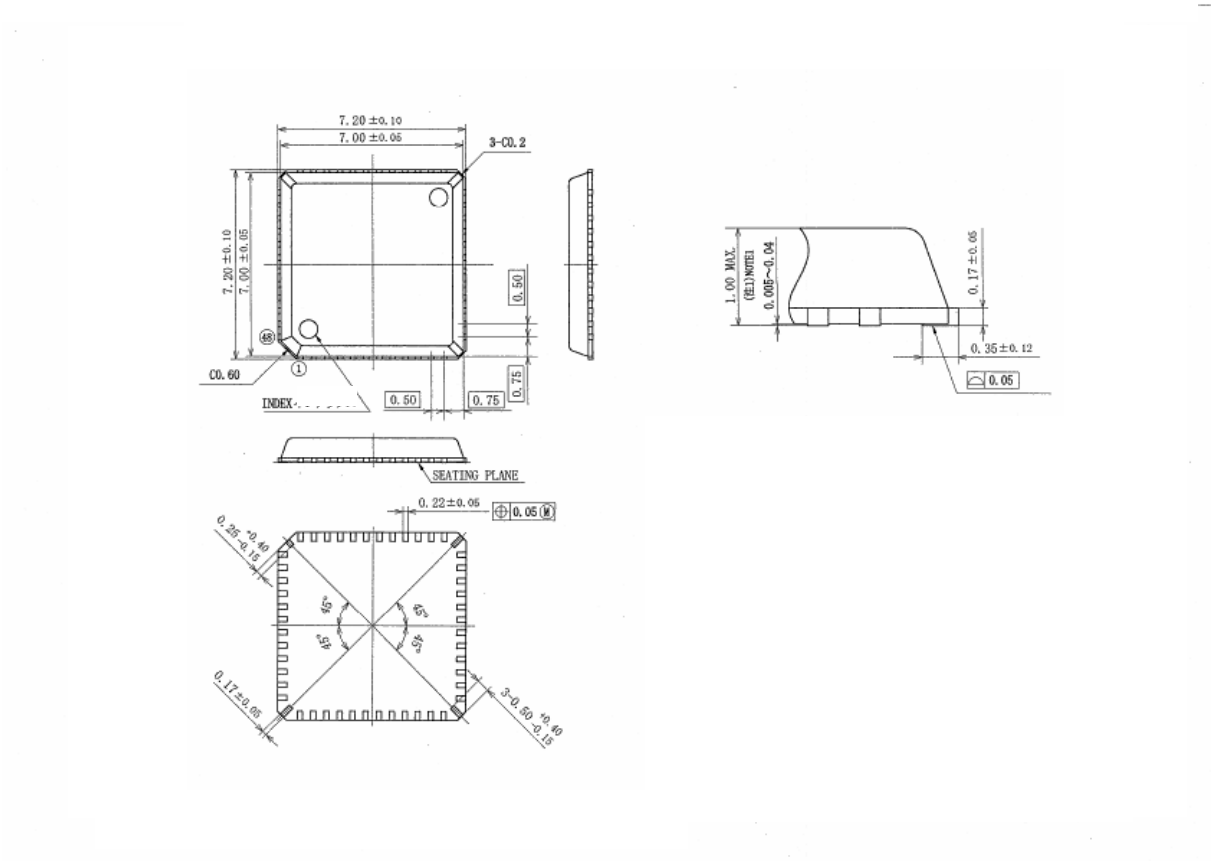


Supply voltage1 (standard supply voltage 2.4V)



- **Package dimension diagram**

48 Pin VQFN



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