Integrated Circuit Designs, Inc.

Product Data Sheet – Advanced Information

ICD9001 - RF Activity Monitor and Power Sequencer Broadband input from 100MHz – 2.5GHz

FEATURES

- Linear operating Range from 100MHz to 2.5GHz
- Unbalanced or Balanced Antenna Inputs
- Power Level Threshold Set Point Adjustment
- 3 Output Power Sequencer
- Compact 14-pin TSSOP Package
- Low external parts count
- Low power for battery operation

PIN CONFIGURATION



APPLICATIONS

- WiFi, ZigBee and BlueTooth Repeaters
- WLAN remote access point control
- WLAN Repeater Control

DESCRIPTION

The ICD9001is an RF receiver that monitors RF signal strength and detects when the power level has exceeded a user programmable threshold. This RF activity monitor detects and measures RF signals in the frequency range of 100MHz to 2.5GHz. The monitor is a logarithmic receiver whose output is a DC voltage that is linearly related to the RF input power in dB. This voltage is fed to an on-chip comparator with a user-programmable threshold. When power exceeds the threshold, a Signal Active output goes high, followed by three outputs from a power sequencing circuit.

The ICD9001 is designed to be used with any circuit that requires an RF power monitor for start up and/or shutdown of external circuits. The power sequencer is initiated when the RF input power crosses the user defined threshold level. Applications include low power WLAN repeaters where the repeater is powered up only when RF power is detected above a preset level.

The ICD9001 is available in a 14-pin TSSOP package. The low-power device consumes less than 6mA with a 3V supply.

- Consumer Gateway Sleep Mode
- RF Sniffers for Dosimeter Applications
- Medical Proximity Monitors



FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

PIN	Name	Function
1	IN LO	RF- Signal input. Must be capacitively coupled. This may be coupled to ground for single
		ended input
2	GND 1	Ground for first gain stages
3	GND 2	Ground for remaining gain stages and other circuits
4	SA	Signal Active – indicates RF power exceeds threshold. This signal goes false when power
		level falls below the threshold.
5	S1	Sequencer output 1 – goes true 5ms after SA. This signal goes false 30 seconds after SA
		goes false.
6	S2	Sequencer output 2 – goes true 10ms after S1. This signal goes false 30 seconds after SA
		goes false.
7	S3	Sequencer output 3 – goes true 35ms after S2. This signal goes false 30 seconds after SA
		goes false.
8	ENABLE	Low puts chip in power down mode (10uA current to operate)
9	T2	Threshold set digital input MSB (Threshold repeatability within 10%)
10	T1	Threshold set digital input middle bit
11	T0	Threshold set digital input LSB
12	VDD 2	Input voltage for remaining gain stages and other circuits (2V to 5.5V) Total current for VDD
		1 and VDD 2 is 5.6mA at 3V
13	VDD 1	Input voltage for first gain stages (2V to 5.5V)
14	IN HI	RF+ Signal input. Must be capacitively coupled. Input resistance is 1000 ohms, capacitance
		1.2pF at 0.1GHz. Dynamic range is 45dB.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Supply Voltage Range (VDD to GND)	V _{dd}	+6	V
Voltage on Any Other Pin to GND	V _{in}	-0.3 to (VDD+0.3)	V
Continuous Power Dissipation	Pd	457	mW
Operating Junction Temperature	T _a	0 to 85	°C
Storage Temperature Range	T _{stg}	-65 to 150	°C

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS TABLE

 $(V_{dd1} = V_{dd2} = +3V, \ V_{GND1} = V_{GND2} = 0V, \ V_{ENABLE} \ge (0.7xV_{dd})V)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Units
GENERAL						
Supply Voltage Range	V _{dd}	Running	2		5.5	V
Quiescent Supply Current	I _{dd}	Running		5	9	mA
Shutdown Current	Idd(/SHDN)	Enable Low			10	μΑ
INPUT						
Frequency Range	fmin fmax		0.1		2.5	GHz
Input Resistance	Rin	Differential, f=0.1GHz	750	1000	1400	Ohm
Input Capacitance	Cin	f=0.1 GHz		1.2		pF
Minimum Input Signal	Smin	Input with 50 Ohm Matching network		-60		dBm
Dynamic Range	Range			45		dB
OUTPUT						
Prop Delay to Signal	tdsa	Threshold at –60dBm, input with 50		6		us
Active		Ohm matching network, signal pulsed from –70dBm to full scale		-		pro
Prop Delay Signal Active to S1 Active	tds1		3.5	5	7.5	ms
Prop Delay S1 Active to S2 Active	tds2		7	10	15	ms
Prop Delay S2 Active to S3 Active	tds3		24	35	51	ms
S1-S3 max. low output	Voh	I _{OL} =100uA			0.1* Vdd	V
S1-S3 min. high output	Vol	I _{OH} =-100uA	Vdd* 0.9			
Prop delay from loss of active signal to S1,S2,S3 inactive	Tdsoff		20	30	45	S
RSSI Slope			25	29	35	mV/dB
RSSI Deviation vs. Temperature		Input –40dBm@600MHz			2	dB
RSSI Deviation vs. Supply Voltage		Input –40dBm@600MHz Vdd=2 to 5.5V, Temp = 25C			4	dB
RSSI Deviation vs. Input Frequency		Input -40dBm, Temp = 25C		17	30	dB
ENABLE						
Maximum Low Voltage	V _{il}				V _{dd} *.3	V
Minimum High Voltage	V _{ih}		V _{dd} *.7			V
Activation Time	tactive	From ENABLE high or Vdd >2V		33	100	us

DETAILED DESCRIPTION

The purpose of the RF activity monitor is to allow the detection and measurement of RF signal present in the frequency range of 100MHz to 2.5GHz. The monitor is basically a logarithmic receiver whose output is a DC voltage that is linearly related to the RF input power in dB. The IC includes a user programmable threshold comparator and a power up sequencing circuit. The power sequencer is initiated when the RF input power crosses the user-defined threshold level.

Applications include low power WLAN repeaters where the repeater is powered up only when RF power is detected in the appropriate input band.

A simplified block diagram for the RF activity monitor is shown in the Functional Block Diagram on page 1. The logarithmic receiver utilizes successive approximation architecture that is composed of a string of limiting amplifiers and full wave rectifiers (FWR). The output voltage of each limiter is converted to rectified currents in the FWR. The current outputs of each FWR are summed into a resistor and filtered to extract a DC voltage that is proportional the input signal level in dB. This signal is referred to as the Received Signal Strength Indicator or RSSI. A typical plot of the RSSI output voltage as a function of the RF input power in dBm is shown below in Figure 2.



FIGURE 2 – TYPICAL RSSI OUTPUT VS. INPUT SIGNAL

A fully integrated programmable threshold comparator and power sequencer is also provided. The programmable threshold comparator monitors the filtered RSSI voltage and initiates the power sequencing circuit once the RSSI exceeds the programmed threshold voltage. The voltage threshold is set to one of eight steps via three digital programming bits. Figure 3 shows the typical RF input power level required to switch the comparator for each program setting.



FIGURE 3 – TYPICAL RSSI TRIP VOLTAGE VS. PROGRAM SETTING

The RSSI low pass filter is fully integrated with a corner frequency of 40MHz . Response time is expected to be 6uS to a full scale (-70 to -20 dBm) RF pulse.

The power sequencer block is composed of four logic outputs and associated timing circuitry. When the RF input power exceeds the programmed threshold the power sequencer is initiated. The three outputs S1-S3 are activated sequentially beginning with S1 and at 5, 10 and 35 mS intervals (see Timing Diagram). The sequencing begins after an initial 6 uS delay from the threshold crossing of the RF input. These outputs remain active so long as the RF input power is above threshold and for 30 seconds after the RF input power falls below threshold. De-activation occurs simultaneously from S3 to S1.

If the RF input power again crosses above the threshold before the 30 seconds de-activation timer has completed, the outputs remain active and the de-activation timer is reset until the RF power again crosses below the threshold.



FIGURE 4 – TYPICAL APPLICATION DIAGRAM – WLAN REPEATER

PACKAGE INFORMATION – 14 PIN TSSOP





S		COMMON DIMENSION(MILLIMETERS)							
- M B O	0.65mm LEAD PITCH				NOT	0.50mm LEAD PITCH			N O T
Ľ	MIN	-	NOM	MAX	Ē	MIN	NOM	MAX	Ē
A		-		1.10				1.10	
A1	0.0	5		0.15		0.05		0.15	
A2	0.8	5	0.90	0.95		0.85	0.90	0.95	
L	0.5	0	0.60	0.75		0.45	0.60	0.75	
R	0.0	9				0.09			
R1	0.0	ġ				0.09			
b	0.1	9		0.30	5	0.17		0.27	5
b1	0.1	θ	0.22	0.25		0.17	0.20	0.23	
S	0.0	ġ		0.20		0.09		0.20	
c1	0.0	ω		0.16		0.09		0.16	
Ð1	0.			8'		0"		8*	
L1	1.0 REF					1.0 REF			
aaa	0.10					0.10			
bbb	0.10					0.08			
666	0.05						0.05		
ddd	0.20						0.20		
e	0.65 BSC					0.50 BSC			
0 2	12" REF					12' REF			
Ø 3	12" REF					12' REF			
NC	DTE 1,2				1,2				
ISS	SUE A					A			
1									1

LIMITED PRODUCT LIABILITY STATEMENT

This information is believed to be correct and reliable at the time of publication, however, ICD reserves the right to change the preliminary circuitry and specifications at any time and without notice. No licenses are granted or implied.

ICD's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of ICD.

Approval / Notification address:

Documentation Control C/O President Integrated Circuit Designs, Inc. 3223-A Corporate Court Ellicott City, MD 21042

Tel:	410-750-9406
Fax:	410-750-9358