ILLUMINANT 北極光企業有限公司

PRODUCT SPECIFICATION FOR TFT LCM

CUSTOMER:	
MODEL NO:	I2812-7IPT2432A
ACCEPTED BY:	

APPROVED BY:	CHECKED BY:	ORGANIZED BY:
LCM產品部 2009.12.30 隆茂生	LCM產品部 2009.12.30 贺秋芳	LCM產品部 2009.12.30 贺秋芳

☐Approval for Specifications Only

■Approval for Specifications and Sample

Note: 1. Version of Specifications : 1

2. Others: Rohs Compliment

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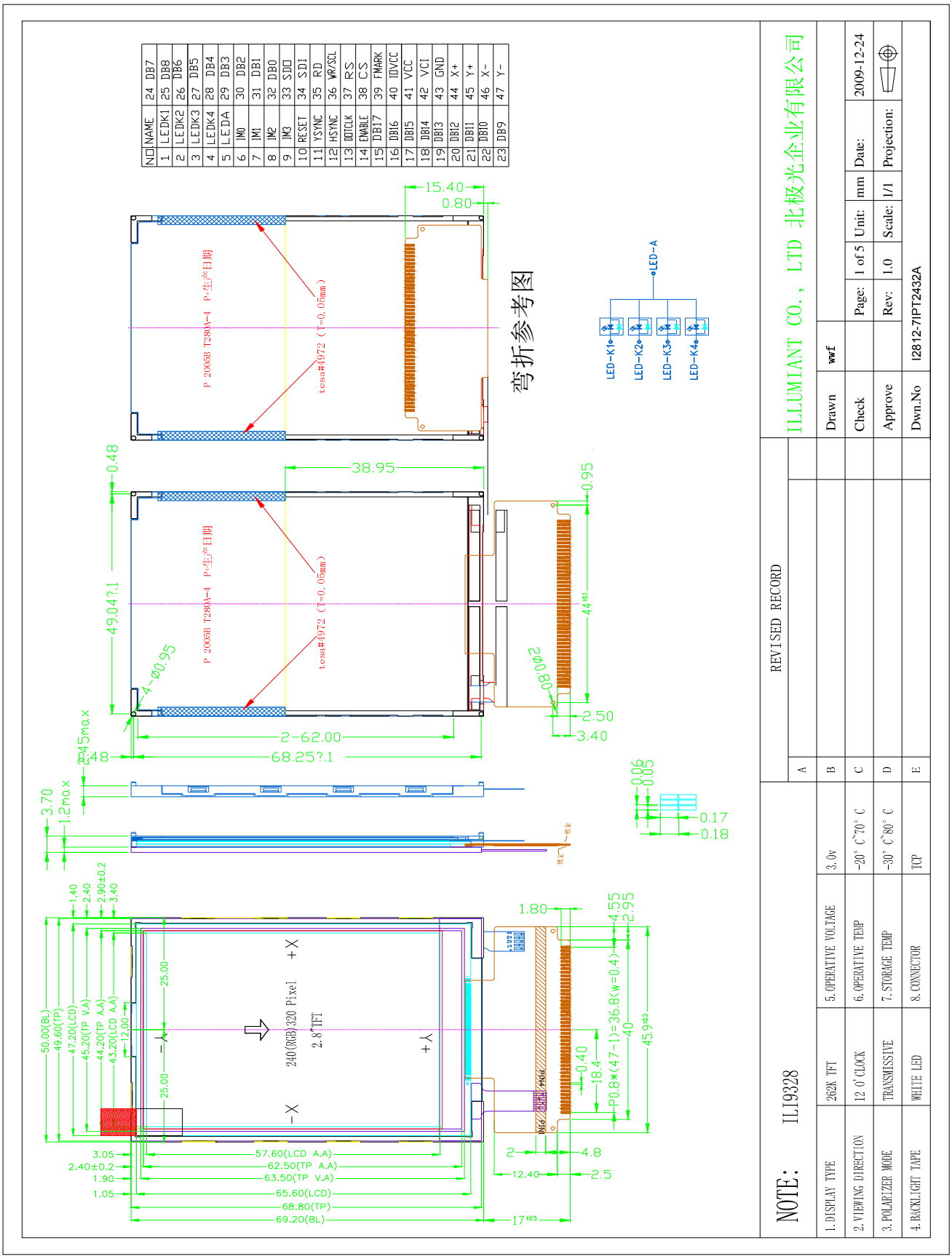
Version	Date	Contents
1	2009/12/30	New Version

CONTENTS

1.Mechanical Specification:

Item	Standard Value	Unit
Display size	2.83	inch
Module Dimension	69.2(H)*50.0(W)*3.7(D)	mm
Active Area(LCD)	43.2(W)*57.6(H)	mm
Viewing Area(T/P)	44.8(W)*63.1(H)	mm
Number of Dots	240(W)*3(RGB)*320(H)	Dot
LCD Type	TFT / Transmissive / Normal white	-
Viewing Direction	12H	-
Driver	ILI9328	-
Approx. Weight	TBD	g
Various color Display	262	K
Luminance	200	cd/m^2
Backlight Type	4-LED parallel	
Backlight Color	White	


NO NAME
1 LEDK1
2 LEDK2
3 LEDK3
4 LEDK4
5 LEDA
6 IM0
7 IM1
8 IM2
9 IM3
10 RESET
11 YSYNC
12 HSYNC
13 DOTCLK
14 ENABLE
15 DB17
16 DB16
17 DB15
18 DB14
19 DB13
20 DB12
21 DB11
22 DB10
23 DB9
24 DB7
25 DB8
26 DB6
27 DB5
28 DB4
29 DB3
30 DB2
31 DB1
32 DB0
33 SDO
34 SDI
35 RD
36 WR/SCL
37 RS
38 CS
39 FMARK
40 IOVCC
41 VCC
42 VCI
43 GND
44 X+
45 Y+
46 X-
47 Y-
弯折参考图
LED-A
LED-K1
LED-K2
LED-K3
LED-K4
15.40
0.80
38.95
0.48
0.95
2.50
3.40
2-62.00
68.25±0.1
3.70
1.2max
0.06
0.05
0.17
0.18
240(RGB)320 Pixel
2.8"TFT
57.60(LCD A.A)
62.50(TP A.A)
63.50(TP V.A)
65.60(LCD)
68.80(TP)
69.20(BL)
NOTE: ILI9328
REVISED RECORD
ILLUMIANT CO., LTD 北极光企业有限公司
Drawn wwf
Check
Approve
Dwn.No I2812-7IPT2432A
Page: 1 of 5
Rev: 1.0
Unit: mm
Scale: 1/1
Date: 2009-12-24
Projection:
1. DISPLAY TYPE 262K TFT
2. VIEWING DIRECTION 12 O' CLOCK
3. POLARIZER MODE TRANSMISSIVE
4. BACKLIGHT TAPE WHITE LED
5. OPERATIVE VOLTAGE 3.0v
6. OPERATIVE TEMP -20° C~70° C
7. STORAGE TEMP -30° C~80° C
8. CONNECTOR TCP

2.Absolute Maximum Ratings:

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Logic	V_{DD}	-0.3		+4.0	V	
Input voltage	V_{IN}	-0.5		VDD+0.3	V	
Operating Temperature	T_{OP}	-10	-	+60	℃	-
Storage Temperature	T_{ST}	-20	-	+70	℃	-

*NOTE: Based on Vss=0V.

3.Electrical Characteristics:

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage for Logic	V_{DD}	Ta=25℃	2.4	2.8	3.3	V
High-level input voltage	VIHC	VDD=2.8V	0.8VDD	-	VDD	
Low-level input voltage	VILC	VDD=2.8V	-0.3	-	0.2VDD	
TFT Gate ON Voltage	V_{GH}	VDD=2.8V	--	15	--	-
TFT Gate OFF Voltage	V_{GL}	VDD=2.8V	--	-8	--	V
TFT Common Electrode Voltage	VCOMH	VDD=2.8V	2.5	-	4.5	
	VCONL	VDD=2.8V	-2.0	-	0	
Power Supply Current for V_{DD}	I_{DD}	VDD=2.8V	-	-	7	mA

4. Optical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmittance	T(%)		5.8		%	Fig.1
Luminance	I	180	200		cd/m	
Contrast Ratio	C/R	-	300			
Response time	Tr		10		ms	Fig.3
Response time	Tf		15		ms	Fig.3
CIE Color coordinate	Rx	-	0.6457	-	-	Fig.1
	Ry	-	0.3391	-	-	-
	Gx	-	0.3438	-	-	-
	Gy	-	0.6012	-	-	-
	Bx	-	0.1476	-	-	-
	By	-	0.1110	-	-	-
	Wx	-	0.313	-	-	-
	Wy	-	0.329	-	-	-
*1) Viewing angle	Θl	-	50	-	Degree	C/R>10 Fig.4
	Θr	-	50	-		
	Θu	-	60	-		
	Θd	-	55	-		

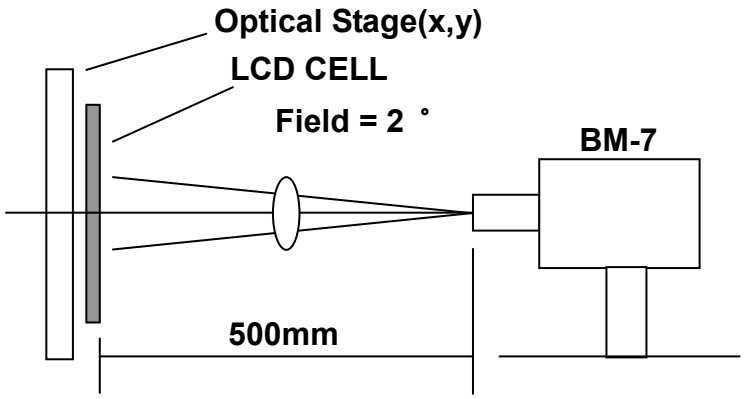
Notes :

1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the center point across the LCD surface 500mm from the surface with all pixels displaying white. For more information see FIG 1.
3. Response time is the time required for the display to transition from to black(Rise Time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see FIG 3.
4. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 5.
5. Optimum contrast is obtained by adjusting the LCD Threshold voltage(Vth & Vsat)

FIG. 1 Optical Characteristic Measurement Equipment and Method



<Transmissive Mode>

FIG. 2 The definition of Vth and Vsat

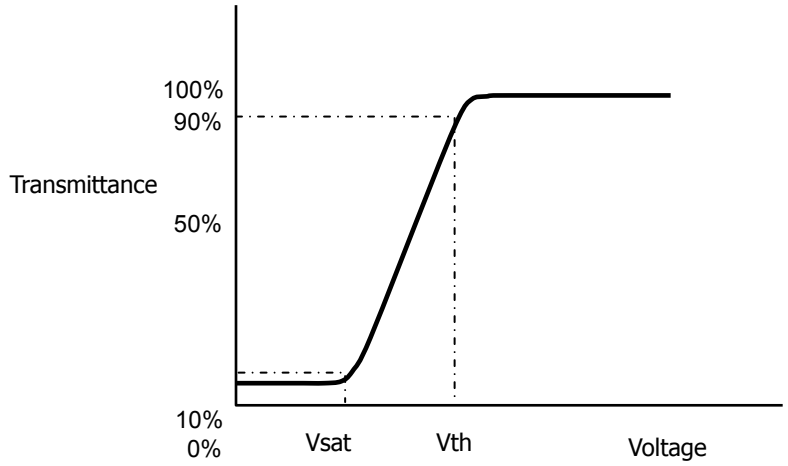


FIG. 3 The definition of Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

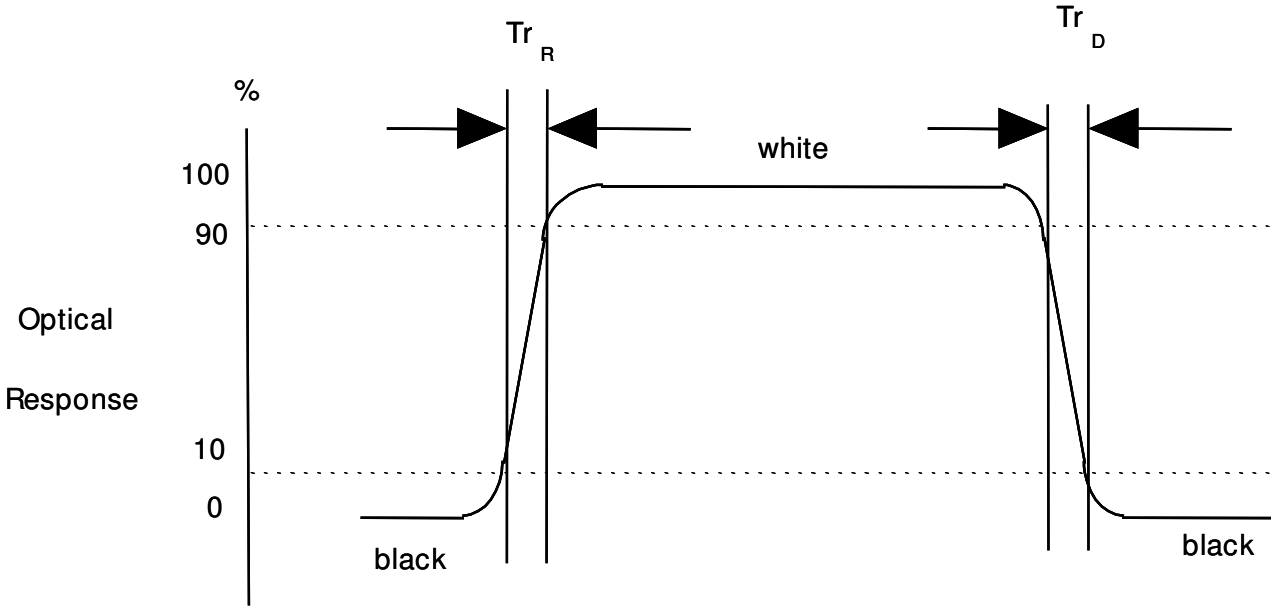
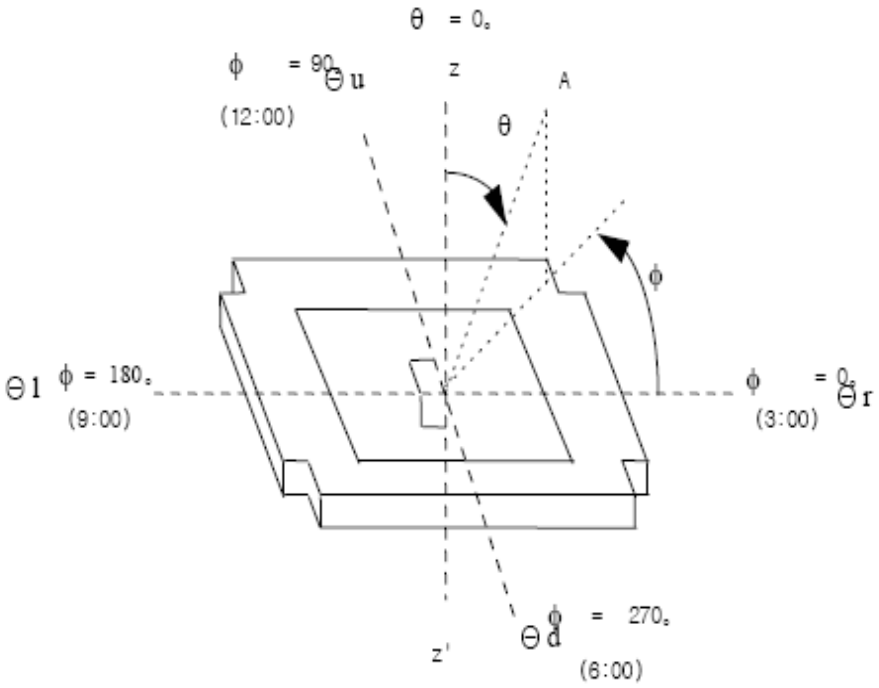


FIG. 4 The definition of viewing angle

<dimension of viewing angle range>



5. Interface:

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Level</th><th>Description</th></tr>
<tr><td>1~4</td><td>LEDK1~4</td><td>-</td><td>LED light cathode</td></tr>
<tr><td>5</td><td>LEDA</td><td>-</td><td>LED light anode</td></tr>
<tr><td rowspan="4">6~9</td><td>IM0</td><td rowspan="4">H/L</td><td rowspan="4">Select a mode to interface to an MPU. In SPI mode, the IM0 pin is used to set the ID of device code.

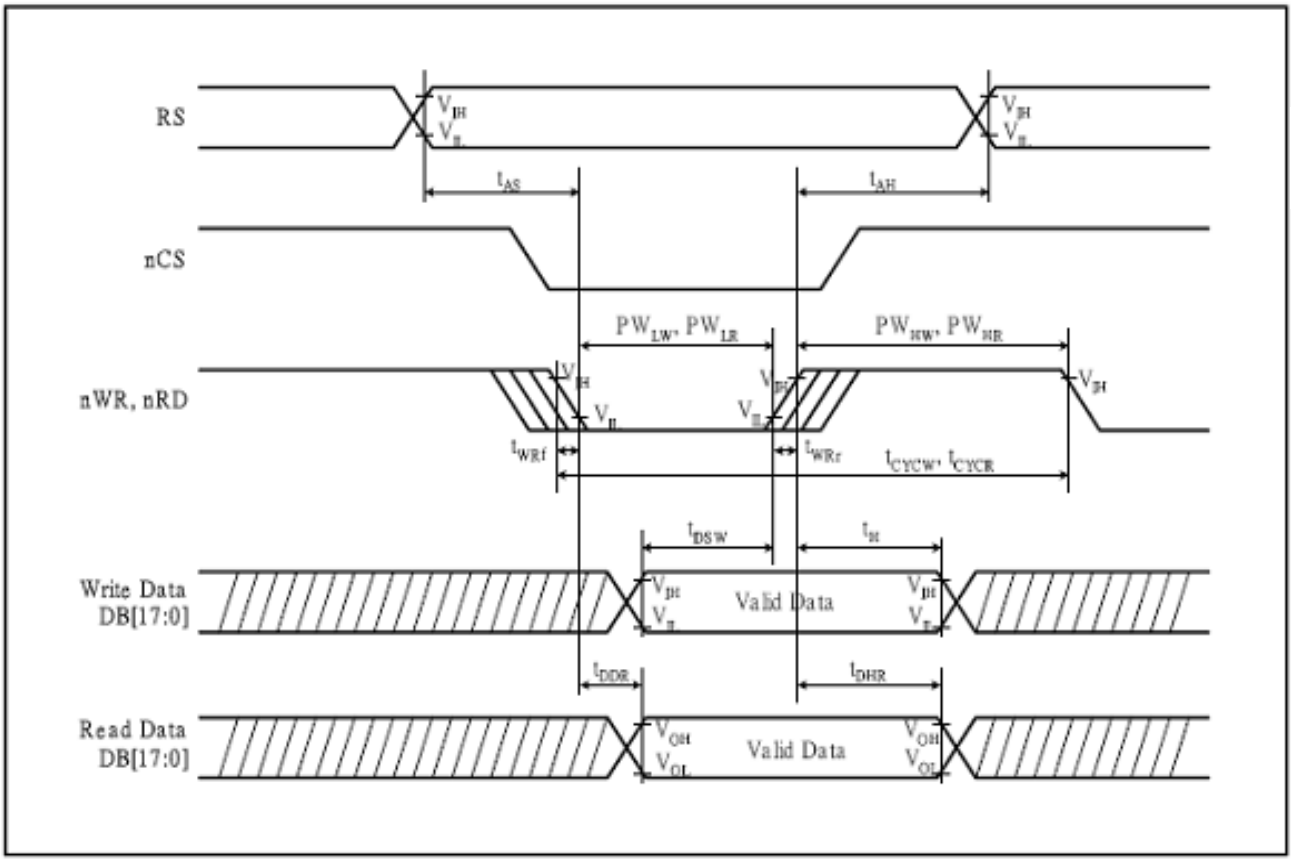
<table>
<tr><th>IM[3:0]</th><th>Interface Mode</th><th>DB Pins</th></tr>
<tr><td>000*</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>0010</td><td>80-system 16-bit interface</td><td>DB[17:10]
DB[8:1]</td></tr>
<tr><td>0011</td><td>80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>010*</td><td>Serial peripheral interface (SPI)</td><td>SDI, SDO</td></tr>
<tr><td>011*</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>100*</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1010</td><td>80-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1011</td><td>80-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>11**</td><td>Setting disabled</td><td>-</td></tr>
</table></td></tr>
<tr><td>IM1</td></tr>
<tr><td>IM2</td></tr>
<tr><td>IM3</td></tr>
<tr><td>10</td><td>RESET</td><td>H/L</td><td>Reset signal</td></tr>
<tr><td>11</td><td>VSYNC</td><td>H/L</td><td>Frame synchronous signal for RGB interface operation</td></tr>
<tr><td>12</td><td>HSYNC</td><td>H/L</td><td>Line synchronous signal for RGB interface operation</td></tr>
<tr><td>13</td><td>DOTCLK</td><td>H/L</td><td>Dot clock signal for RGB interface operation</td></tr>
<tr><td>14</td><td>ENABLE</td><td>H/L</td><td>Data enable signal for RGB interface operation</td></tr>
<tr><td>15~32</td><td>DB17~DB0</td><td>H/L</td><td>Data bus</td></tr>
<tr><td>33</td><td>SDO</td><td>H/L</td><td>Serial data output pin in SPI mode</td></tr>
<tr><td>34</td><td>SDI</td><td>H/L</td><td>Serial data input pin in SPI mode</td></tr>
<tr><td>35</td><td>RD</td><td>H/L</td><td>Read signal</td></tr>
<tr><td>36</td><td>WR/SCL</td><td>H/L</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when WR is low. Synchronous clock signal (SCL) in serial interface operation</td></tr>
<tr><td>37</td><td>RS</td><td>H/L</td><td>Command / data select</td></tr>
<tr><td>38</td><td>CS</td><td>H/L</td><td>Chip selection</td></tr>
<tr><td>39</td><td>FMARK</td><td>H/L</td><td>Frame head pulse signal</td></tr>
<tr><td>40</td><td>IOVCC</td><td>1.65~3.3V</td><td>Interface I/O power supply</td></tr>
<tr><td>41</td><td>VCC</td><td>2.5~3.3V</td><td>Logic regulator power supply</td></tr>
<tr><td>42</td><td>VCI</td><td>2.5~3.3V</td><td>Liquid crystal analog circuit power supply</td></tr>
<tr><td>43</td><td>GND</td><td>0V</td><td>Ground</td></tr>
<tr><td>44</td><td>X+</td><td>-</td><td>Touch panel coordinate in the right side of envisage drawing</td></tr>
<tr><td>45</td><td>Y+</td><td>-</td><td>Touch panel coordinate in the down side of envisage drawing</td></tr>
<tr><td>46</td><td>X-</td><td>-</td><td>Touch panel coordinate in the left side of envisage drawing</td></tr>
<tr><td>47</td><td>Y-</td><td>-</td><td>Touch panel coordinate in the up side of envisage drawing</td></tr>
</table>

6. Timing Control:

6.1 I80-system Interface timing characteristics

Normal Write Mode (IOVCC=1.65~3.3V, VCC=2.4~3.3V)

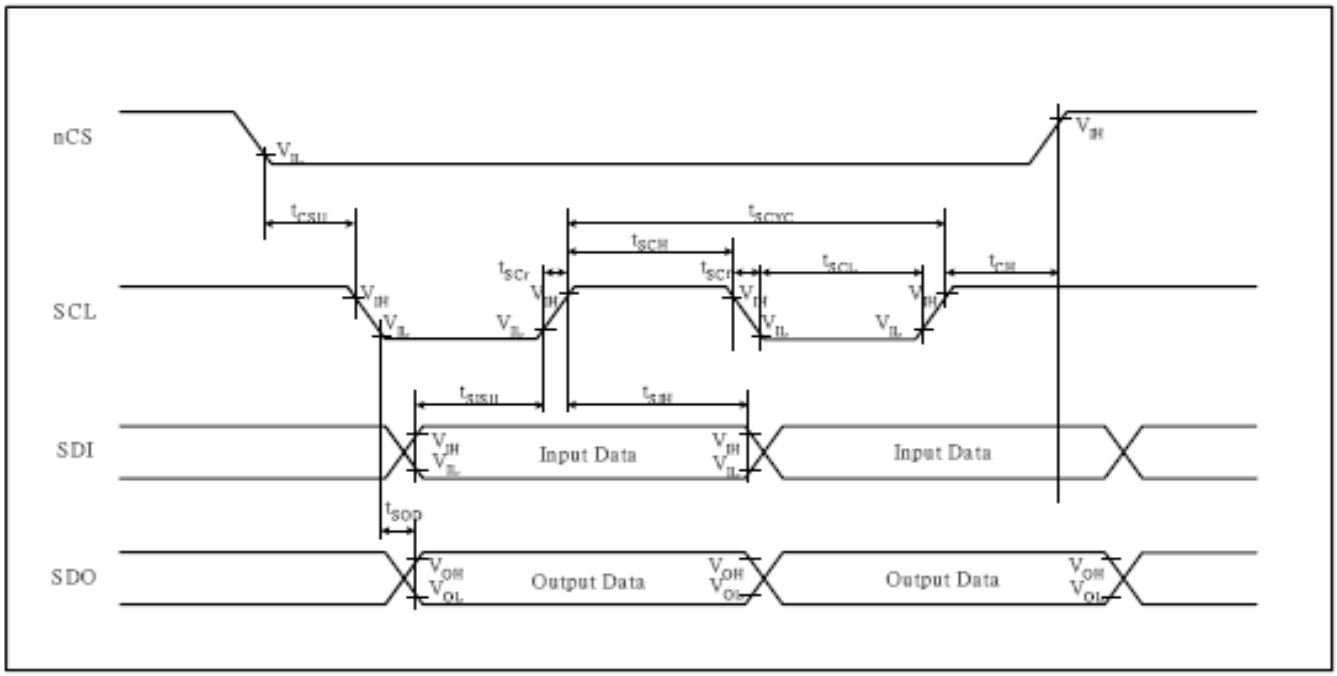
Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	100	-	-	-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	50	-	500	-
Write high-level pulse width		PW_{HW}	ns	50	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / Fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5		-	
Write data set up time		t_{DSW}	ns	10		-	
Write data hold time		t_H	ns	15		-	
Read data delay time		t_{DDR}	ns	-		100	
Read data hold time		t_{DHR}	ns	5		-	



6.2 serial data transfer interface timing characteristics

(IOVCC=1.65~3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write(received)	t_{SCYC}	μs	100	-	-	
	Read(transmitted)	t_{SCYC}	μs	200	-	-	
Serial clock high-level Pulse width	Write(received)	t_{SCH}	ns	40	-	-	
	Read(transmitted)	t_{SCH}	ns	100	-	-	
Serial clock low-level Pulse width	Write(received)	t_{SCL}	ns	40	-	-	
	Read(transmitted)	t_{SCL}	ns	100	-	-	
Serial clock rise / fall time		t_{SCR}, t_{SCR}	ns	-	-	5	
Chip select set up time		t_{CSU}	ns	10	-	-	
Chip select hold time		t_{CH}	ns	50	-	-	
Serial input data set up time		t_{SISU}	ns	20	-	-	
Serial input data hold time		t_{SIH}	ns	20	-	-	
Serial output data set up time		t_{SOD}	ns	-	-	100	
Serial output data hold time		t_{SOH}	ns	5	-	-	



6.3 RGB interface timing characteristics

18/16-bit Bus RGB Interface Mode (IOVCC=1.65~3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	--	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	--	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	--	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rgbr}, t_{rgbf}	ns	-	-	25	-

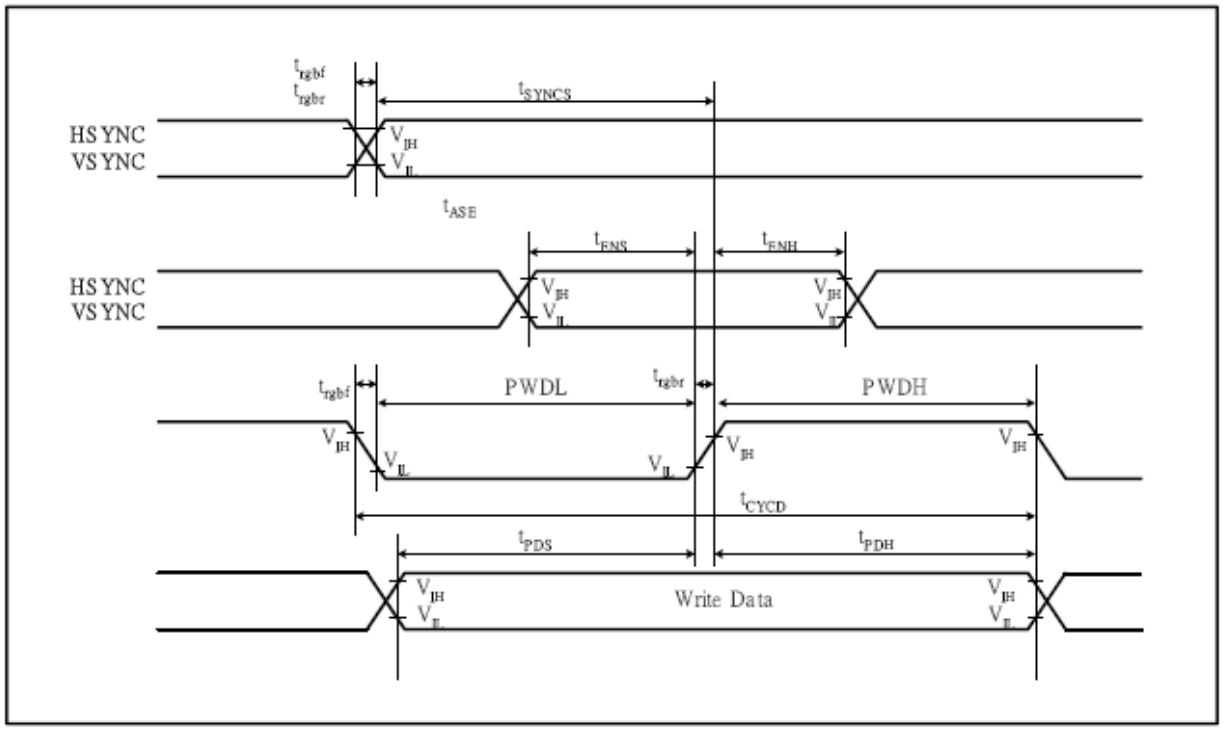


Figure52 RGB Interface Timing

7.Backlight:

7.1 Standard Lamp Styles (Edge Lighting Type):

The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

7.2 The Main Advantages of the LED Backlight are as Following:

The brightness of the backlight can simply be adjusted. By a resistor or a potentiometer.

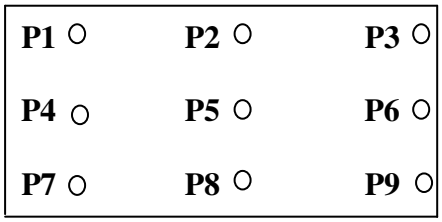
7.3 Data About LED Backlight:

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition
Forward voltage	Vf	-	3.2	3.5	V	If=60mA
Reverse voltage	Vr	-	-	5.0	V	-
Forward current	If	-	60	80	mA	4-chip parallel
Power Consumption	-	-	192	280	mW	If=60mA
Uniformity(with L/G)	-	80%	-	-	%	If=60mA
Color	White					
Chip connection	4- chip parallel connection					

NOTE:

1.Backlight Only
2.Average Luminous Intensity of P1-P9
3.Uniformity = Min(P1~P9)/Max(P1~P9) * 100%>80%

7.4 Measured Method:



(Effective spatial Distribution)
Hole Diameter±1ø ; 1 to 9per Position Measured Luminous

8.Reliability:

8.1 MTTF

The LCD module shall be designed to meet a minimum MTTF value of 50,000 hours with normal condition. (25°C in the room without sunlight; not include lifetime of backlight and Touch Panel).

8.2 Tests

No.	Item	Condition	Criterion
1	High Temperature Operating	+70°C 240hrs	。No defect of operational function in room temperature are allowable(23±5°C). 。Leakage current should be below double of initial value.
2	Low Temperature Operating	-20°C 240hrs	
3	High Temperature Non-Operating	+80°C 240hrs	
4	Low Temperature Non-Operating	-30°C 240hrs	
5	High Temperature / Humidity Non-Operating	60°C ; 90%RH ; 240hrs	
6	Temperature Shock Operating	-20°C ←→ 70°C (30min) (5min) (30min) 50 Cycles	
7	Electro-Static Discharge	HBM : ±2kv	

Note 1: Test after 24 hours in room temperature(23±5°C).

Note 2: The sampling above is individually for each reliability testing condition.

Note 3: The color fading of polarizing filter should not care.

Note 4: All of the reliability testing chamber above, is using D.I. water.(Min value:1.0 MΩ-cm)

Note 5: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

9.Inspection Criteria:

9.1 Inspection Conditions

9.1.1 Environmental Conditions

The environmental conditions for inspection shall be as follows

Room Temperature : 23±5°C

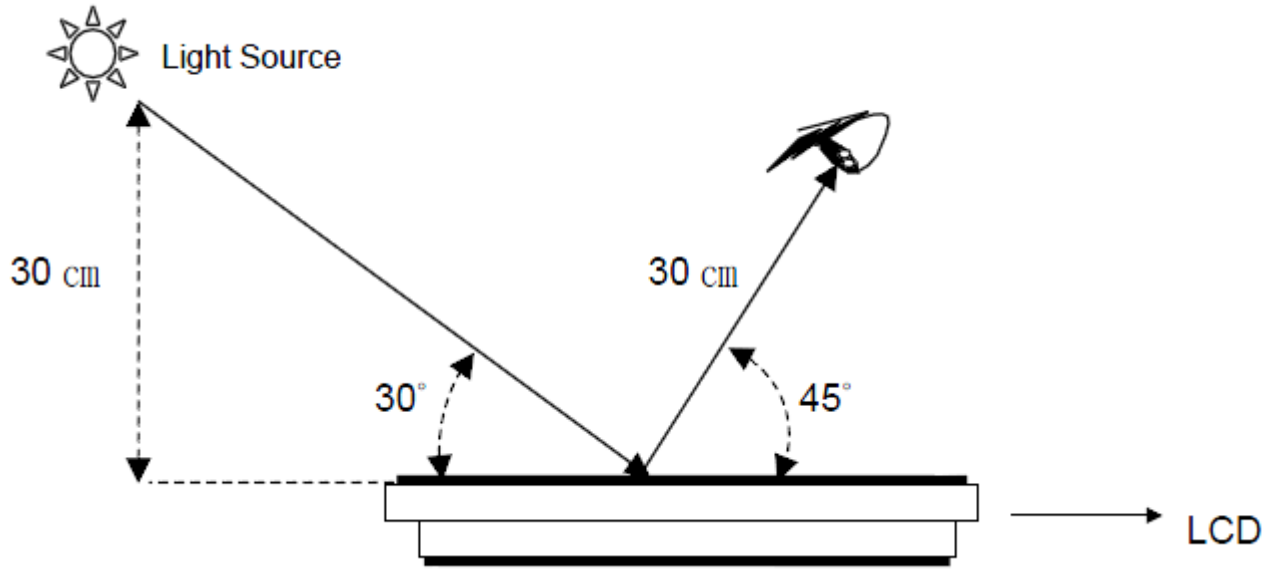
Humidity : 50±20%RH

9.1.2 The External Visual Inspection

With 1000±200 lux fluorescent lamp as the light source, the inspection was in the distance of 30cm or more from the LCD to the inspector's eyes .

9.2 Light Method

1. Inspection is implemented over 30cm vertical distance and 30° incidence under 1000±200 lux. (As showed below)
2. Viewing direction for inspection over 30cm far and is 45° against from LCD (As showed below)



9.3 Classification of Defects

9.3.1 Major Defect

A major defect refers to a defect that may substantially degrade usability for product applications.

9.3.2 Minor Defect

A minor defect refers to a defect which is not considered to be able substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation.

Notes: If the LCD/LCM's cosmetic and display performance do not specify in "inspection criterion", it should be based on these delivered samples.

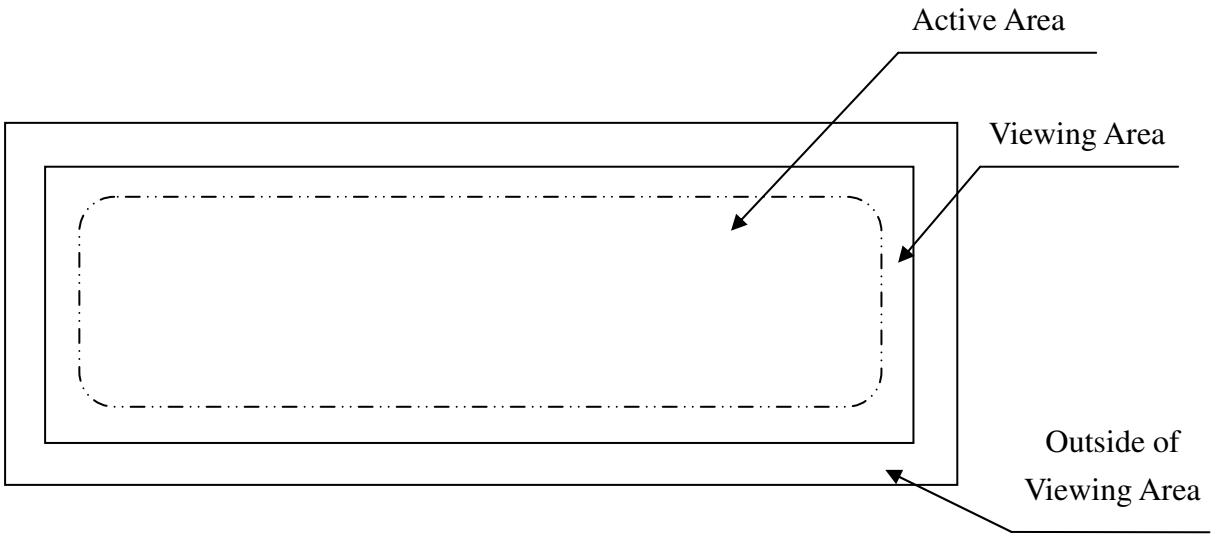
9.4 Sampling & Acceptable Quality Level

Inspection Item	Major Defect	Minor Defect
Cosmetic	1.0%	1.5%
Electrical Test	0.4%	0.65%

9.5 Definition of Inspection Area

V/A : Viewing Area

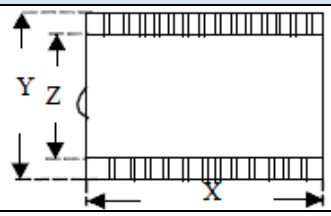
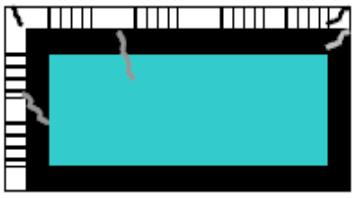
A/A : Active Area



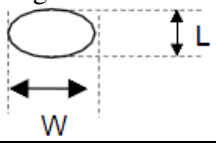
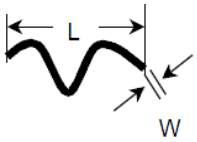
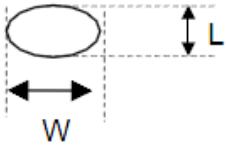
9.6 Items and Criteria

9.6.1 Visual Inspection Criterion in Cosmetic

(1) Glass Defect

Glass Defect			
No	**Defect**	**Criteria**	**Remark**
1	Dimension (Minor)	By engineering diagram	
2	Cracks (Major)	Extensive crack [Reject]	

(2) LCM Appearance Defect

No	Defect	Criteria		Remark
1	Round Type (Minor)	Spec.	Permissible Q'ty	1. Φ =(L+W)/2, L: Length, W: Width 2. Disregard if out of A.A. 
		Φ ≦0.10mm	Disregard	
		0.10mm< Φ ≦0.20mm	3	
		0.20mm< Φ	0	
2	Line Type (Minor)	Spec.	Permissible Q'ty	1. L: Length, W: Width 2. Disregard if out of A.A. 
		W ≦0.03mm	Disregard	
		L≦3.0mm and 0.03mm<W≦0.05mm	2	
		L≦3.0mm and 0.05mmW≦0.10mm	1	
		W>0.10mm or L>3.0mm	0	
3	Polarizer Dent (Minor)	Spec.	Permissible Q'ty	1. Φ =(L+W)/2 , L: Length, W: Width 2. Disregard if out of A.A. 
		Φ ≦0.20mm	Disregard	
		0.20mm< Φ ≦0.30mm	2	
		0.30mm< Φ ≦0.50mm	1	
		0.50mm< Φ	0	

(3) FPC

No	Defect	Criteria	Remark
1	Copper Peeling (Minor)	Copper Peeling [Reject]	

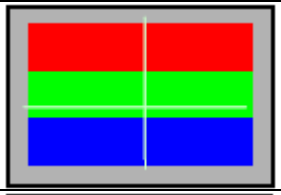
(4) Black Tape

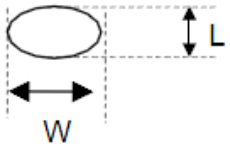
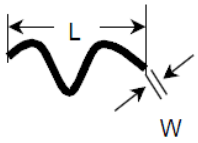
No	Defect	Criteria	Remark
1	Copper Peeling (Minor)	Copper Peeling [Reject]	
2	No Black Tape (Minor)	No Black Tape [Reject]	

(5) Silicon

No	Defect	Criteria	Remark
1	Amount of Silicon (Minor)	ITO exposed [Reject]	

9.6.2 Visual Inspection Criterion in Electrical Display

<table>
<tr><th>No</th><th>Defect</th><th colspan="2">Criteria</th><th>Remark</th></tr>
<tr><td>1</td><td>No Display
(Major)</td><td colspan="2">Not Allowed</td><td>  </td></tr>
<tr><td>2</td><td>Missing Line
(Major)</td><td colspan="2">Not Allowed</td><td>  </td></tr>
<tr><td>3</td><td>Darker or Lighter Line
(Major)</td><td colspan="2">Not Allowed</td><td>  </td></tr>
<tr><td>4</td><td>Weak Line
(Minor)</td><td colspan="2">By Limited Sample</td><td></td></tr>
<tr><td rowspan="3">5</td><td rowspan="3">Bright / Dark Point
(Minor)</td><td>Spec.</td><td>Permissible Q’ty</td><td rowspan="3">1:1sub-pixel: 1R or 1G or 1B
2:Point defect area≧1/2 sub pixel.</td></tr>
<tr><td>Bright Point</td><td>1</td></tr>
<tr><td>Dark Point</td><td>2</td></tr>
</table>

No	Defect	Criteria		Remark
6	Round Type (Minor)	Spec.	Permissible Q'ty	1. Φ =(L+W)/2 , L:Length, W: Width 2. Disregard if out of A.A. 
		Φ ≦0.10mm	Disregard	
		0.10mm<Φ ≦0.20mm	3	
		0.20mm<Φ	0	
7	Line Type (Minor)	Spec.	Permissible Q'ty	1. L: Length, W: Width 2. Disregard if out of A.A. 
		W≦0.03mm	Disregard	
		L≦3.0mm and 0.03mm<W≦0.05mm	2	
		L≦3.0mm and 0.05mm<W≦0.10mm	1	
		W>0.10mm or L>3.0mm	0	
8	Mura (Minor)	By 5% ND filter invisible		

9.6.3 Others

1. Issues that are not defined in this document shall be discussed and agreed with both parties. (customer and supplier)
2. Unless otherwise agreed upon in writing, the criteria shall be applied to both parties. (customer and supplier)