

Version : 7.0

TECHNICAL SPECIFICATION  
MODEL NO : PA035XSE

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Customer's Confirmation


Customer \_\_\_\_\_

Date \_\_\_\_\_

By \_\_\_\_\_

PVI's Confirmation

  
Confirmed By \_\_\_\_\_

  
Prepared By \_\_\_\_\_

## Revision History

| Rev. | Issued Date | Revised Contents  |
|------|-------------|---|
| 0.1  | Feb.3,2004  | NEW   |
| 1.0  | Mar.2,2004  | Updata<br>Page:24 12. Reliability test Vibration Test& ShockTest ok   |
| 1.1  | Oct.6,2004  | Updata<br>Page9:Note 8-5 B/L Lamp voltage kick-off time   |
| 1.2  | Oc.21,2004  | Modify<br>Page 10: 8-5) Timing Characteristics Of Input Signals<br>Page 13: Fig.8-2 Horizontal Start Pixel  |
| 1.3  | Jan.20,2005 | Updata:<br>Page 20: Lamp current about 5mA brightness & lamp life time.   |
| 1.4  | Nov.21.2005 | Modify Page 9 : 8-3) Backlight driving<br>Starting voltage (25°C) Vs(max)=400Vrms chang Vs(max)=440Vrms<br>Starting voltage (0°C) Vs(max)=520Vrms chang Vs(max)=530Vrms |
| 1.5  | Mar,09,2006 | Modify Page 26/27 : Packing   |
| 7.0  | Nov,08,2007 | Modify<br>Page 27: 14.Delete carton and change Packing  |

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## 1. Application

This technical specification applies to 3.5" color TFT-LCD module , PA035XSE  
The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system..

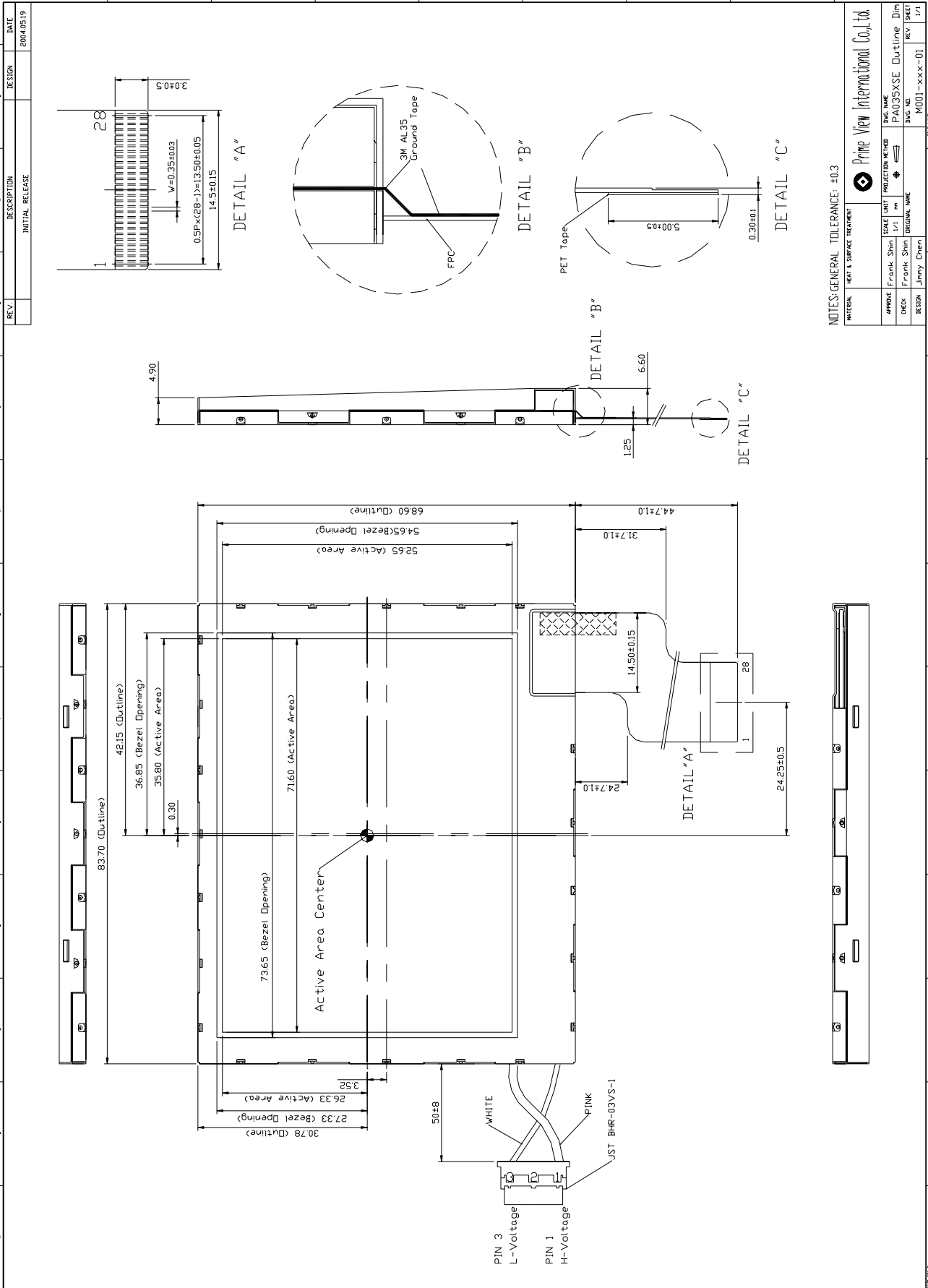
## 2. Features

- . Compatible with NTSC & PAL system
- . Pixel in delta configuration
- . Slim and compact
- . Image Reversion : Up/Down and Left/Right
- . Optimum Viewing Direction : 6 o'clock

## 3. Mechanical Specifications

| <b>Parameter</b>               | <b>Specifications</b>            | <b>Unit</b> |
|--------------------------------|----------------------------------|-------------|
| Screen Size                    | 3.5(diagonal)                    | inch        |
| Display Format                 | 320× (R,G,B) ×234                | dot         |
| Active Area                    | 71.6(H) × 52.65(V)               | mm          |
| Pixel Pitch                    | 0.2237(H) × 0.225(V)             | mm          |
| Pixel Configuration            | Delta                            |             |
| Black-light                    | CCFL,1 tube                      |             |
| Outline Dimension              | 83.7(W) × 68.6(H) × 6.6(D)(typ.) | mm          |
| Surface Treatment              | Anti – Glare                     |             |
| Weight                         | 58±5                             | g           |
| Gray scale inversion direction | 6 o'clock<br>[Note 10-1]         |             |

4. Mechanical Drawing of TFT-LCD Module



NOTES: GENERAL TOLERANCE: ±0.3  
HATCH & SURFACE TREATMENT

|                                    |                                  |
|------------------------------------|----------------------------------|
| PRIME VIEW INTERNATIONAL CO., LTD. |                                  |
| APPROVE                            | SCALE UNIT PROJECTION METHOD DIM |
| FRANK SHIN                         | 1/1 mm 1st                       |
| CHECK                              | FRANK SHIN                       |
| DESIGN                             | JINHY CHEN                       |
| PA035XSE Outline Dim               |                                  |
| DWG. NO. M001-xxx-01               |                                  |
| REV. SHEET 1/1                     |                                  |

**5. Input / Output Terminals**

TFT-LCD Module Connector

FPC Down Connect , 28Pins , Pitch : 0.5 mm

| Pin No | Symbol           | I/O | Description                                | Remark     |
|--------|------------------|-----|--|------------|
| 1      | STH1             | I/O | Start pulse for source driver              | Note 5 – 5 |
| 2      | AV <sub>SS</sub> | I   | Analog GND for source driver               |            |
| 3      | AV <sub>DD</sub> | I   | Analog power input for source driver       | Note 5 – 3 |
| 4      | V <sub>B</sub>   | I   | Video Input B                              | Note 5 – 1 |
| 5      | V <sub>G</sub>   | I   | Video Input G                              |            |
| 6      | V <sub>R</sub>   | I   | Video Input R                              |            |
| 7      | V <sub>SS</sub>  | I   | Digital GND                                |            |
| 8      | V <sub>DD</sub>  | I   | Digital power input                        | Note 5 – 3 |
| 9      | CPH1             | I   | Sampling and shift clock for source driver | Note 5 – 6 |
| 10     | CPH2             | I   | Sampling and shift clock for source driver |            |
| 11     | CPH3             | I   | Sampling and shift clock for source driver |            |
| 12     | STH2             | I/O | Start pulse for source driver              | Note 5 – 5 |
| 13     | Q2H              | I   | Video input rotation control               |            |
| 14     | INH              | I   | Output enable for source driver            |            |
| 15     | R/L              | I   | Left/Right Control for source driver       | Note 5 – 5 |
| 16     | V <sub>COM</sub> | I   | Common electrode voltage                   | Note 5 – 1 |
| 17     | V <sub>COM</sub> | I   | Common electrode voltage                   |            |
| 18     | XOE              | I   | Output enable for gate driver              |            |
| 19     | CPV              | I   | Clock input for gate driver                |            |
| 20     | U/D              | I   | Up/Down Control for gate driver            | Note 5 – 5 |
| 21     | DIO2             | I/O | Vertical start pulse                       |            |
| 22     | DIO1             | I/O | Vertical start pulse                       |            |
| 23     | V <sub>GL</sub>  | I   | Gate off voltage(alternative every 1-H)    | Note 5 – 1 |
| 24     | V <sub>EE</sub>  | I   | Gate driver negative voltage               | Note 5 – 2 |
| 25     | V <sub>SS</sub>  | I   | GND  |            |
| 26     | V <sub>CC</sub>  | I   | Logic power for gate driver                | Note 5 – 3 |
| 27     | V <sub>GH</sub>  | I   | Gate on voltage                            | Note 5 – 4 |
| 28     | GND              | -   | B/L case GND                               |            |

Note 5 – 1 :  $V_{COM(TYP.)} = 6.0V_{PP}$ .

**Phase of the video signal input and  $V_{COM}$**

The relation between these values could refer to 8-1 Operating condition.

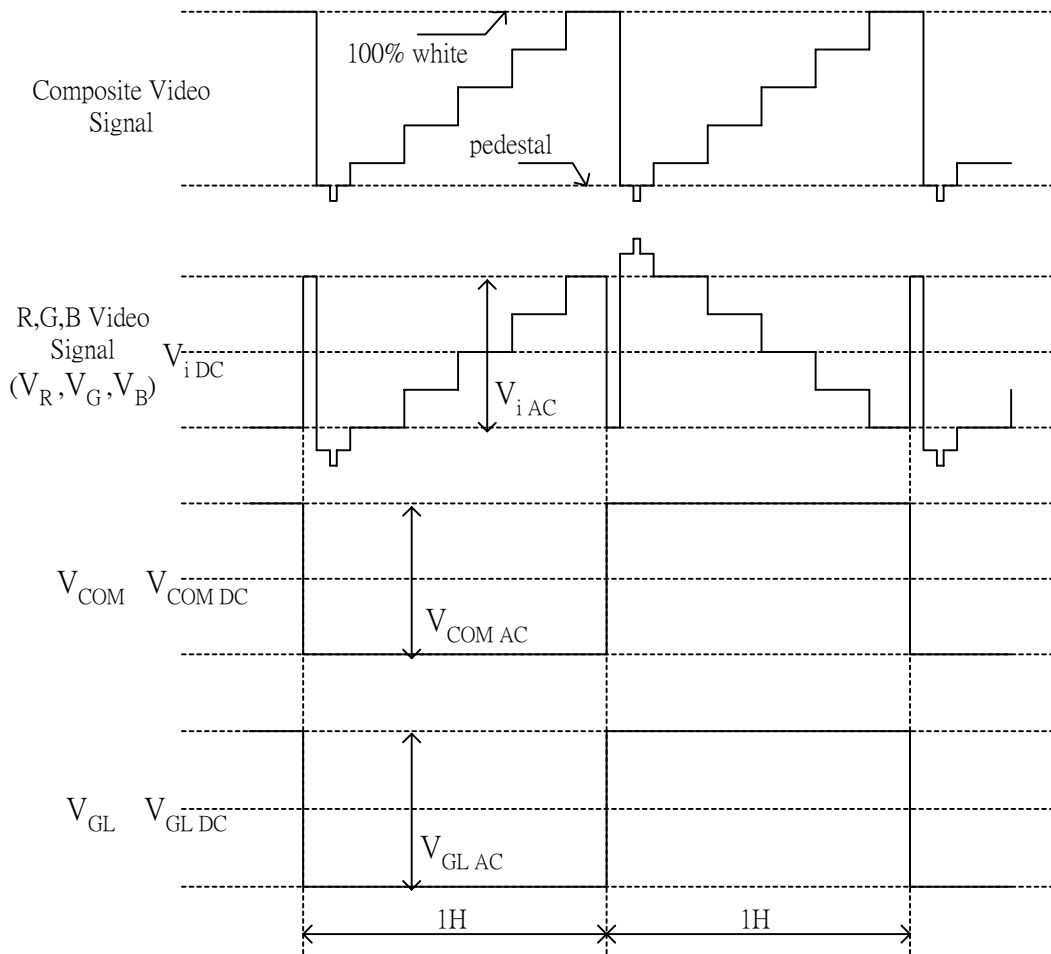


Fig.1

**Liquid crystal transmission of the video signal input,  $V_{COM}$  and timing**

|                            | $V_{COM}$ |         |
|----------------------------|-----------|---------|
|                            | H Level   | L Level |
| Video Signal Input Maximum | Black     | White   |
| Video Signal Input Minimum | White     | Black   |

White : maximum transmission / Black : minimum transmission

Note 5 – 2 :  $V_{EE(TYP.)} = -15V$

Note 5 – 3 :  $V_{DD}, V_{CC(TYP.)} = +3.3V$  ,  $AV_{DD(TYP.)} = +5.0V$

Note 5 – 4 :  $V_{GH(TYP.)} = +17V$

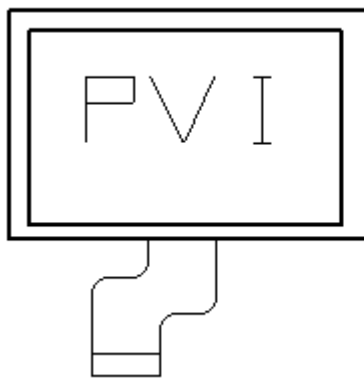
Note 5 – 5 : STH1, STH2 and R/L mode

| R/L                    | STH1   | STH2   | Remark        |
|------------------------|--------|--------|---------------|
| High(V <sub>DD</sub> ) | Input  | Output | Left to Right |
| Low(0 Volt.)           | Output | Input  | Right to Left |

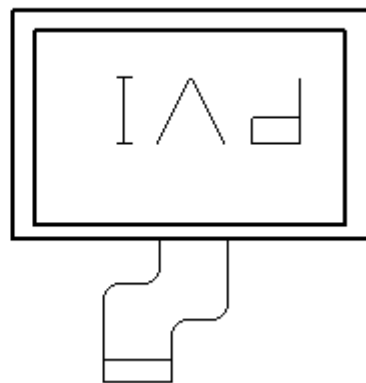
DIO1,DIO2,and U/D mode

| U/D                    | DIO1   | DIO2   | Remark     |
|------------------------|--------|--------|------------|
| High(V <sub>CC</sub> ) | Input  | Output | Down to Up |
| Low(0 Volt.)           | Output | Input  | Up to Down |

U/D(PIN 20)=Low R/L(PIN 15)=High



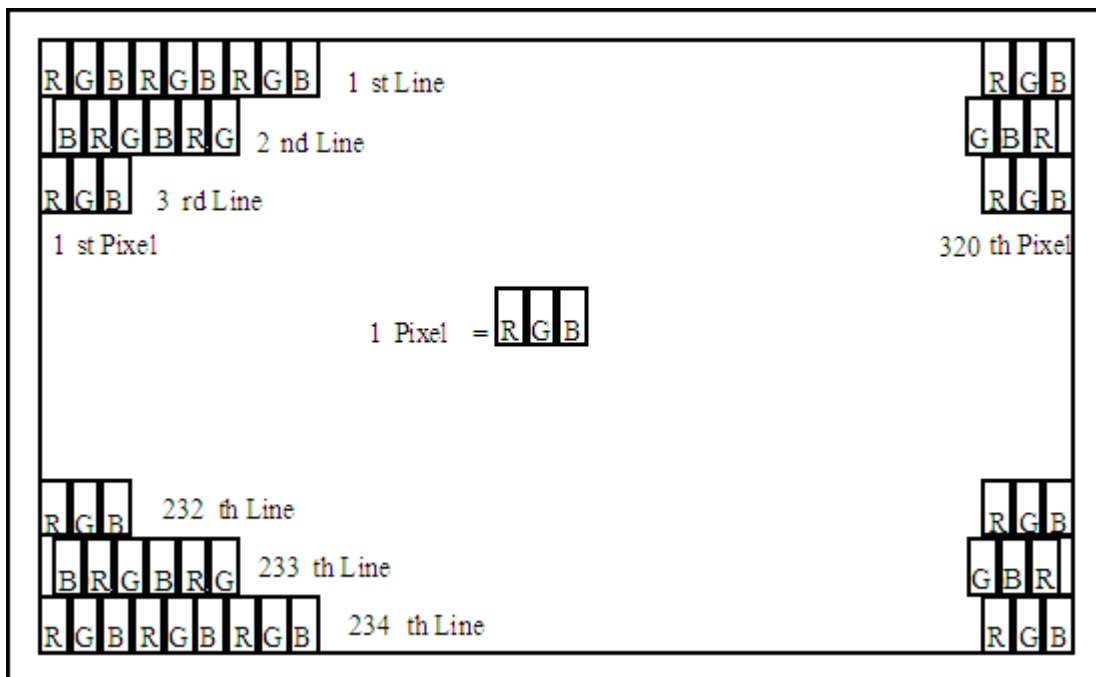
U/D(PIN 20)=High R/L(PIN 15)=Low



Note 5 – 6: The CPH1 reference Fig.8-1 Sampling clock timing

CPH2 and CPH3 connect GND.

6. Pixel Arrangement





**7. Absolute Maximum Ratings :**

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

$$\text{GND} = 0\text{V} \cdot \text{Ta} = 25^{\circ}\text{C}$$

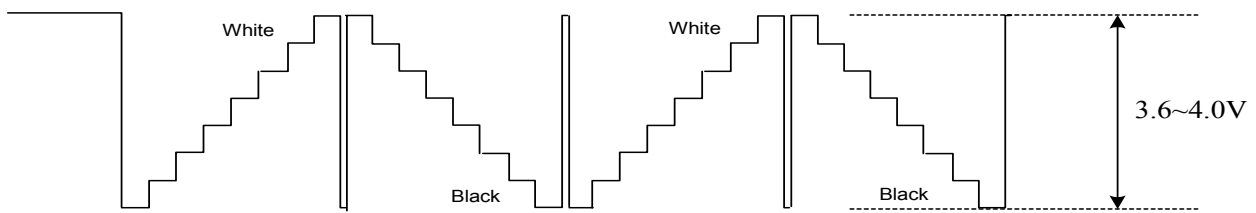
| Parameter                        | Symbol           | MIN. | MAX. | Unit | Remark |
|----------------------------------|------------------|------|------|------|--------|
| Supply Voltage For Source Driver | $AV_{DD}$        | -0.3 | +7.0 | V    |        |
|                                  | $V_{DD}$         | -0.3 | +7.0 | V    |        |
| Supply Voltage For Gate Driver   | H Level $V_{GH}$ | -0.3 | +45  | V    |        |
|                                  | L Level $V_{GL}$ | -23  | +0.3 | V    |        |
|                                  | $V_{GH}-V_{GL}$  | +15  | +40  | V    |        |

**8. Electrical Characteristics**
**8-1) Operating Condition**

| Parameter                                | Symbol           | MIN.          | Typ.  | MAX.          | Unit      | Remark                             |
|--|------------------|---------------|-------|---------------|-----------|------------------------------------|
| Supply Voltage For Source Driver         | Analog $AV_{DD}$ | +4.5          | +5.0  | +5.5          | V         | Depend on T/C signal voltage       |
|  | Logic $V_{DD}$   | +3.0          | +3.3  | +3.6          | V         |                                    |
|  |                  | +4.5          | +5.0  | +5.5          | V         |                                    |
| Supply Voltage For Gate Driver           | $V_{GH}$         | +15.0         | +17.0 | +19.0         | V         |                                    |
|  | $V_{EE}$         | -15.5         | -15.0 | -14.5         | V         |                                    |
|  | $V_{GL\ DC}$     | -12.5         | -11.0 | -9.5          | V         | DC Component of $V_{GL}$           |
|  | $V_{GL\ AC}$     | -             | +6.0  | -             | $V_{P-P}$ | AC Component of $V_{GL}$           |
|  | Logic $V_{CC}$   | +3.0          | +3.3  | +3.6          | V         | Depend on T/C signal voltage       |
| +4.5                                     |                  | +5.0          | +5.5  | V             |           |                                    |
| Analog Signal input Level (VR , VG , VB) | $V_{IAC}$        | -             | +3.6  | +4.0          | V         | Note 8-2                           |
|  | $V_{IDC}$        | -             | +2.5  | -             | V         |                                    |
| Digital input voltage                    | H level $V_{IH}$ | +0.7 $V_{DD}$ | -     | -             | V         |                                    |
|  | L level $V_{IL}$ | -             | -     | +0.3 $V_{DD}$ | V         |                                    |
| $V_{COM}$                                | $V_{COM\ AC}$    | -             | +6.0  | -             | $V_{P-P}$ | AC Component of $V_{COM}$          |
|  | $V_{COM\ DC}$    | -             | +0.96 | -             | V         | DC Component of $V_{COM}$ Note 8-1 |

Note 8-1 : PVI strongly suggests that the  $V_{COM\ DC}$  level shall be adjustable ,and the adjustable level range is  $0.96V \pm 1V$ , every module's  $V_{COM\ DC}$  level shall be carefully adjusted to show a best image performance.

Note 8-2: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



### 8-2) Current Consumption (GND=0V)

Ta= 25 °C

| Parameter          | Symbol          | Condition              | Min. | Typ.  | Max.  | Unit | Remark                         |
|--------------------|-----------------|------------------------|------|-------|-------|------|--------------------------------|
| Current for Driver | I <sub>GH</sub> | V <sub>GH</sub> =+17V  | -    | 0.055 | 0.083 | mA   |                                |
|                    | I <sub>GL</sub> | V <sub>GL</sub> =-12V  | -    | 0.067 | 0.087 | mA   | V <sub>GL</sub> center voltage |
|                    | I <sub>CC</sub> | V <sub>CC</sub> =+3.3V | -    | 0.441 | 0.563 | mA   |                                |
|                    | A <sub>DD</sub> | V <sub>DD</sub> =+3.3V | -    | 1.2   | 3     | mA   |                                |
|                    | I <sub>EE</sub> | V <sub>EE</sub> =-15V  | -    | 0.441 | 0.6   | mA   |                                |
|                    | I <sub>DD</sub> | AV <sub>DD</sub> =+5V  | -    | 7     | 10    | mA   |                                |

### 8-3) Backlight driving & Power Consumption

| Pin No | Symbol | Description                       | Remark   |
|--------|--------|-----------------------------------|----------|
| 1      | VL1    | Input terminal (Hi voltage side)  |          |
| 2      | VL3    | Input terminal (Low voltage side) | Note 8-3 |

Note 8-3 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

Ta= 25 °C

| Parameter                                      | Symbol         | Min. | Typ. | Max. | Unit             | Remark   |
|--|----------------|------|------|------|------------------|----------|
| Lamp voltage                                   | V <sub>L</sub> | -    | 265  | -    | V <sub>rms</sub> |          |
| Lamp current                                   | I <sub>L</sub> | 2    | 3    | 5    | mA               | Note 8-4 |
| Lamp frequency                                 | P <sub>L</sub> | 25   | 35   | 65   | KHz              | Note 8-5 |
| Starting voltage (25°C)<br>(Reference Voltage) | V <sub>S</sub> | -    | -    | 440  | V <sub>rms</sub> | Note 8-6 |
| Starting voltage (0°C)<br>(Reference Voltage)  | V <sub>S</sub> | -    | -    | 530  | V <sub>rms</sub> | Note 8-6 |

Note 8-4 : In order to satisfy the quality of B/L, no matter use what kind of inverter, the output lamp current must be between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-5: The waveform of lamp driving voltage should be as close to a perfect SIN wave as possible.

Note 8-6 : The "Max of starting voltage" means the minimum voltage of inverter to turn on the CCFL. And it should be applied to the lamp for more than 1 second to start up. Otherwise the lamp may not be turned on.

## Power Consumption

Ta= 25 °C

| Parameter                        | Symbol | Conditions | TYP. | Unit | Remark   |
|----------------------------------|--------|------------|------|------|----------|
| LCD Panel Power Consumption      |        |            | 50   | mW   |          |
| Backlight Lamp Power Consumption |        |            | 0.65 | W    | Note 8-7 |
| Total Power Consumption          |        |            | 0.69 | W    |          |

 Note 8-7 : Backlight lamp power consumption is calculated by  $I_L \times V_L$ .

## 8-4) Input / Output Connector

6. Backlight Connector  
 JST BHR-03VS-1,  
 Pin No. : 3 ,  
 Pitch : 4 mm

## 8-5) Timing Characteristics Of Input Signals

| Characteristics                   | Symbol            | Min.  | Typ.   | Max.  | Unit | Remark          |
|-----------------------------------|-------------------|-------|--------|-------|------|-----------------|
| 1Field Scanning Period            | t1V               | -     | 262.5  | -     | H    |                 |
| 1Line Scanning Period             | t1H               | -     | 63.5   | -     | μs   |                 |
| Source Driver Operating Frequency | fhc               | 4     | 6.4    | 8     | MHz  |                 |
| Signal Sampling Pulse Width       | tchw              | 125   | 156.25 | 250   | ns   |                 |
| Signal Sampling Pulse Delay       | tchd              | 47.65 | 52     | 58.25 | ns   | tchd 12,23      |
| Signal Sampling Pulse Width(H)    | tchwh             | 71.45 | 78.12  | 87.35 | ns   |                 |
| Signal Sampling Pulse Delay(L)    | tchwl             | 71.45 | 78.12  | 87.35 | ns   |                 |
| Source Start Signal Pulse Width   | tshw              | 45    | 156.25 | 315   | ns   | *tshset=tshhld  |
| Source Start Signal Setup Time    | tshset            | 20    | 78.12  | -     | ns   |                 |
| Source Start Signal Hold Time     | tshhld            | 20    | 78.12  | -     | ns   |                 |
| Source Output Enable Pulse Width  | tohw              | 1.0   | 2.0    | -     | μs   |                 |
| Source Start Signal Rising Time   | tss               | -     | 9.8    | -     | μs   |                 |
| Video Input Signal Start Point    | tvS               | -     | 10.0   | -     | μs   |                 |
| Phase Difference Between XOE&CPV  | toc               | 1.5   | 2.3    | -     | μs   |                 |
| Gate Clock Period                 | tevw              | 10    | 63.5   | -     | μs   |                 |
| Gate Clock Pulse Width(H)         | tevwh             | 10    | 31.7   | 48    | μs   |                 |
| Gate Clock Pulse Width(L)         | tevwl             | 10    | 31.7   | 48    | μs   |                 |
| Gate Start Signal Pulse Width     | tsvw              | 5     | 63.5   | 126** | μs   | **tsvset=tsvhld |
| Gate Start Signal Setup Time      | tsvset            | 5     | 53.2   | -     | μs   |                 |
| Gate Start Signal Hold Time       | tsvhld            | 5     | 10.3   | -     | μs   |                 |
| Phase Difference Between INH&STH  | tosp              | -     | 4      | -     | μs   |                 |
| Phase Difference Between SYNC&INH | tohs              | -     | 1.4    | -     | μs   |                 |
| Gate Output Enable Pulse Width    | toev              | -     | 2.5    | -     | μs   |                 |
| V <sub>COM</sub> Delay Time       | t <sub>DCOM</sub> | -     | -      | 3     | μs   |                 |
| RGB Delay Time                    | t <sub>DRGB</sub> | -     | -      | 2     | μs   |                 |
| Vertical Display Start            | tSV               | -     | 3      | -     | tH   |                 |

8 – 6 ) Signal Timing Waveforms

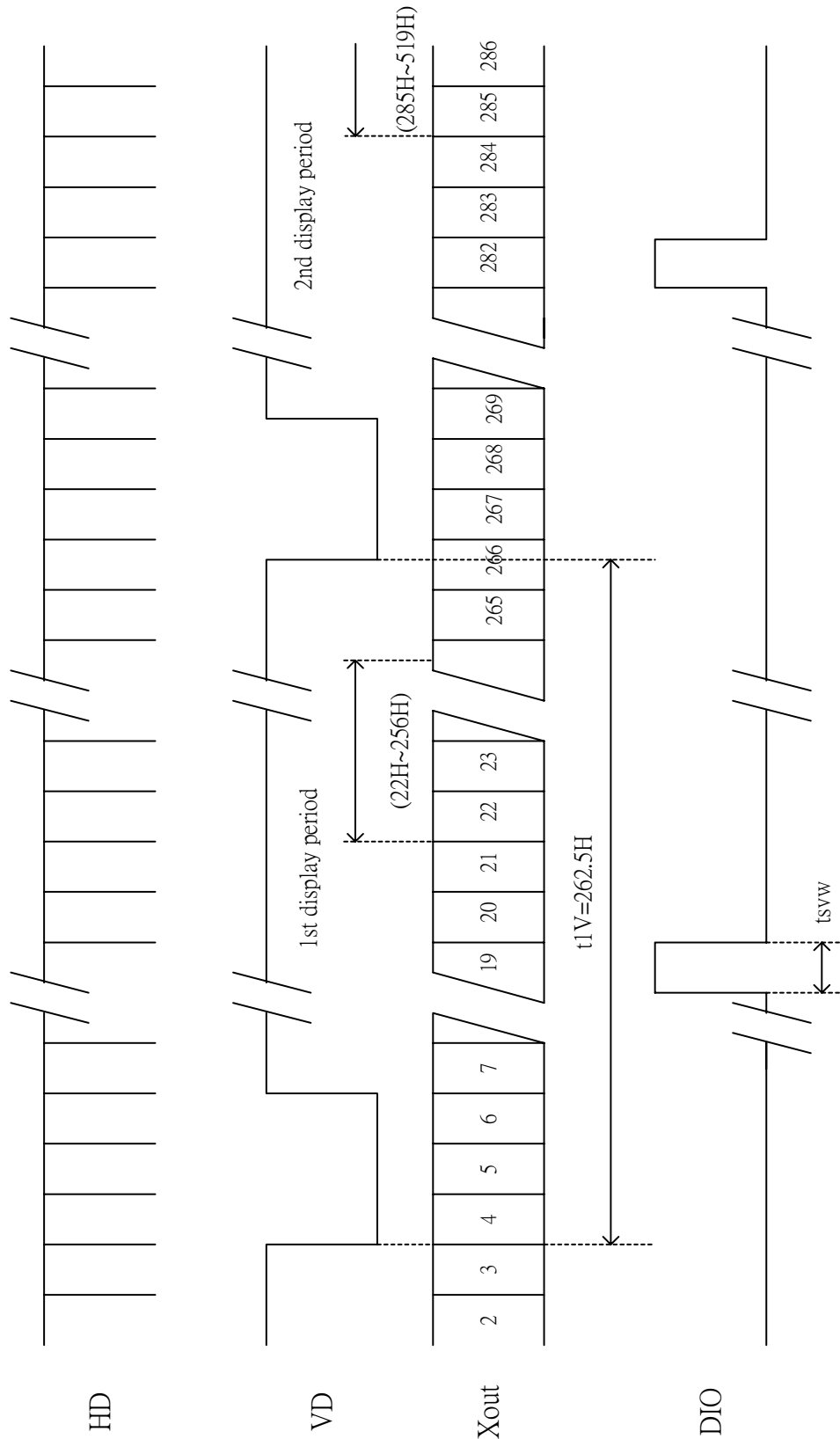
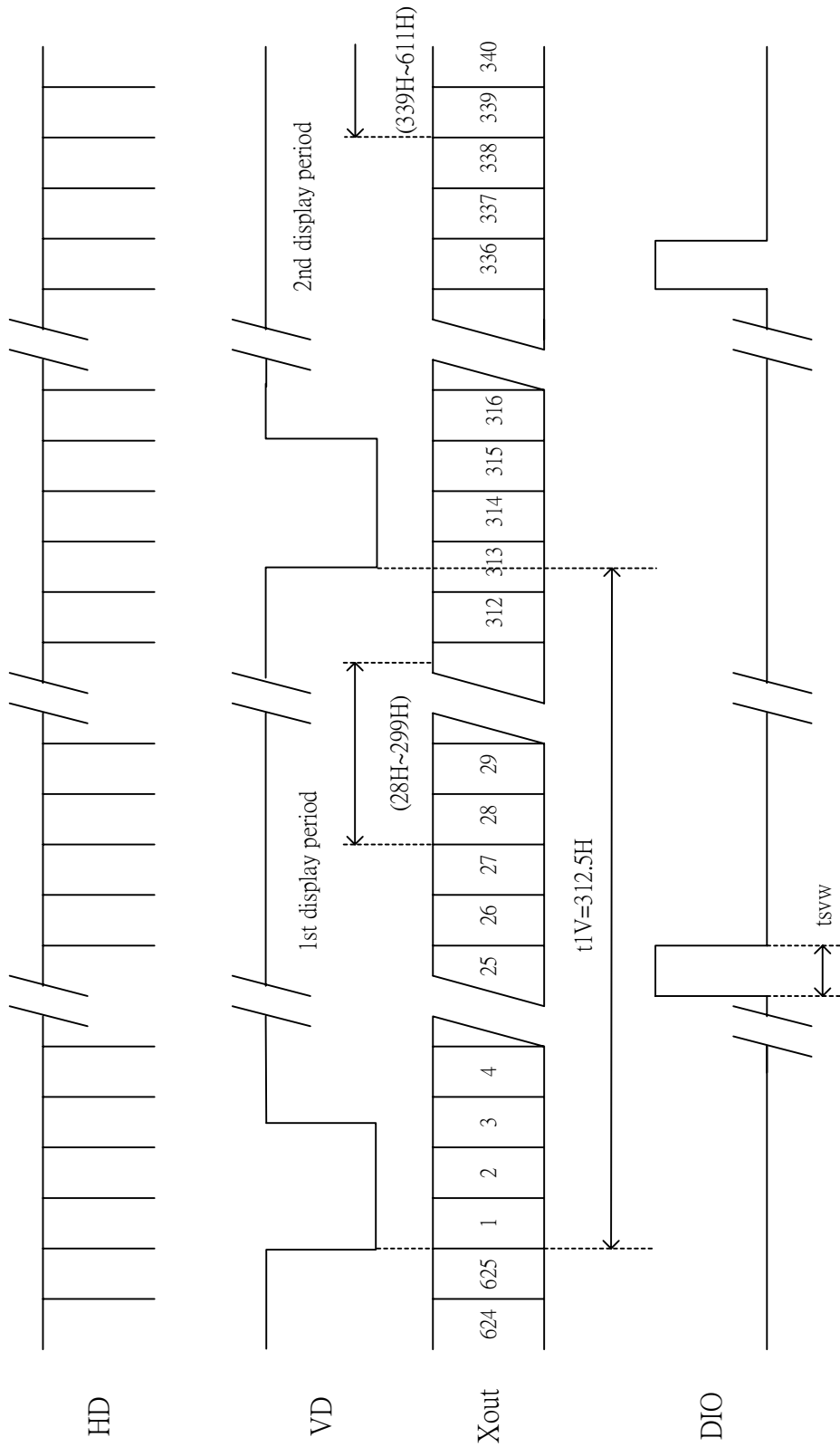


Fig. 8-1 Vertical Start Line for NTSC



\*\* odd field : Scan lines  $14n+6$   $14n+12$  ( $n = 2, 3, 4..$ ) are not displayed.  
 even field : Scan lines  $14n+12$   $14n+20$  ( $n = 2, 3, 4..$ ) are not displayed.

Fig. 8-1 Vertical Start Line for PAL

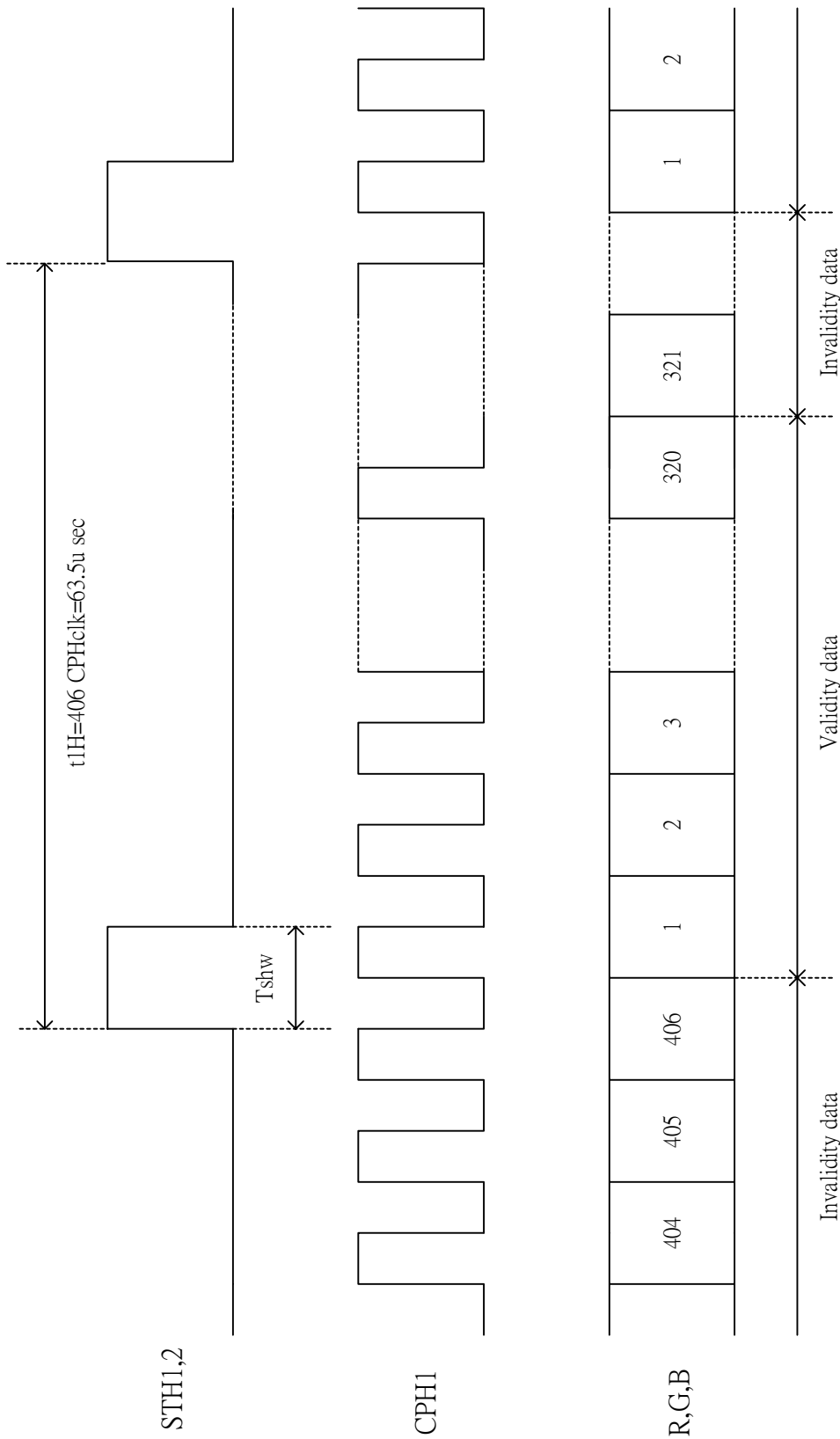


Fig. 8-2 Horizontal Start Pixel

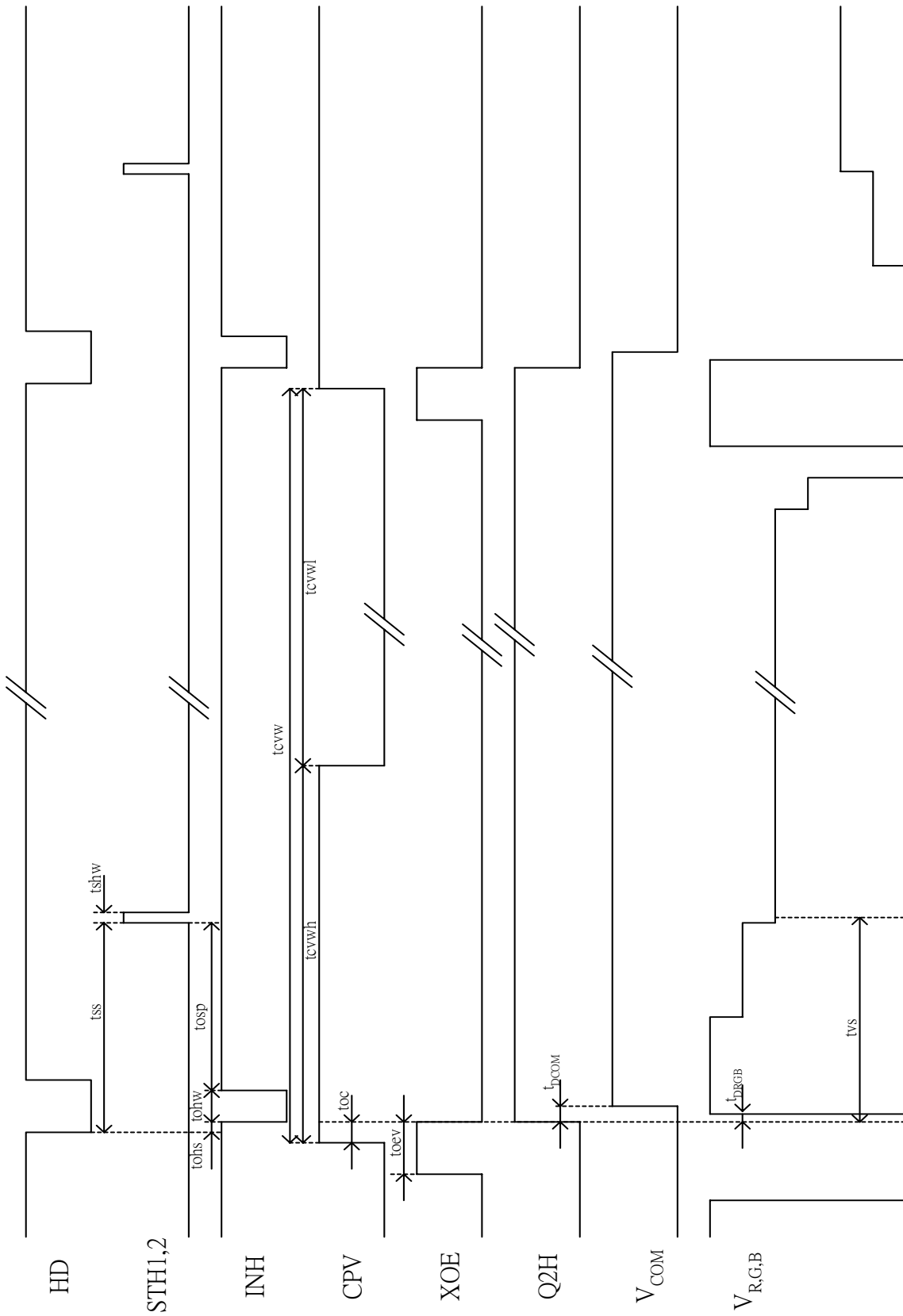


Fig. 8-3 Detail Horizontal Timing

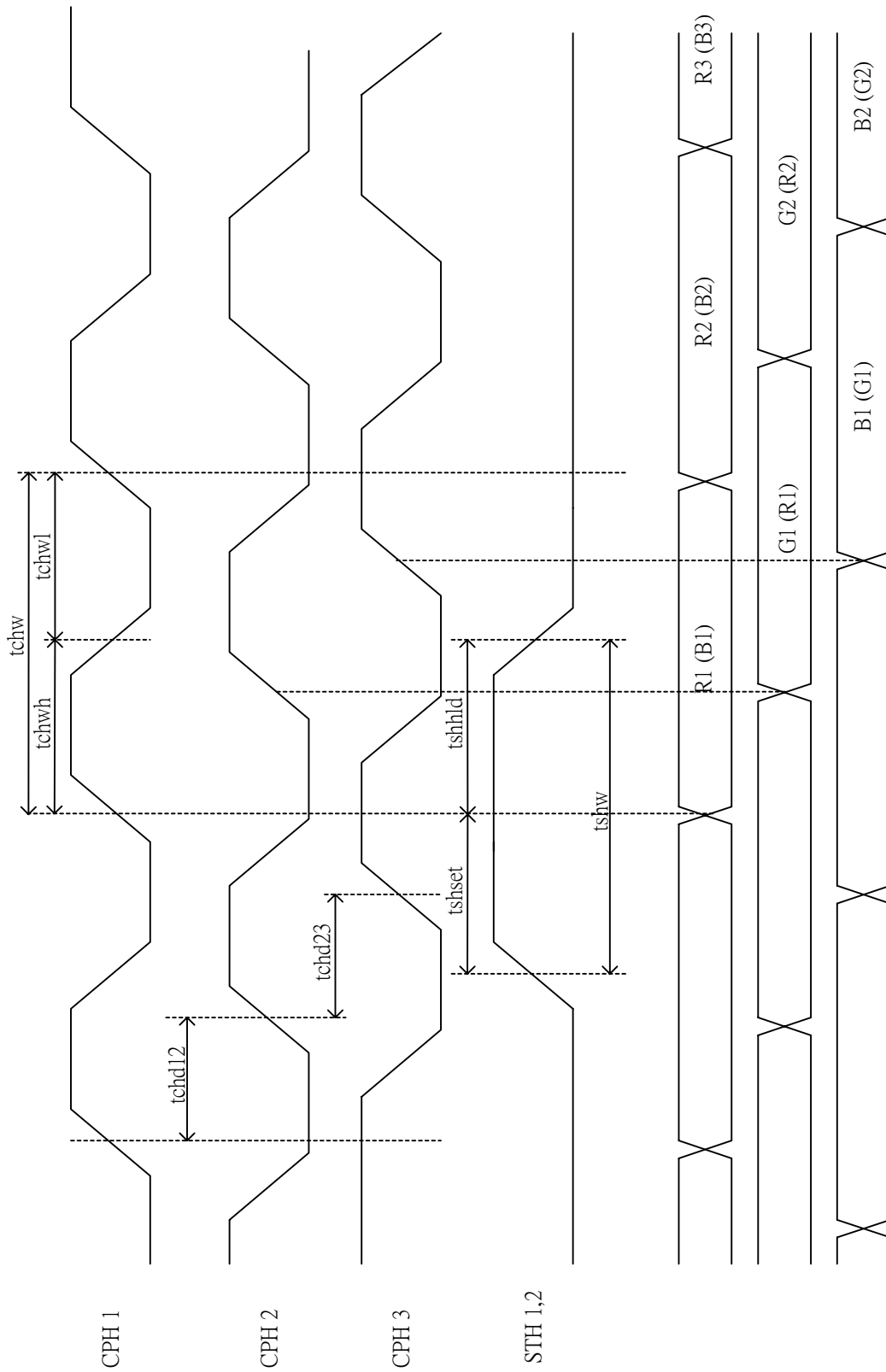


Fig. 8-4 Sampling Clock Timing



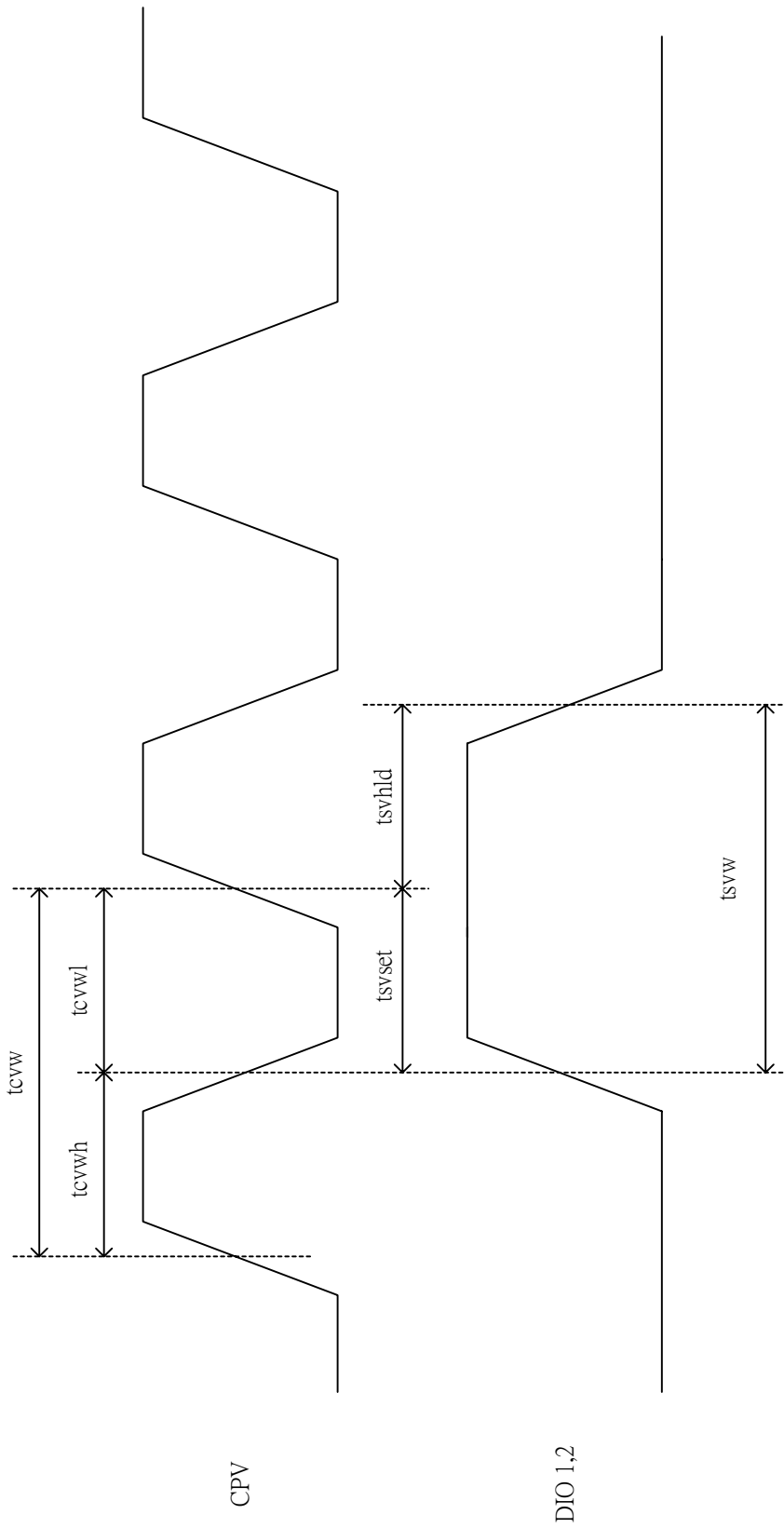


Fig. 8-5 Vertical Shift Clock Timing

Vertical timing (From up to down)

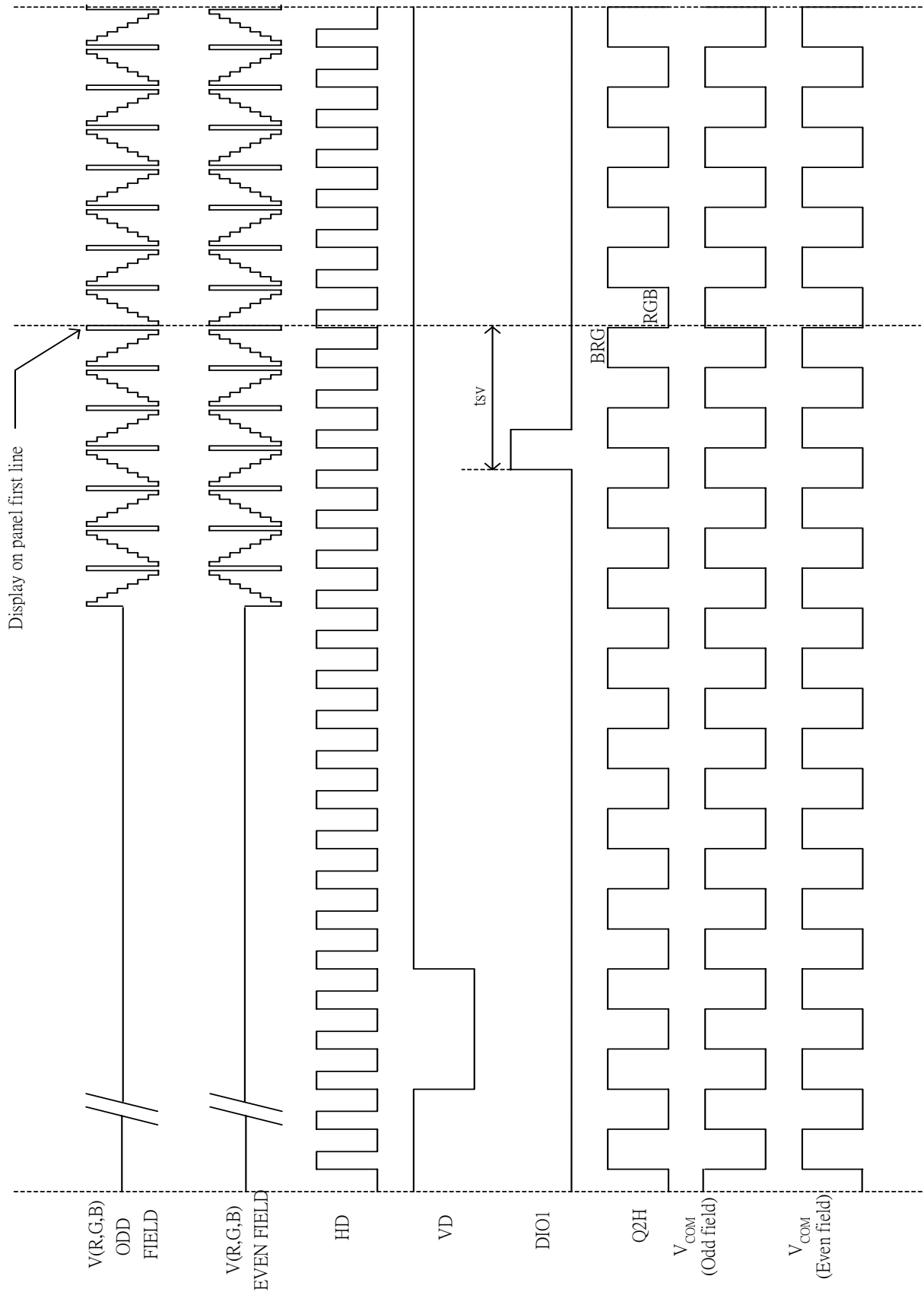


Fig. 8-6(a) Vertical Timing (From Up to Down)

Vertical timing (From down to up)

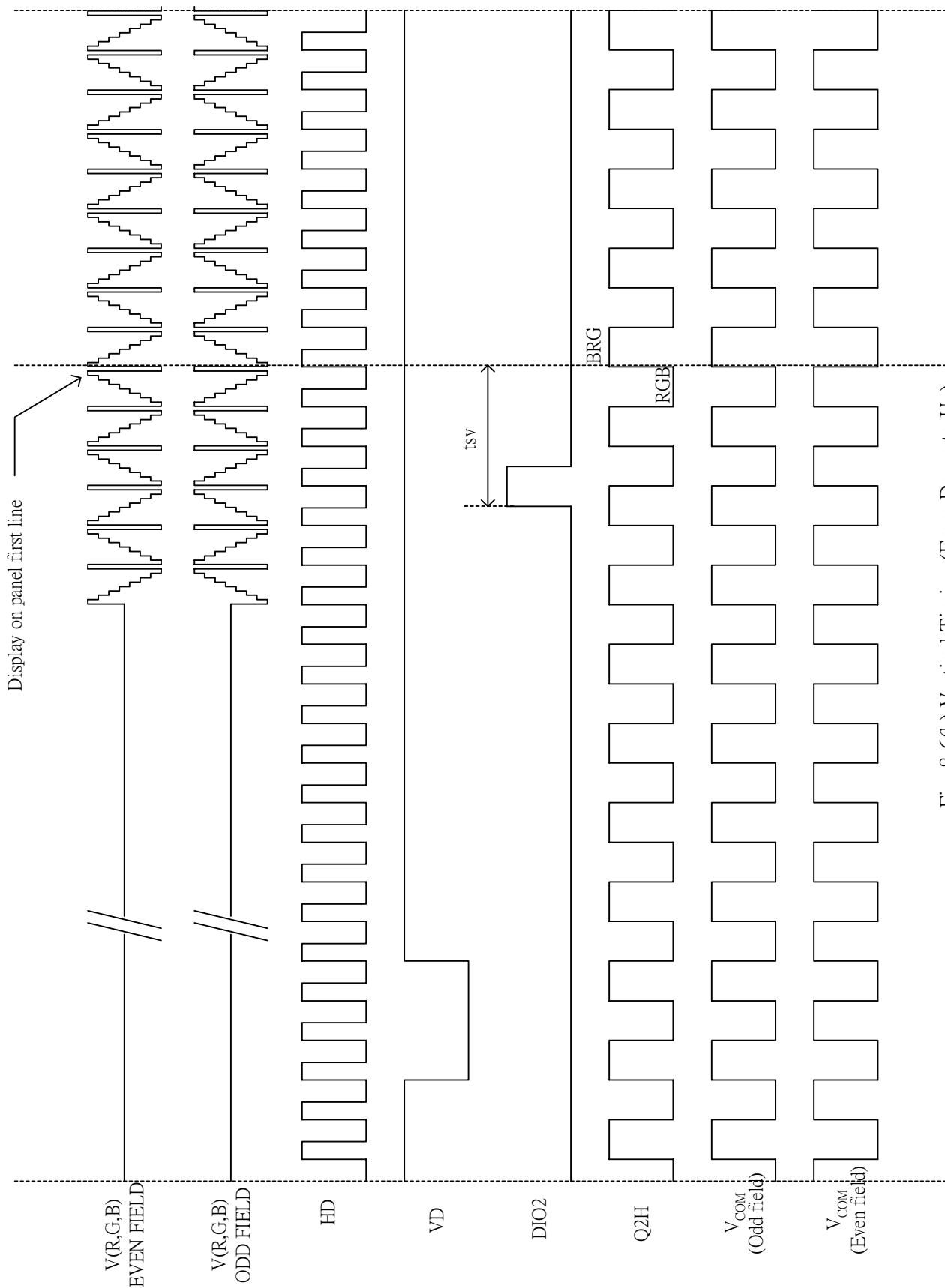
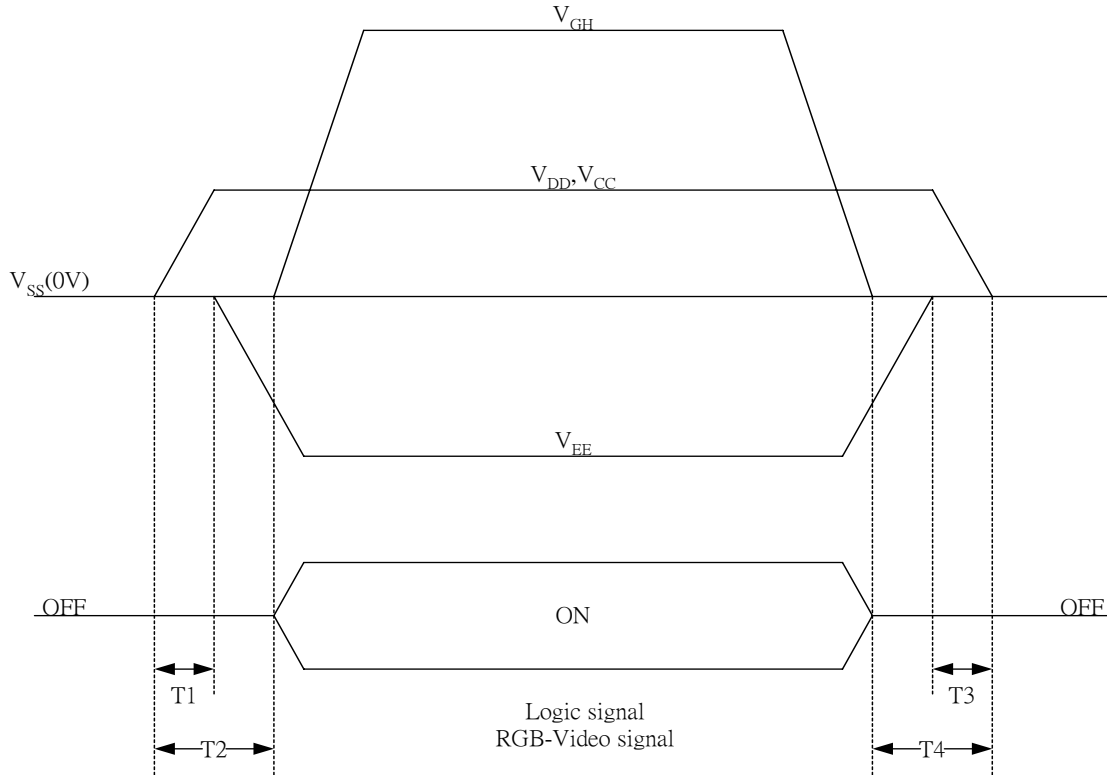


Fig. 8-6(b) Vertical Timing (From Down to Up)

9. Power On Sequence

The Power on Sequence only effect by  $V_{CC}$ ,  $V_{SS}$ ,  $V_{DD}$ ,  $V_{EE}$  and  $V_{GH}$ , the others do not care.



- 1)  $10\text{ms} \leq T1 < T2$
- 2)  $0\text{ms} < T3 \leq T4 \leq 10\text{ms}$

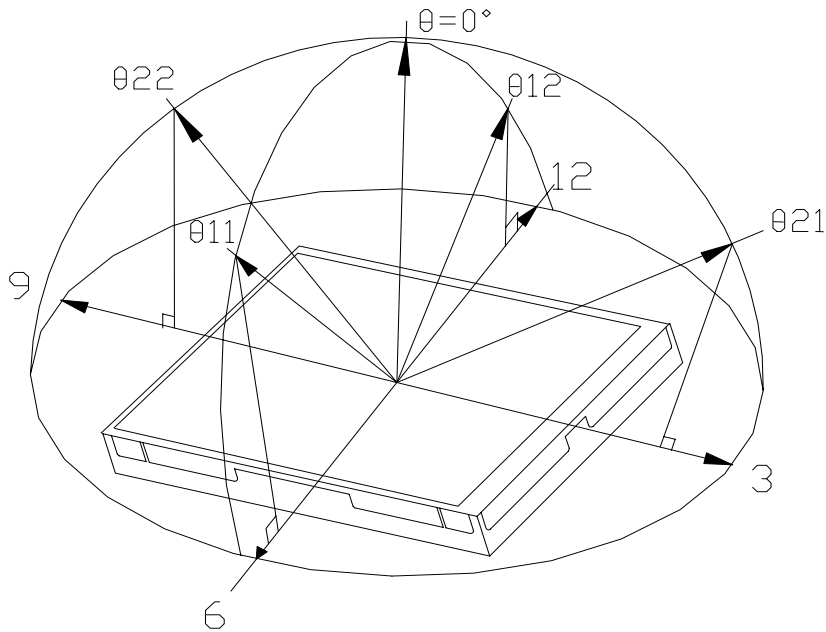
10. Optical Characteristics

10-1) Specification:

$T_a = 25^\circ\text{C}$

| Parameter          |            | Symbol                 | Condition                  | MIN.     | TYP.     | MAX.  | Unit            | Remarks   |
|--------------------|------------|------------------------|----------------------------|----------|----------|-------|-----------------|-----------|
| Viewing Angle      | Horizontal | $\theta 21, \theta 22$ | $CR \geq 10$               | $\pm 45$ | $\pm 50$ | -     | deg             | Note 10-1 |
|                    | Vertical   | $\theta 12$            |                            | 10       | 15       | -     | deg             |           |
|                    |            | $\theta 11$            |                            | 30       | 35       | -     | deg             |           |
| Contrast Ratio     |            | CR                     | At optimized Viewing angle | 200      | 350      | -     |                 | Note 10-2 |
| Response time      | Rise       | Tr                     | $\theta = 0^\circ$         | -        | 15       | 30    | ms              | Note 10-4 |
|                    | Fall       | Tf                     |                            | -        | 25       | 50    | ms              |           |
| Uniformity         |            | U                      |                            | 65       | 70       | -     | %               | Note 10-6 |
| Brightness         |            | L                      | 3mA                        | 200      | 250      | -     | $\text{cd/m}^2$ | Note 10-3 |
|                    |            |                        | 5mA                        | 300      | 350      | -     |                 |           |
| White Chromaticity |            | x                      | $\theta = 0^\circ$         | 0.280    | 0.310    | 0.340 |                 |           |
|                    |            | y                      | $\theta = 0^\circ$         | 0.310    | 0.340    | 0.370 |                 |           |
| Lamp Life Time     |            |                        | $+25^\circ\text{C}$        | -        | 30000    | -     | hrs             | Note 10-5 |

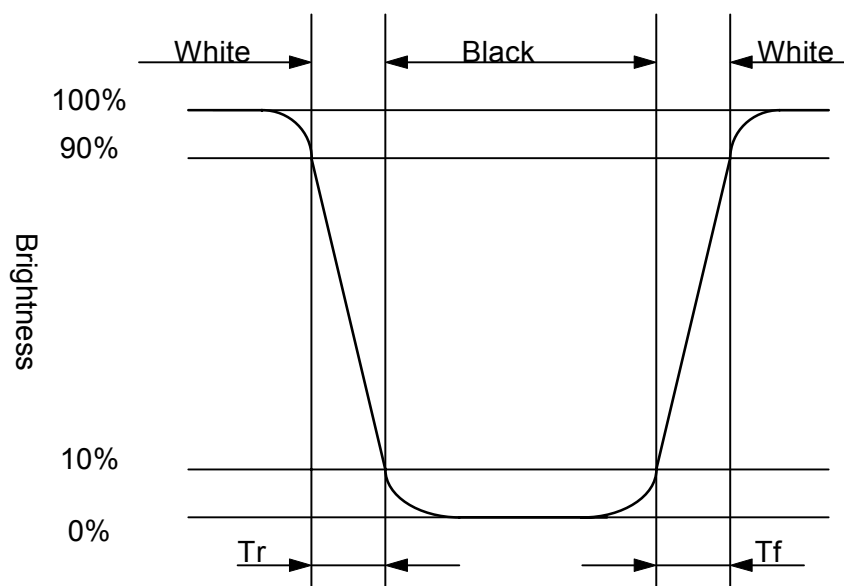
Note 10-1 : The definitions of viewing angles



Note 10-2 :  $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$   
 (Testing configuration see 10-2 )  
 Contrast Ratio is measured in optimum common electrode voltage.

- Note 10-3 :
1. Topcon BM-7(fast) luminance meter 1° field of view is used in the testing (after 20~30 minutes operation).
  2. Lamp Current 3mA & 5mA
  3. Inverter model : TDK-347.

Note 10-4 : The definition of response time :



Note 10-5: Lamp life time 3mA about 30000hrs ; 5mA about 20000hrs

Note 10-6: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

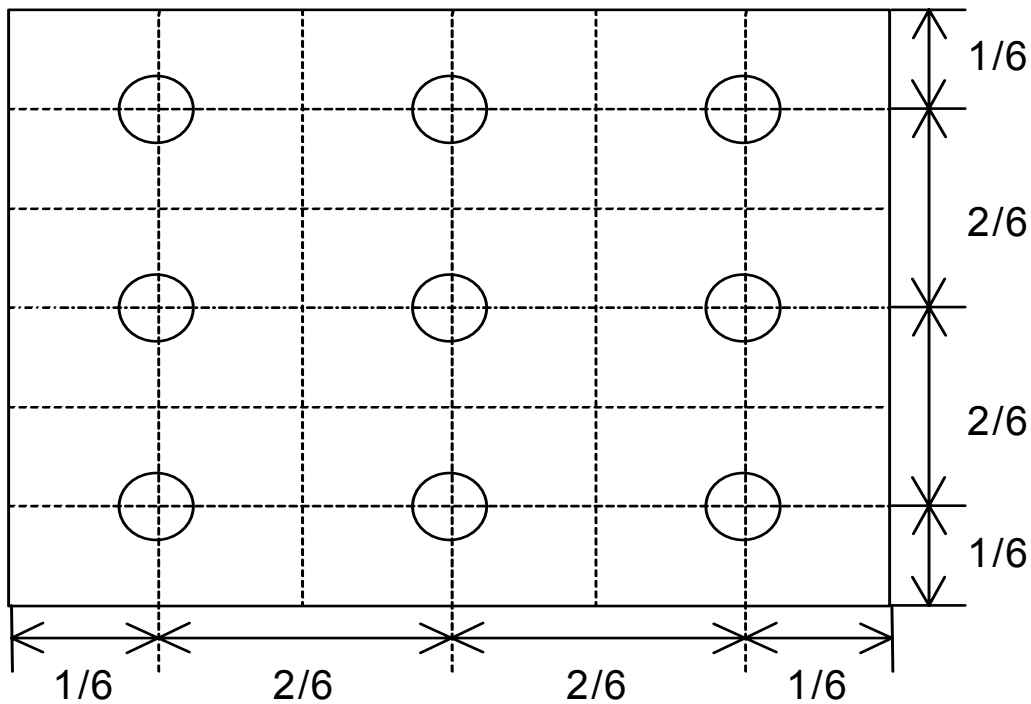
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

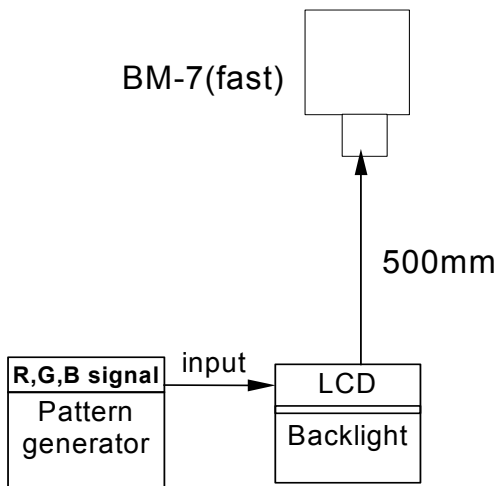
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

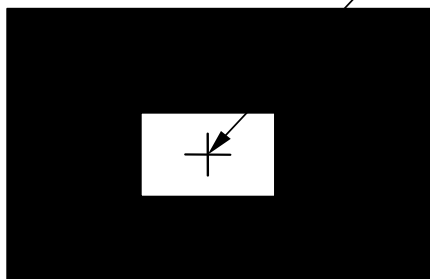


10-2) Testing configuration

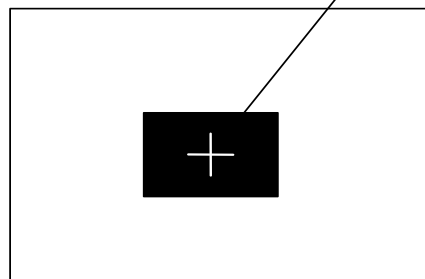


Caution: 1. Environmental illumination  $\leq 1$  lux  
 2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display Testing Point
- Testing Point

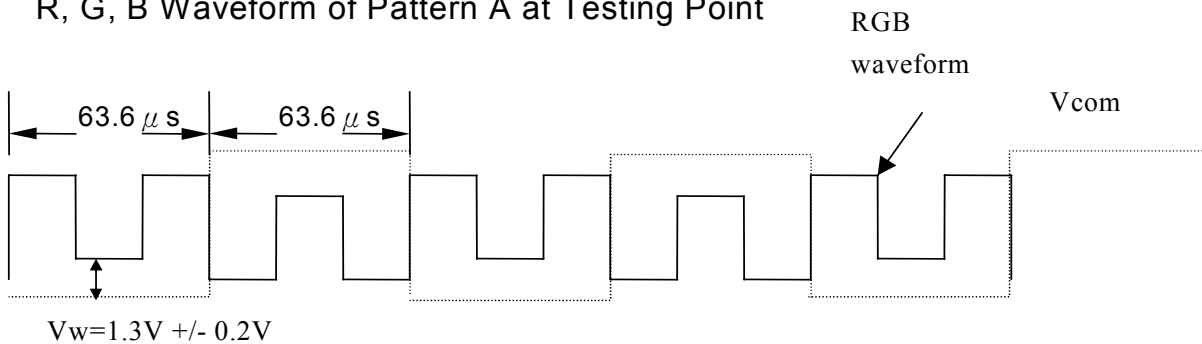


Pattern A

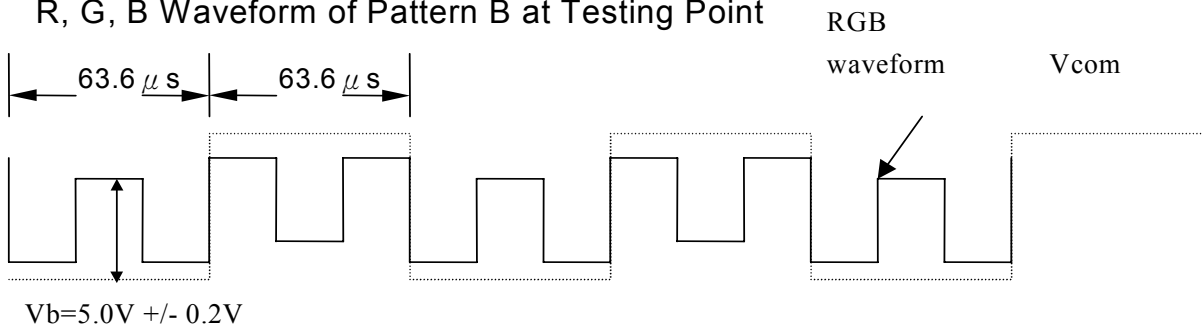


Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



## 11. Handling Cautions

### 11-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
  - 1.The noise from the backlight unit will increase.
  - 2.The output from inverter circuit will be unstable.
  - 3.In some cases a part of module will heat.
  6. Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
  6. Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

### 11-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

### 11-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

### 11-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.



## 12. Reliability Test

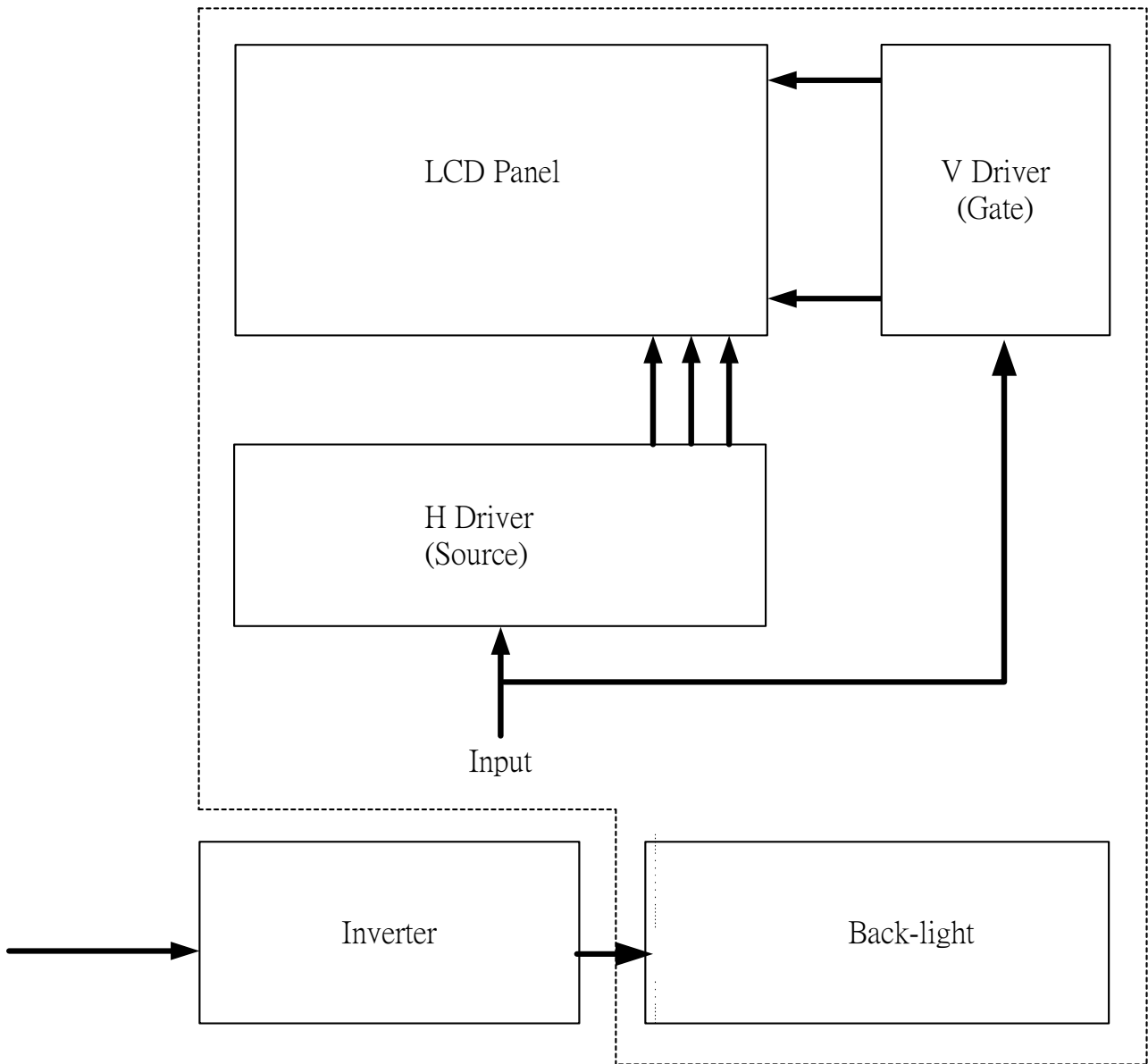
| No | Test Item                                       | Test Condition  |
|----|---|---|
| 1  | High Temperature Storage Test                   | Ta = +70°C, 240 hrs   |
| 2  | Low Temperature Storage Test                    | Ta = -20°C, 240 hrs   |
| 3  | High Temperature Operation Test                 | Ta = +60°C, 240 hrs   |
| 4  | Low Temperature Operation Test                  | Ta = 0°C, 240 hrs   |
| 5  | High Temperature & High Humidity Operation Test | Ta = +60°C, 90%RH, 240 hrs  |
| 6  | Thermal Cycling Test<br>(non-operating)         | -25°C → +70°C, 200 Cycles<br>30 min 30 min  |
| 7  | Vibration Test<br>(non-operating)               | Frequency : 10 ~ 55 Hz<br>Amplitude : 1.5 mm<br>Sweep time: 11 mins<br>Test Period : 6 Cycles for each direction of X, Y, Z |
| 8  | Shock Test<br>(non-operating)                   | 100G, 6ms<br>Direction : ±X, ±Y, ±Z<br>Cycle : 3 times  |
| 9  | Electrostatic Discharge Test<br>(non-operating) | 200pF, 0Ω<br>±200V<br>1 time / each terminal  |

Ta: ambient temperature

[Criteria]

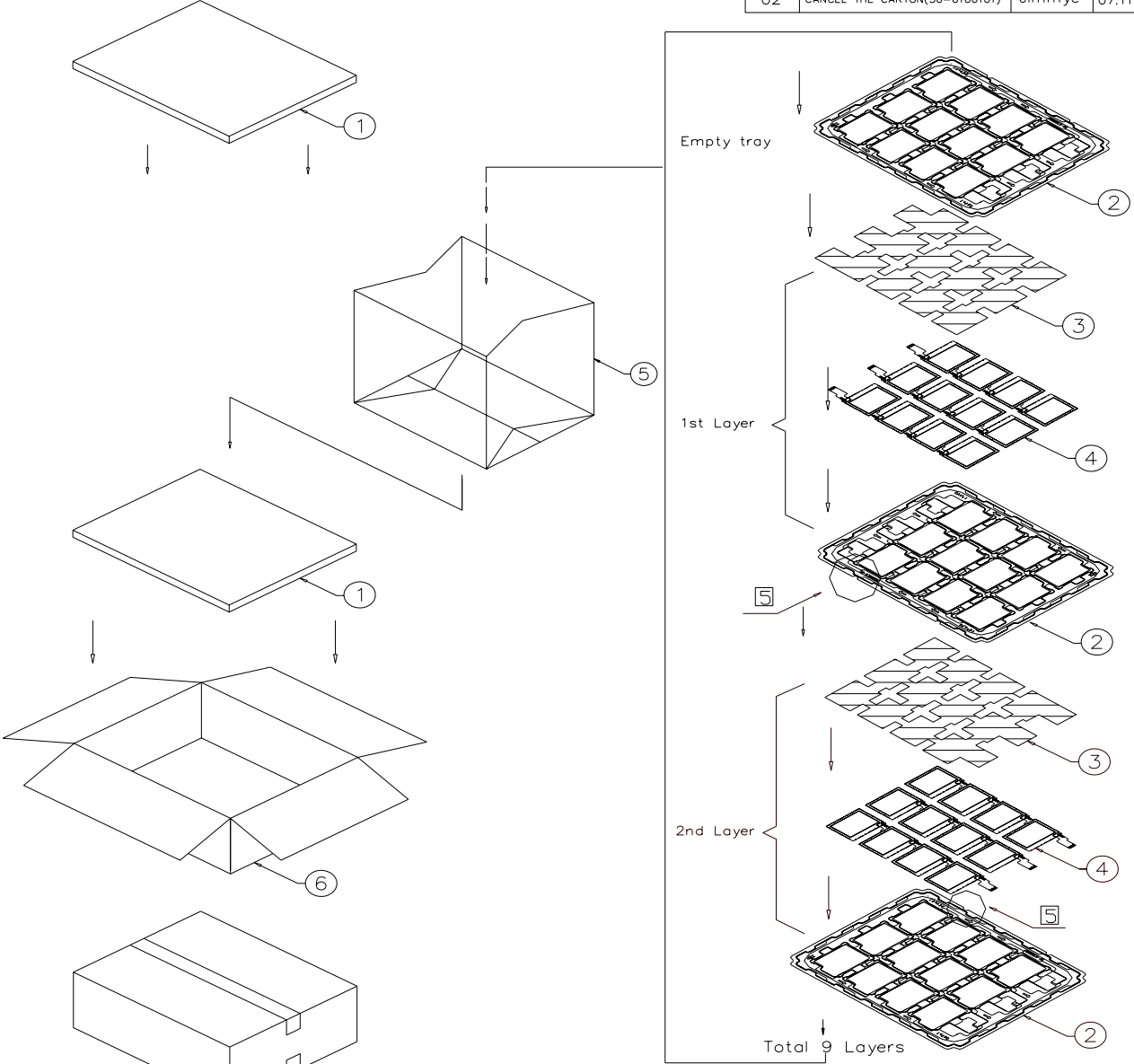
In the standard conditions, there is not display function NG issue occurred. (Including: line defect , no image). All the cosmetic specification is judged before the reliability stress.

13. Block Diagram




14. Packing

| REV | DESCRIPTION                   | DESIGN | DATE     |
|-----|-------------------------------|--------|----------|
| 01  | INITIAL RELEASE               | Jimmyc | 05.12.06 |
| 02  | CANCEL THE CARTON(50-0100101) | Jimmyc | 07.11.05 |



**NOTE:**  
 1. One layer include: 1 piece of cushion sheet, 12 pcs panel & 1 piece of tray.  
 2. Q'TY: 108 pcs panel/carton.  
 3. Dimension: 455\*375\*190mm  
 4. Weight: 8.5 KG  
 5. tray 需180°交叉堆疊，疊堆後可從側邊檢視圓弧防呆方向是否正確

|      |            |                   |     |        |
|------|------------|-------------------|-----|--------|
| 6    | 50-0100091 | CARTON INTERNAL   | 1   |        |
| 5    | 50-0500041 | 槽口袋450*380*700mm  | 1   | 抗靜電    |
| 4    |            | PA035XS Panel     | 108 |        |
| 3    | 50-0200035 | EPE CUSHION SHEET | 9   | 抗靜電    |
| 2    | 50-0300882 | PS TRAY           | 10  | 抗靜電    |
| 1    | 50-0300491 | EPE FOAM          | 2   |        |
| ITEM | PART NO.   | DESCRIPTION       | QTY | REMARK |

|           |            |                   |      |        |                       |  |  |      |      |
|-----------|------------|-------------------|------|--------|-----------------------|--|--|------|------|
| MTL.SPEC. |            | UNSPECIFIED TOL'S |      | REMARK |                       |  元太科技股份有限公司<br>Prime View International Co., Ltd. |  |      |      |
|           |            | ANGLE             |      |        |                       |  |  |      |      |
|           |            | ROUGHNESS         |      |        |                       |  |  |      |      |
| APPROVE   | Frank Shin | SCALE             | UNIT | SHEET  | DWG.TITLE             |  |  |      |      |
| CHECK     | Frank Shin | 1:1               | mm   | 1 OF 1 | PA035XSE PACKING DRAW |  |  |      |      |
| DESIGN    | Jimmyc     | MTL.NO.           |      |        | DWG.NO.               |  |  | REV. | SIZE |
|           |            |                   |      |        |                       |  |  | 02   | A4   |