MODEL	YTS200EF01
Rev. No	00

MODEL NO. : YTS200EF01

Approved by :

LCD DIVISION

YOUNG JIN COMPLEX

REV. NO.	REV. DATE	PAGE	REVISION DESCRIPTION	BEFORE	AFTER
00				-	-

CONTENTS

1. FEATURES

1.1 LCD Module

Item	LCD Module
LCD Type	Transmissive mode , Normally White
Glass Thickness	1.3(Max)mm—with polarizer
Display Resolution	176 x RGB x 220 Dots
Number of Color	262,144 color
MPU Interface	80-System, 16bit
Driver IC	R61503U

2. ELECTRIC ABSOLUTE MAXIMUM RATINGS

Item	Symbol	MIN	MAX	UNIT
Supply Voltage for LCD	Vcc	+2.8	+3.3	V
Supply Current for BLU	LED+	-	30	mA
Input Voltage	DB2~DB17 LCD_RS LCD_WR LCD_CS LCD_ RESET	VCC -0.3	VCC +0.3	V

3. MECHANICAL SPECIFICATIONS

3.1 Entire Dimension

Item	Specification	Unit
External dimension (W x H x T)	38.1×76.65×2.6(Without Boss)	mm
Total Weight (Typical)	7.0	g

3.2 LCD Panel Dimension

Item		Specification	Unit
LCD Panel	Glass Size (W x H x T)	35.68x47.3x0.8(MAX)	mm
	Viewing Area (W x H)	32.88x 40.8	mm
	Active Area (W x H)	31.68x39.6	mm
	Resolution (W x H)	176xRGBx220 dots	Dots
	Pixel size (W x H)	0.18 x 0.18	mm
	Dot Pitch (W x H)	0.06 x 0.18	mm

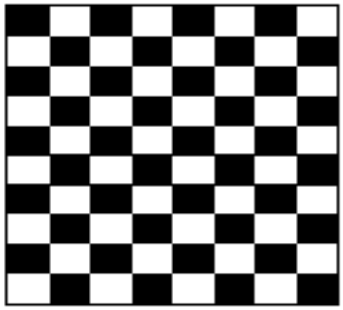
4. ENVIRONMENTAL CONDITION

Item		Min	Max	Remark
Storage Temperature	Main	-30°C	+80°C	Condensation not allowed
Operating Temperature	Main	-20°C	+70°C	

5. DC CHARACTERISTICS

Item	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	Vcc	Vcc = 2.8V	2.3	2.8	3.1	V
Input high voltage	VIH	Vcc = 2.8V	0.7Vcc	-	Vcc	V
Input low voltage	VIL	Vcc = 2.8V	Vss		0.3Vcc	V
Output high voltage	V0H	I0H = -0.06mA	Vcc-0.3	-	Vcc	V
Output low voltage	V0L	I0L = 0.06mA	Vss	-	Vss+0.3	V
Input leakage current	ILI1	VI = Vcc or GND	-1.0	-	+1.0	uA
Current consumption for normal operation (*1)	Icc	Vcc = 2.8V Ta = 25°C Measuring Point: Vcc	-	3.3	-	mA

NOTE*1) LCD Test Pattern : Mosaic Pattern



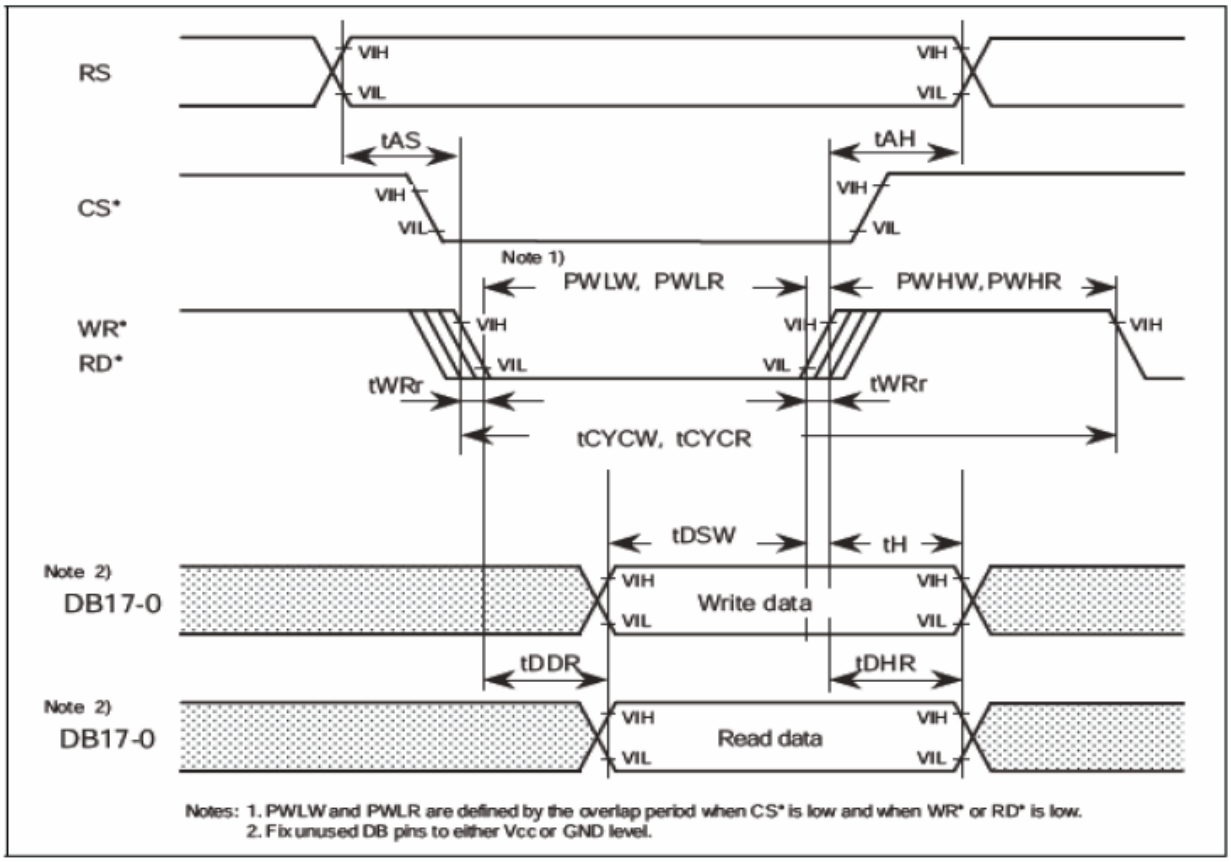
6. AC CHARACTERISTICS

6.1 LCD DISPLAY AC CHARACTERISTICS

- Parallel interface Characteristics (80-svstem mode)

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	Figure 90	100	-	20,000
	Read (transmitted)	t_{SCYC}	ns	Figure 90	350	-	20,000
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 90	40	-	-
	Read (transmitted)	t_{SCH}	ns	Figure 90	150	-	-
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 90	40	-	-
	Read (transmitted)	t_{SCL}	ns	Figure 90	150	-	-
Serial clock rise/fall time		t_{SCr}, t_{SCf}	ns	Figure 90	-	-	20
Chip select setup time		t_{CSU}	ns	Figure 90	20	-	-
Chip select hold time		t_{CH}	ns	Figure 90	60	-	-
Serial input data setup time		t_{SISU}	ns	Figure 90	30	-	-
Serial input data hold time		t_{SIH}	ns	Figure 90	30	-	-
Serial output data delay time		t_{SOD}	ns	Figure 90	-	-	130
Serial output data hold time		t_{SOH}	ns	Figure 90	5	-	-

* 80-system Bus Operation



7. ELECTRO-OPTICAL CHARACTERISTICS

7.1 LCD Panel Electro-Optical Characteristics

Optical characteristics are determined after the unit has been ' **ON**' and stable for approximately 30 minutes in a dark environment at 25°C. The values specified are an approximate distance 50cm From the TFT-LCD surface at a viewing angle of Θ equal to 0°
Measurement condition: Refer to next page (C-light source, Halogen Lamp)

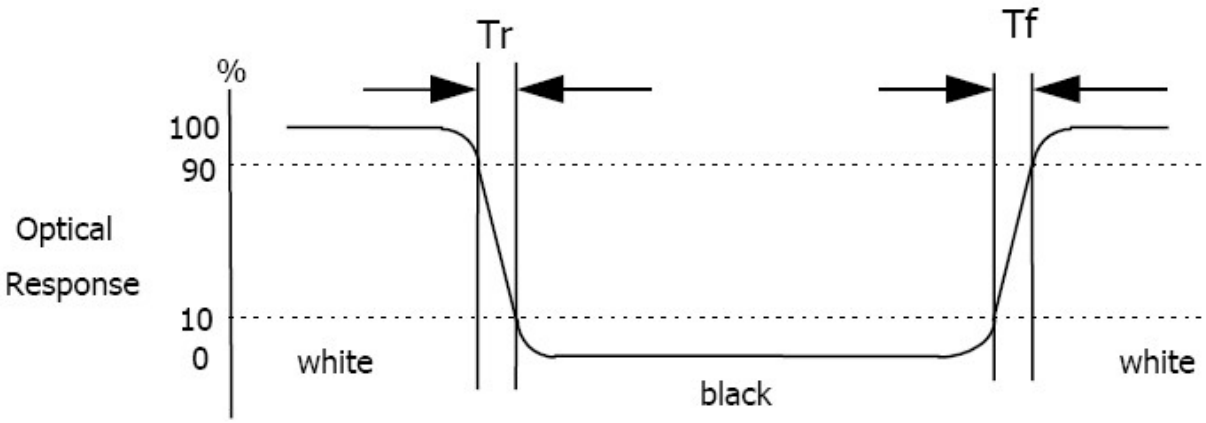
(Ta=25°C)

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing angles		Θ l	C/R ≥ 10	45	-	-	Degree	ALL Left side Date base On LPL's Following condition Normal Polarizer REFERENCE Only
		Θ r		45	-	-		
		Θ u		35	-	-		
		Θ d		15	-	-		
Contrast ratio		C/R	-		350	-	-	
Threshold Voltage		Vsat		1.90	2.15	2.40	V	
		Vth		0.90	1.10	1.30		
Response Time		Tr + Tf		-	25	40	msec	
Chromaticity (Only color filter)	White	x	Θ =0°	0.287	0.307	0.327	-	
		y		0.323	0.343	0.363		
	R	x		0.580	0.600	0.620		
		y		0.300	0.320	0.340		
	G	x		0.289	0.309	0.329		
		y		0.541	0.561	0.581		
	B	x		0.118	0.138	0.158		
		y		0.142	0.162	0.182		

7.2 LCD Panel Definitions of Electro-Optical Characteristics

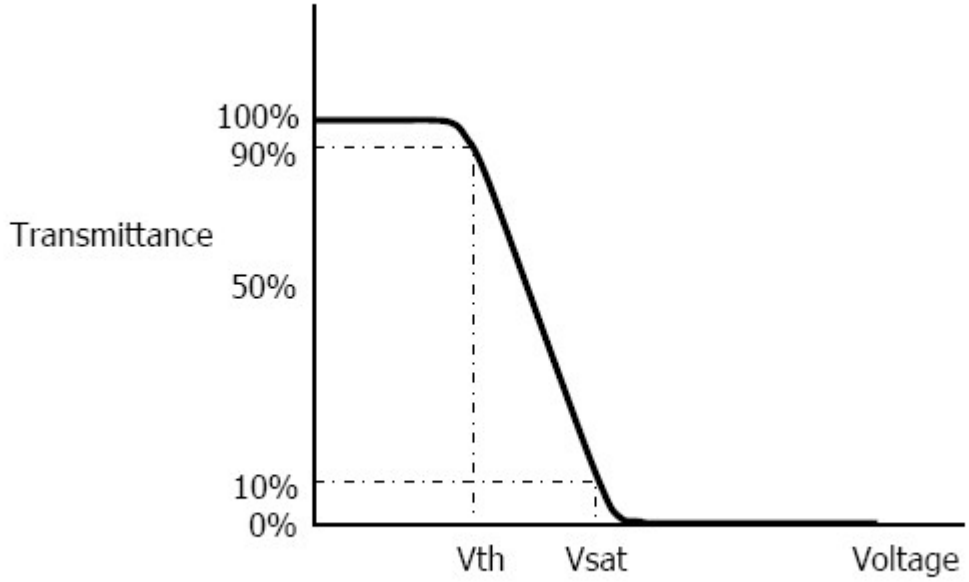
7.2.1 Definitions of response time

The response time defined as the following figure and shall be measured by Switching the input signal or " black" and " white"



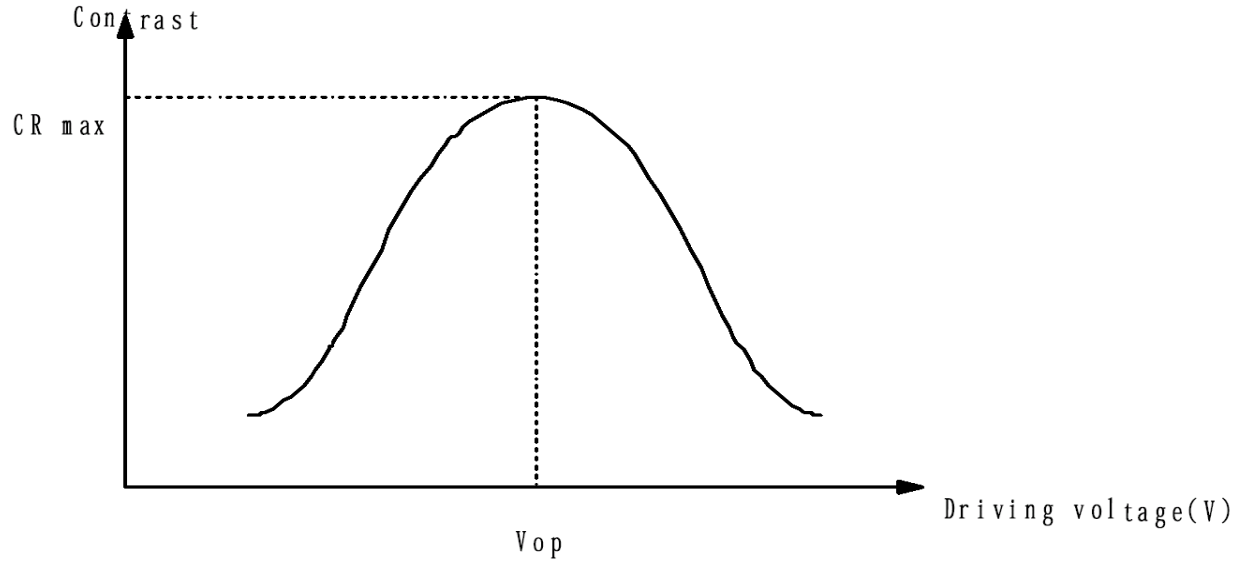
Response Time of LCD

7.2.2 Definition of Vth and Vsat



7.2.3 Definition of contrast ratio, Vop

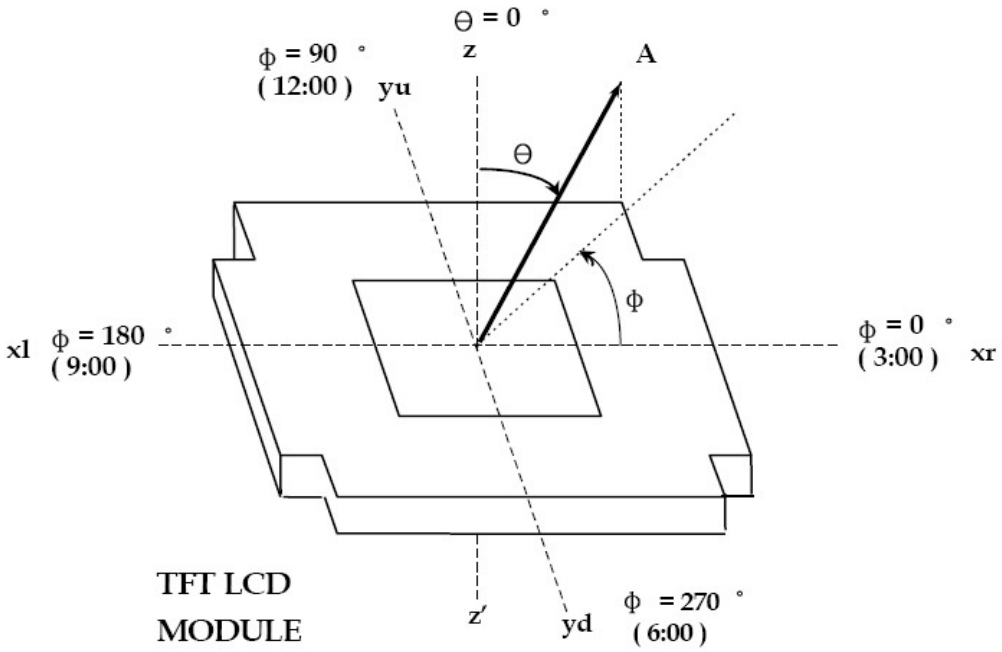
CR(Contrast)= Brightness all pixels " White"
Brightness all pixels " Black"



DEFINITION OF CONTRAST RATION of LCD

7.2.4 Definition of viewing & visual angle

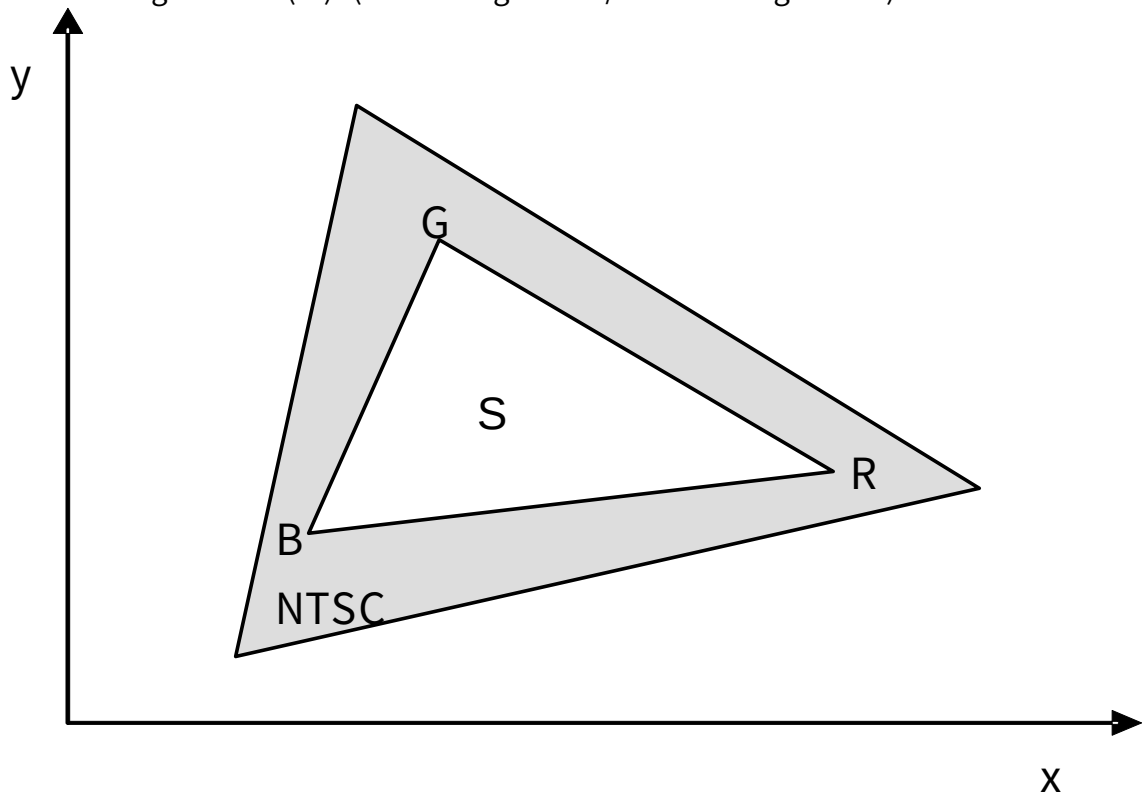
(dimension of viewing angle range)



VIEWING ANGLE of MAIN LCD

7.2.5 Definition of color Gamut

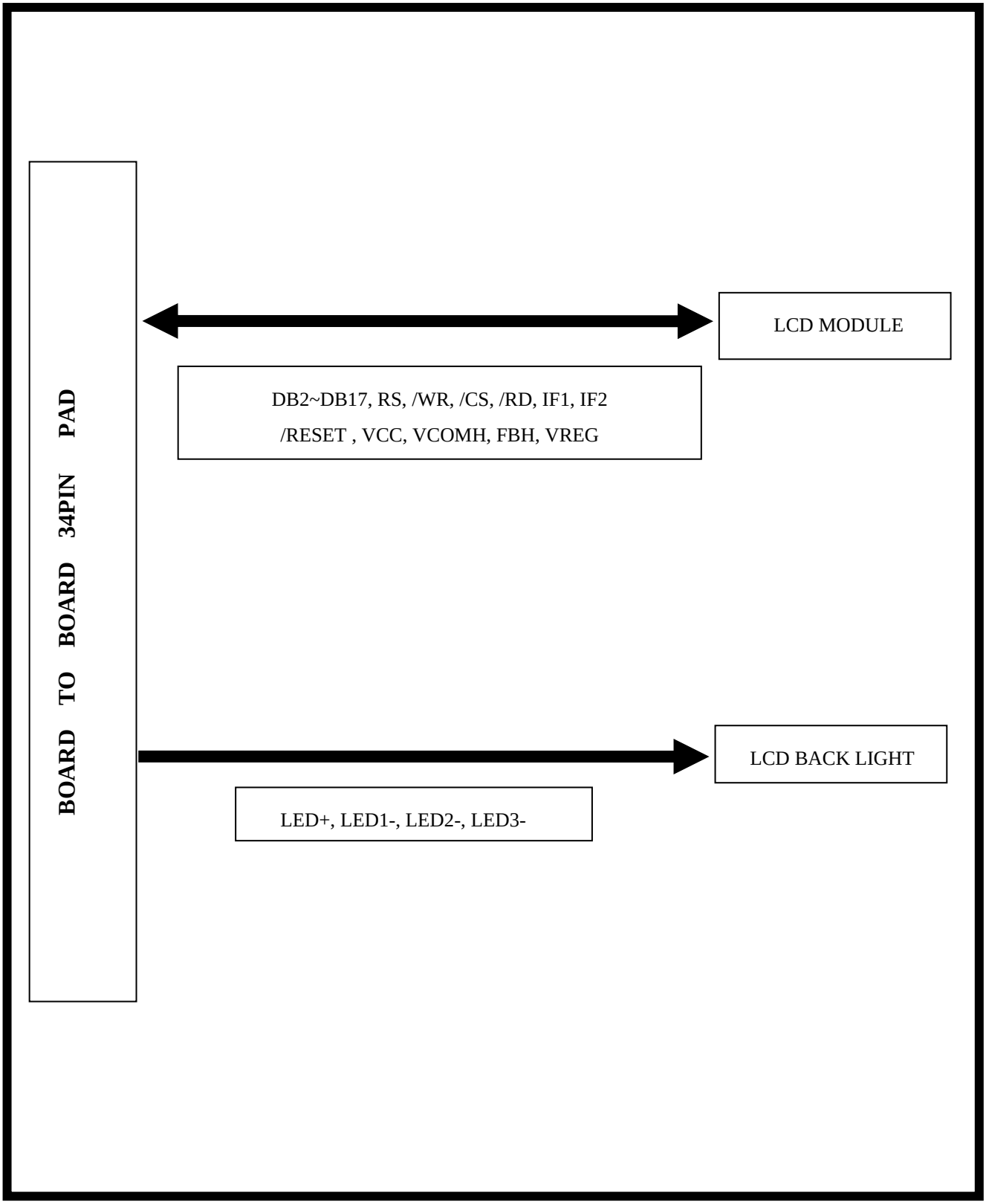
Color gamut : S(%)=(RGB triangle Area/ NTSC triangle Area) x100



8. INPUT PIN DESCRIPTION
8.1 34 PIN PAD

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	GND	G	Ground
2	IF1	I	MPU Interface switching pin.
3	IF2		
4	/RESET	I	Reset pin. Reset if set to LOW
5	/CS	I	Chip select pin. When LCD_CS = LOW, data and command input is enabled.
6	RS	I	Data/command identification pin. When RS = HIGH, data entered in the data bus pins. When RS = LOW, command entered in the data bus pins.
7	/WR	I	Write pin A signal on the data bus is latched at the rising edge of the LCD_WR signal.
8	/RD	I	Read pin. While this signal is kept LOW, the data bus is output enabled at the /RD signal pin of 80-series MPU.
9	DB2	I/O	16bit parallel bi-directional data bus. -. 16bit I/F : DB17-DB2are used
10	DB3		
11	DB4		
12	DB5		
13	DB6		
14	DB7		
15	DB8		
16	DB9		
17	DB10		
18	DB11		
19	DB12		
20	DB13		
21	DB14		
22	DB15		
23	DB16		
24	DB17		
25	VCC	P	Power supply for LCD.
26	VCC		
27	VCOMH2	0	This pin is used for connecting to FBH to adjust the VC voltage With the built-in electronic control.
28	FBH	I	It is an adjustment voltage input pin in the case of adjusting VCOMH voltage.
29	VREG	O	Reference voltage for built-in power supply.
30	LED+	P	This is a power supply signal for LED+ driving.
31	LED1-	P	This is a power supply signal for LED- driving.
32	LED2-		
33	LED3-		
34	GND	G	Ground

9. BLOCK DIAGRAM

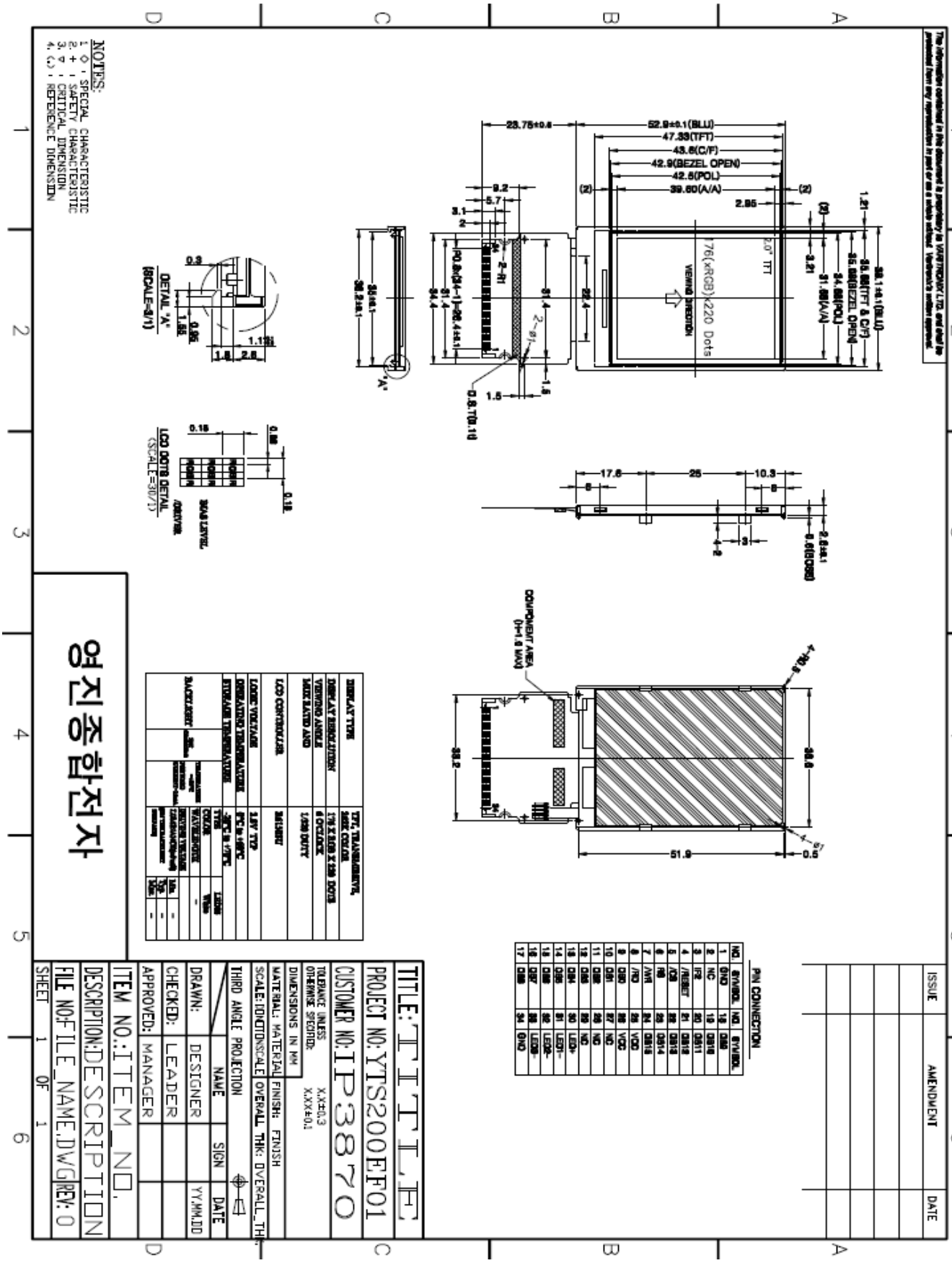


10. INSTRUCTION LIST

No.	Command	Parameter	Code (Bin)								Decimal	Initial state
			D17	D16	D15	D14	D13	D12	D11	D10		
3	Sets display	P1	0	0	0	0	*	*	0	0	0	1H=74 clocks
		P2	0	1	0	0	1	0	0	1	73	1H=74 clocks
		P3	0	0	*	*	*	*	0	0	—	Liquid crystal type, etc.
		P4	*	1	0	0	*	1	0	0	—	Boosting clock frequency
		P5	1	1	0	1	1	0	1	1	219	220-line display
		P6	0	0	0	0	0	0	0	0	0	All pins enabled.
		P7	0	0	0	0	0	0	1	0	2	Number of back poaching lines 3
		P8	0	0	0	0	0	0	0	1	1	Number of front poaching lines 2
		P9	*	*	*	*	*	0	0	0	0	All pins enabled.
4	Set Display Timing	P1	0	0	0	0	0	0	0	0	0	Source output ON at the 1st clock
		P2	0	1	0	0	0	1	1	0	70	Source output OFF at 71st clock
		P3	0	0	0	0	0	1	0	0	4	Gate output ON at the 5th clock
		P4	0	1	0	0	0	1	0	0	68	Gate output OFF at the 69th clock
		P5	*	*	*	*	0	0	0	0	0	Drive mode switch
		P6	0	0	0	1	0	0	1	1	19	VCOM boost timing
		P7	0	0	0	0	1	0	0	1	9	Drive mode switch timing
5	Set Data	P1	0	0	0	0	0	0	0	0	—	Row address normal setup
6	Set Start Address	P1	0	0	0	0	0	0	0	0	0	Start Column Address
		P2	0	0	0	0	0	0	0	0	0	Start Row Address
7	Set End Address	P1	1	0	1	0	1	1	1	1	175	End Column Address
		P2	1	1	0	1	1	0	1	1	219	End Row Address
11	Set Area Scrolling	P1	0	0	0	0	0	0	0	0	0	Start address
		P2	1	1	0	1	1	0	1	1	219	End address
		P3	0	0	0	0	0	0	0	0	0	Number of scroll lines 0
		P4	*	*	*	*	*	*	1	1	—	The full-screen can be scrolled.
12	Display Start Line	P1	0	0	0	0	0	0	0	0	0	Display Start Line 0
13	Partial Display In	P1	0	0	0	0	0	0	0	0	0	Area 1 Start Line 0
		P2	0	0	0	0	0	0	0	0	0	Area 1 End Line 0
		P3	0	0	0	0	0	0	0	0	—	Non-display refresh rate
15	Set Display Data Interface	P1	0	0	0	0	0	0	0	0	0	MPU interface 18 bits
		P2	*	*	*	*	*	*	0	0	0	Division is not done.
16	Set Display Color Mode	P1	*	*	*	*	*	0	0	0	—	Select voltage and display color
		P2	*	0	0	1	*	0	0	1	—	Gray scale amplifier ability
		P3	*	1	0	0	*	1	0	0	—	Bias setting
		P4	*	1	0	0	*	1	0	0	—	Boosting clock frequency
17	Set Gate Line Scan Mode	P1	*	*	*	*	0	*	0	0	—	Normal direction, interlace drive
		P2	0	0	0	0	0	0	0	0	0	Scan start line
		P3	1	1	0	1	1	0	1	1	219	Scan end line

No.	Command	Parameter	Code (Bin)								Decimal	Initial state
			D17	D16	D15	D14	D13	D12	D11	D10		
18	Set AC Operation Drive	P1	*	*	*	*	*	*	0	0	—	n-line reverse
		P2	*	*	*	*	0	0	0	0	0	n-line set 1
19	Set Electronic Control	P1	*	*	*	0	0	0	0	0	0	VDDHS
		P2	*	*	0	0	0	0	0	0	0	VCOMH
		P3	*	*	*	0	0	0	0	0	0	VCA
		P4	*	*	*	0	0	0	0	0	0	VDDRH
		P5	*	*	*	0	0	0	0	0	0	VDDRL
		P6	*	*	*	0	0	0	0	0	0	VONREG
		P7	*	*	*	0	0	0	0	0	0	VOFREG
		P8	*	*	*	*	*	0	0	0	0	VLDO
20	Set γ Correction Characteristics	P1	0	0	1	1	0	0	1	0	—	VRP3 VRP0
		P2	*	0	0	0	*	0	0	0	—	VRP2 VRP1
		P3	*	1	0	0	*	1	0	0	—	VP2 VP1
		P4	*	1	0	0	*	1	0	0	—	VP4 VP3
		P5	*	1	0	0	*	1	0	0	—	VP6 VP5
		P6	*	1	0	0	*	1	0	0	—	VP8 VP7
21	Set Power Control	P1	0	0	0	1	0	0	0	0	—	Wait1, 2
		P2	0	0	0	1	0	0	0	1	—	Wait3, 4
		P3	*	*	*	*	0	0	0	0	—	Booster circuit
		P4	0	0	*	0	0	0	0	0	—	Regulator 1
		P5	0	0	0	0	0	0	0	0	—	Regulator 2
		P6	0	0	0	*	*	*	*	*	—	Regulator 3
		P7	*	1	0	0	*	1	0	0	—	Pre-buffer ability setting
		P8	0	0	0	0	0	0	0	0	—	Gray scale amplifier control 1
		P9	*	*	*	*	*	*	0	0	0	Gray scale amplifier control 2
		PA	0	0	0	0	0	0	0	0	0	Gray scale amplifier output Hz1
		PB	*	*	*	*	*	*	0	0	0	Gray scale amplifier output Hz2
		PC	*	0	0	1	*	0	0	1	—	Gray scale amplifier ability
		PD	*	1	0	0	*	1	0	0	—	Bias setting
22	Set Partial Power Control	P1	*	*	*	0	*	0	0	1	—	VCOM ability setting
		P2	*	1	0	0	*	1	0	0	—	Boosting clock frequency
		P3	*	*	*	0	0	0	0	0	—	Regulator 1
		P4	0	0	0	*	0	0	0	0	—	Regulator 2
		P5	0	0	0	*	*	*	*	*	—	Regulator 3
		P6	*	0	0	1	*	0	0	1	—	Gray scale amplifier ability
		P7	*	1	0	0	*	1	0	0	—	Bias setting
29	Test	P1	*	*	0	0	0	0	0	0	—	VREG adjustment
		P2	*	*	*	*	0	0	0	0	—	Constant current adjustment
		P3	*	*	*	0	0	0	0	0	—	Oscillation frequency adjustment
		P4	*	0	0	0	0	0	0	0	—	Discharge control 1
		P5	0	0	0	0	0	0	0	0	—	Discharge control 2
		P6	*	*	0	0	0	0	0	0	—	Gate driver test
		P7	0	*	*	*	0	0	0	0	—	Detector test
32	Revision Read	P1	0	0	0	0	1	1	0	1	—	00H

11. MODULE DIMENSION



12. Instruction List

12.1 LCD Instruction set

Main category		Sub category		Upper code								Lower code							
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
—	Index			*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status read			L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
0"	Display control 1	00h	Start oscillation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
			Device code read	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	1
		01h	Driver output control 1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
		02h	Liquid crystal drive waveform	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0
		03h	Entry mode	TRI	DFM1	DFM0	BGR	0	DACKE	HWM		0	0	ID1	ID0	AM	0	0	0
		04h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		05h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		06h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		07h	Display control 1	0	0	PTDE1	PTDE0	0	0	BASEE	0	0	0	GON	DTE	CL	0	D1	D0
		08h	Display control 2	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
		09h	Display control 3	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
		0A-0Bh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Ch	External display Interface 1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
		0Dh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Eh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Fh	External display Interface 2	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	DPL	EPL
1"	Power control	10h	Power control 1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	0	AP1	AP0	0	DSTB	SLP	STB
		11h	Power control 2	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC01	0	VC2	VC1	VC0
		12h	Power control 3	0	0	0	VCN	0	0	0	VCMR	VREG 1R	0	PSON	PON	VRH3	VRH2	VRH1	VRH0
		13h	Power control 4	VCOM G	0	0	0	VDV3	VDV2	VDV1	VDV0	VCM SEL	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
		14h	Power control 5	DC5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		15h- 17h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		18h	Power control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE
		19h-1Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2"	RAM Access	20h	RAM Address set (horizontal direction)	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		21h	RAM Address set (vertical direction)	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
		22h	RAM data write/ read	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interface's format.															
		23h- 27h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		28h	NV memory read data 1	0	0	0	0	0	0	0	0	0	0	0	0	UID3	UID2	UID1	UID0
		29h	NV memory read data 2	0	0	0	0	0	0	0	0	EVCM E0	0	0	EVCM 04	EVCM 03	EVCM 02	EVCM 01	EVCM 00
		2Ah	NV memory read data 3	0	0	0	0	0	0	0	0	EVCM E1	0	0	EVCM 14	EVCM 13	EVCM 12	EVCM 11	EVCM 10
		2Bh- 2Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3"	Gamma control	30h	Gamma control 1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
		31h	Gamma control 2	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
		32h	Gamma control 3	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
		33h	Gamma control 4	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
		34h	Gamma control 5	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
		35h	Gamma control 6	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
		36h	Gamma control 7	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
		37h	Gamma control 8	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
		38h	Gamma control 9	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	VRP 04	VRP 03	VRP 02	VPR 01	VRP 00
		39h	Gamma control 10	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00
		3Ah	Gamma control 11	0	0	0	VAJN 14	VAJN 13	VAJN 12	VAJN 11	VAJN 10	0	0	0	VAJP 04	VAJP 03	VAJP 02	VAJP 01	VAJP 00

Main category		Sub category		Upper code								Lower code							
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
		3Bh-3Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4*		40h- 4Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5*	Window address control	50h	Horizontal RAM address start position	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
		51h	Horizontal RAM address end position	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
		52h	Vertical RAM address start position	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
		53h	Vertical RAM address end position	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
		54h- 5Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6*		60h- 6Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7*	Base Image display control	70h	Driver output control 2	GS	0	0	NL4	NL3	NL2	NL1	NL0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0
		71h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VLE	REV
		72h- 79h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		7Ah	Vertical scroll control	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL5	VL3	VL2	VL1	VL0
		7Bh- 7Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8*	Partial image control	80h	Partial image 1 display position	0	0	0	0	0	0	0	0	PTDP 07	PTDP 06	PTDP 05	PTDP 04	PTDP 03	PTDP 02	PTDP 01	PTDP 00
		81h	Partial image 1 RAM area (start line)	0	0	0	0	0	0	0	0	PTSA 07	PTSA 06	PTSA 05	PTSA 04	PTSA 03	PTSA 02	PTSA 01	PTSA 00
		82h	Partial image 1 RAM area (end line)	0	0	0	0	0	0	0	0	PTEA 07	PTEA 06	PTEA 05	PTEA 04	PTEA 03	PTEA 02	PTEA 01	PTEA 00
		83h	Partial image 2 display position	0	0	0	0	0	0	0	0	PTDP 17	PTDP 16	PTDP 15	PTDP 14	PTDP 13	PTDP 12	PTDP 11	PTDP 10
		84h	Partial image 2 RAM area (start line)	0	0	0	0	0	0	0	0	PTSA 17	PTSA 16	PTSA 15	PTSA 14	PTSA 13	PTSA 12	PTSA 11	PTSA 10
		85h	Partial image 2 RAM area (end line)	0	0	0	0	0	0	0	0	PTEA 17	PTEA 16	PTEA 15	PTEA 14	PTEA 13	PTEA 12	PTEA 11	PTEA 10
		86h- 8Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9*	Panel interface control	90h	Panel interface control 1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
		91h	Panel interface control 2	0	0	0	0	0	NOI2	NOI1	NOI0	0	0	0	0	0	0	0	0
		92h	Panel interface control 3	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI2	SDTI1	SDTI0
		93h	Panel interface control 4	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
		94h	Panel interface control 5	0	0	0	0	NOE3	NOE2	NOE1	NOE0	0	0	0	0	0	0	0	0
		95h	Panel interface control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE2	SDTE1	SDTE0
		96h- 97h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		98h- 9Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A*	NV memory control	A0h	NV memory access control 1	0	0	0	0	0	0	0	0	TE	0	EOP1	EOP0	0	0	EAD1	EAD0
		A1h	NV memory access control 2	0	0	0	0	0	0	0	0	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
		A2h-A3h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
		A5h-AFh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

13. QUALITY STANDARD FOR LCD

13.1 Acceptable Quality Level

1. Objective

This specification book is the standard for LCD module general inspection. And also this book will be referring to customer approval specification.

2. Scope

This specification book is applicable to general LCD module. If supplier has any doubt or requirement, then it can be discussed.

3. Acceptable Quality Level

INSPECTION	SAMPLING PROCEDURES	A.Q.L
MAJOR	- MIL-STD-105E Inspection Level II - Normal Inspection - Single sample inspection	1.0
MINOR	- MIL-STD-105E Inspection Level II - Normal Inspection - Single sample inspection	1.5

- Major defect

A major defect is a defect that could result in failure or extremely reduction on the usability of the product for its intended purpose.

- Minor defect

A minor defect is one that does not materially reduce the usability of the product for its intended purpose or is a departure from established standards giving no significant bearing on the effective use or operation of the unit.

4. Inspection Conditions

4.1 The environmental conditions for inspection shall be as follows

- Room Temperature : 25±10°C
- Humidity : 45±20%RH

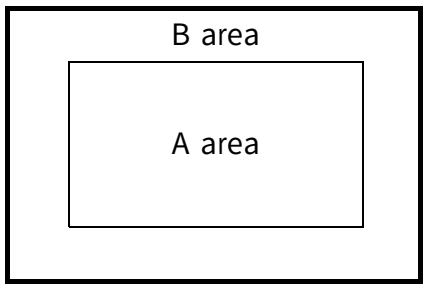
4.2 The external visual inspection

- The inspection shall be performed by using 20~40Watts fluorescent lamp for illumination and the distance between LCD and eyes of the inspector shall be 30cm or more.

5. Inspection Item

Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble	The color of a small area is different from the remainder. The phenomenon dose not changes with voltage.
Glass defect	Glass crack, Chip
Operating	Function, Contrast, Uniformity, Components

6. Definition of Inspection Area

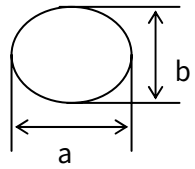
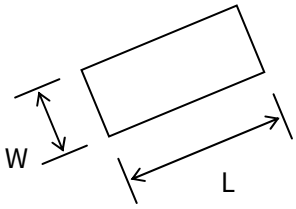
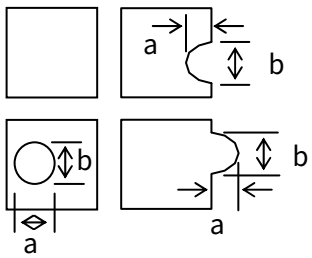


A area: Inside viewing area
B area: Outside viewing area

7. Inspection specifications

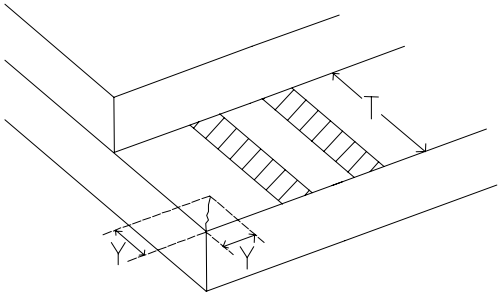
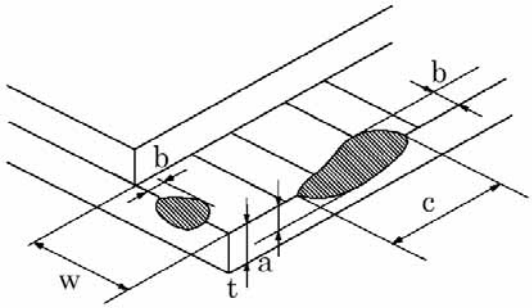
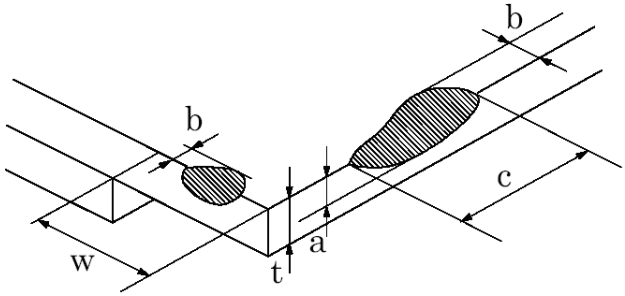
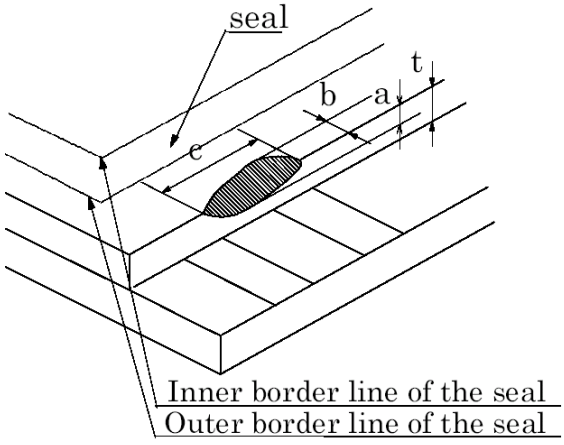
7.1 Non-operating inspection specification

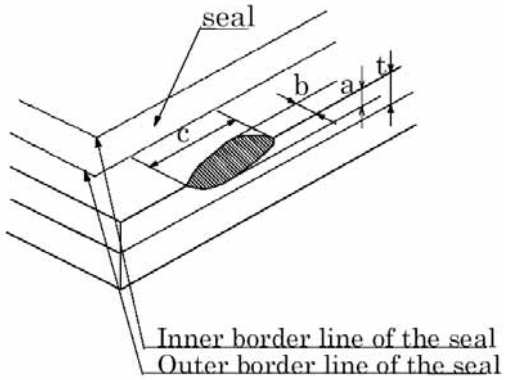
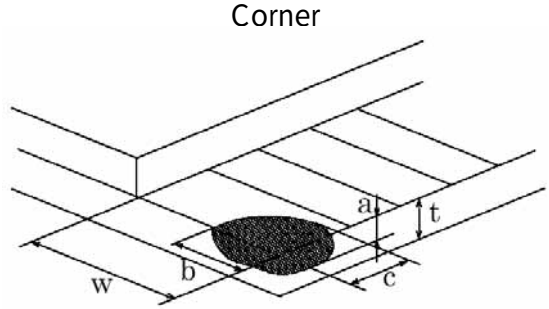
Class of	No.	Inspection Item	Criteria of defects	Acceptable Q'ty

defects						Zone A	Zone B
MAJOR	1	Circuits	1. Circuit short			0	0
			2. Circuit open				
MINOR	2	Black spot, White spot, Bright spot, Foreign particle  Φ = (a+b)/2	A	Φ ≤ 0.1		*	Ignore
			B	0.1 < Φ < 0.2		3	
			C	0.2 ≤ Φ < 0.3		2	
			D	0.3 ≤ Φ		0	
			Total defect point(B,C)			4	
			* Reject when 5 or more spots are gathered within 5mm circle.				
	3	Black line, White line 	A	W ≤ 0.02	-	*	Ignore
			B	0.02 < W ≤ 0.05	L ≤ 5	2	
			C	0.05 < W ≤ 0.1	L ≤ 3	2	
			D	0.1 < W	-	0	
			Total defect point(B,C)			3	
	4	Pattern deformity  Φ = (a+b)/2	1. Pin hole				
			A	Φ ≤ 0.15		Ignore	Ignore
			B	0.15 < Φ ≤ 0.2		2(*)	
				0.2< Φ		0	
			* Two pin hole shall not formed in the single dot				
			2. Excess, void				
			A	a ≤ 0.2 and b ≤ 0.2		Ignore	Ignore
			B	0.2 < a or 0.2 < b		0	

Class of defects	No.	Inspection Item	Criteria of defects	Acceptable Q'ty	
				A zone	B zone

MINOR	5	Bubble between Polarizer and panel	A	Φ ≤ 0.3	Ignore	Ignore
			B	0.3 < Φ ≤ 0.5	2	
			C	0.5 < Φ	0	
	6	Polarizer scratch and particle	Circular	Same as inspection item No.2		Ignore
			Linear	Same as inspection item No.3		
	7	Polarizer Dent	A	Φ ≤ 0.2	Ignore	Ignore
			B	0.2 < Φ ≤ 0.3	3	
			C	0.3 < Φ ≤ 0.4	2	
			D	0.4 < Φ	0	
			Total defect point(B,C)		4	
	8	Dirt on polarizer	Dirt which can be wiped easily should be accepted.			
	9	Protection film	The protection film should not be stripped up to viewing area and the peeled off angle should not exceed 20 degrees.			
	10	Polarizer shift	1. Shifting in position should not exceed the glass outline dimension. 2. Incomplete covering of the viewing area due to shifting is not allowed. 3. Shifting in position should be within the tolerance (refer to module dimensional drawing)			
	12	Tape	1. Location: refer to specification. 2. Insufficient adhesive.			
	13	TCP, FPC defect	Film or Pattern should not have crack.			
MAJOR	14	Components	Missing components not allowed.			

Class of defects	No.	Inspection Item	Criteria of defects
MAJOR	15	Progressive crack 	Reject any progressive crack.
MINOR	16	The front lead terminals 	a ≤ t b ≤ 1 c ≤ 7.0 * Glass crack should not cover alignment mark
	17	The rear of lead terminal 	a ≤ t b ≤ 1 c ≤ 7.0
	18	Short glass side 	a ≤ t c ≤ 7.0 b < Inner border line of the seal

Class of defects	No.	Inspection Item	Criteria of defects
MINOR	19	Side of glasses that is uniform in shape 	a ≤ t c ≤ 7.0 b < Inner border line of the seal
	20	Corner 	a ≤ t b ≤ 3.0 c ≤ 3.0 * Glass crack should not cover patterns used for recognition and assembly, alignment mark and patterns.

* Condition of item 2~9
1. Distance between defects must be more than 10mm with light on, more than 15mm with light off.
2. Total acceptable defect number
   - Defects with light on : 6 points
   - Defects with light off : 4 points
   - Total defect point : 6 points
3. Regarding the defect distance and total acceptable defect number, above 2-A, 3-A should be neglected.

*Condition of item 15 ~ 20
1. Total acceptable defect number: 4

7.2 Operating inspection specifications

Class of defects	No.	Inspection Item	Criteria of defects	
MAJOR	1	No display		
	2	Abnormal operation		
	3	Contrast defect	Judge according to module specification. Establish boundary sample if required.	
	4	Viewing angle defect	Judge according to module specification. Establish boundary sample if required.	
	5	Excess power consumption	Judge according to module specification.	
	6	Back-light defect	1. No light-on 2. Different color 3. Low brightness	
	7	Bright dot	N ≤ 1	Ignore
			1 < N	Reject
		Dark dot	N ≤ 2	Ignore
			2 < N	Reject
MINOR	8	Crosstalk defect	No noticeable crosstalk. Establish boundary sample if required.	
	9	Uneven brightness	No noticeable unevenness allowed. Establish boundary sample if required.	
	10	Uneven color	No noticeable unevenness allowed. Establish boundary sample if required.	
	11	Spot, Pinhole, Foreign particle, Line	Same as in Chapter 7.1	

14. RELIABILITY FLOW / TEST CONDITION FOR LCD

14. 1.1 LCD Reliability Data / Environmental Test

No.	Item	Condition	Test time	Note
1	High temp. storage	80°C	120 Hrs	
2	Low temp. storage	-30°C	120 Hrs	
3	High temp. operating	70°C	120 Hrs	
4	Low temp. operating	-20°C	120 Hrs	
5	High Temp, and High Humidity Operating	T = 40°C /90%	120 Hrs	
6	Thermal Shock	-30°C 60min => 25°C => 80°C 60min 25°C -. 50 cycle		

14.1.2 Test Method

a) The method of visual inspection is equal to the appearance standard
b) Evaluation and assessment made two hours after return to room temperature(25°C± 5°C)
c) The LCDs subjected to the test must not have dew condensation.
d) The non-uniformity and other appearance are checked in LCD.

14.1.3 Result Evaluation Criteria

There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

15.Precautions

15.1 Operation

Burn-in sometimes happens when the same character was displayed at along time.
Therefore, to prevent Burn-in, it is recommended to set up a Screen-saver function.

15.2 Safety

The liquid crystal in the LCD is poisonous, DO NOT put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

15.3 Handling

(1) The LCD module shall be installed flat, without twisting or bending
(2) To avoid damage in appearance or malfunction, DO NOT subject the module to mechanical shock or to excessive force on its surface.

(3) The polarizer attached to the display is very easy to damage, handle it with care to avoid scratching.
(4) COF or FPC has narrow pattern width, so easily become open circuit by external force. DO NOT apply pressure to COF or FPC especially in bending area.
(5) To avoid contamination on the display surface, DO NOT touch the display surface with bare hands.
(6) Provide a space so that the LCD module does not come into contact with other components.
(7) To protect the LCD panel from external pressure, put covering glass (acrylic board or similar board) to keep appropriate space between them.
(8) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(9) Property of semiconductor devices may be affected when they are exposed to
light possibly resulting in malfunctioning of the ICs. To prevent such malfunctioning of the ICs, your design and mounting layout done are so that the IC is not exposed to light in actual use.
(10) Strong light exposure causes degradation of color filter. It may not recover
(11) DO NOT contact with water to avoid Metal corrosion.

16.4 Static electricity

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge.
(1) Ground soldering iron tips, tools and testers when they operate.
(2) Ground your body when handling the products.
(3) DO NOT apply voltage to the input terminal without applying power supply.
(4) DO NOT apply voltage that exceeds the absolute maximum rating.
(5) Store the products in an anti-electrostatic container.
(6) Peel off protect tape, attached to polarizer, slowly to minimize ESD damage.

16.5 Storage

Store the products in a dark place at +5~+25 degree C, low humidity (50%RH or less).
DO NOT store the products in an atmosphere containing organic solvents or corrosive gases.

16.6 Cleaning

(1) DO NOT wipe the polarizer with dry cloth, as it might cause scratch.

(2) Wipe the polarizer with a soft cloth soaked with petroleum IPA, other chemical might damage.

16.7 Waste

When dispose of LCD module, manage it as the production waste.