제 7 장 Color TFT-LCD의 구조 및 동작 원리

4/19(수)

7.3 Color TFT-LCD의 동작원리

7.3.1 TFT-Array의 구성 및 동작원리

7.3.2 중간계조 표현방법

7.3.3 Color 표현방법

7.3.4 LCD의 표시성능

7.4 TFT-LCD의 Design Simulation

7.4.1 단위화소의 동작특성

7.4.2 TFT의 I-V 특성과 동작 Simulation

7.4.3 누설전류와 축적용량의 최적화

7.4.4 신호지연과 신호배선의 최적화

7.3 Color TFT-LCD의 동작원리

7.3.1 TFT-Array의 구성 및 동작원리

7.3.2 중간계조 표현방법

7.3.3 Color 표현방법

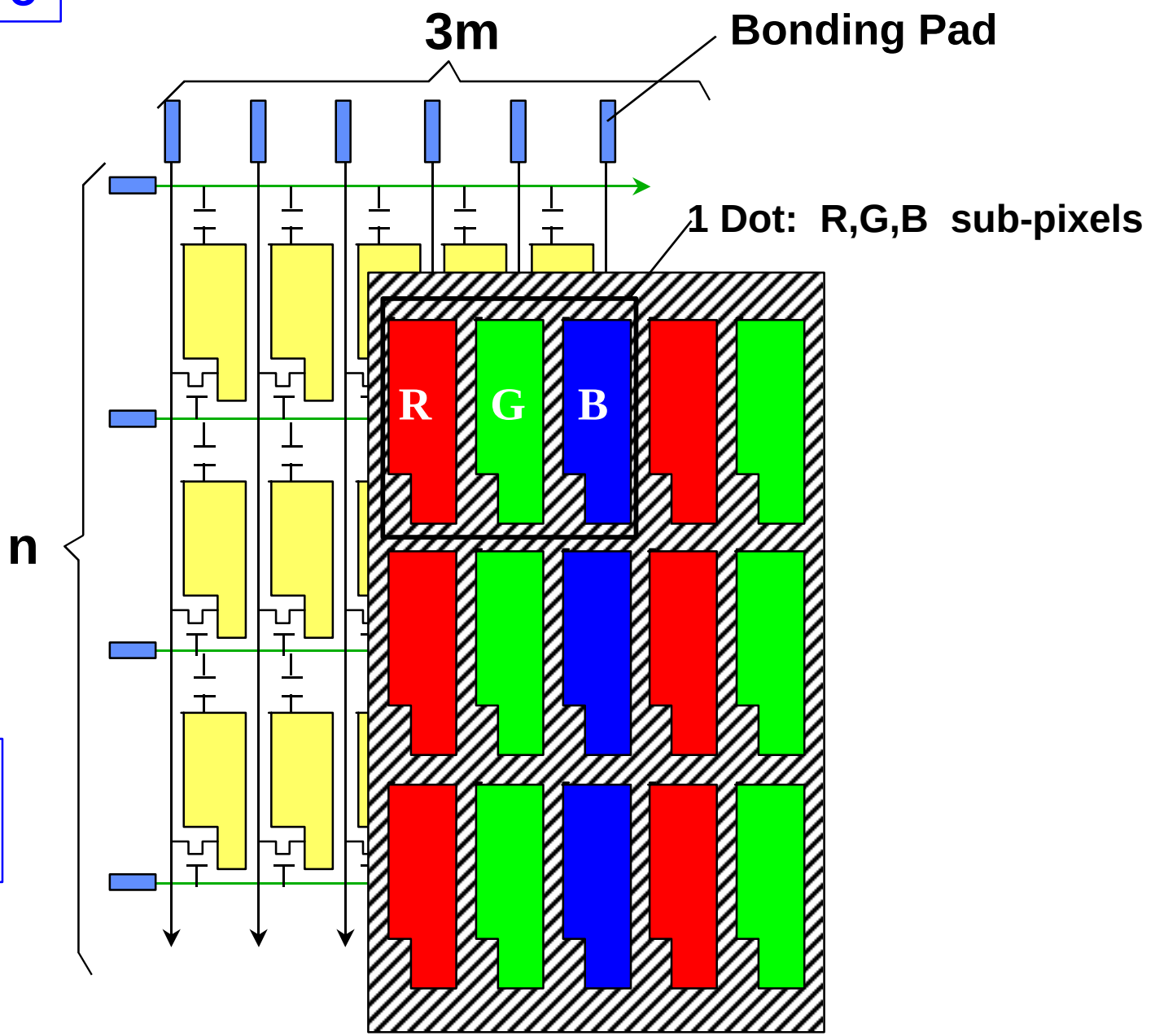
7.3.4 LCD의 표시성능

TFT-Panel의 구성

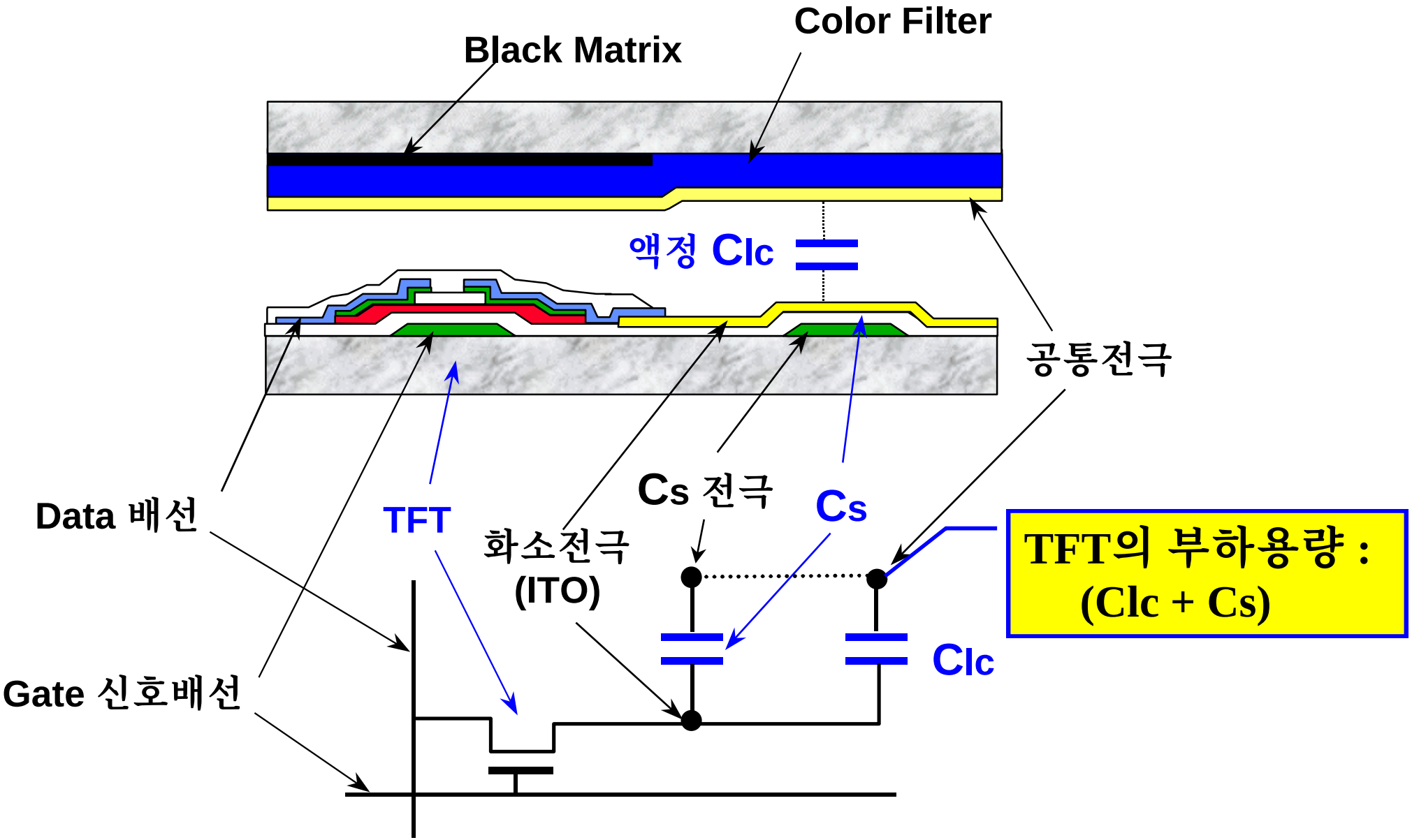
(m x n) 해상도

{(3xm) x n} matrix

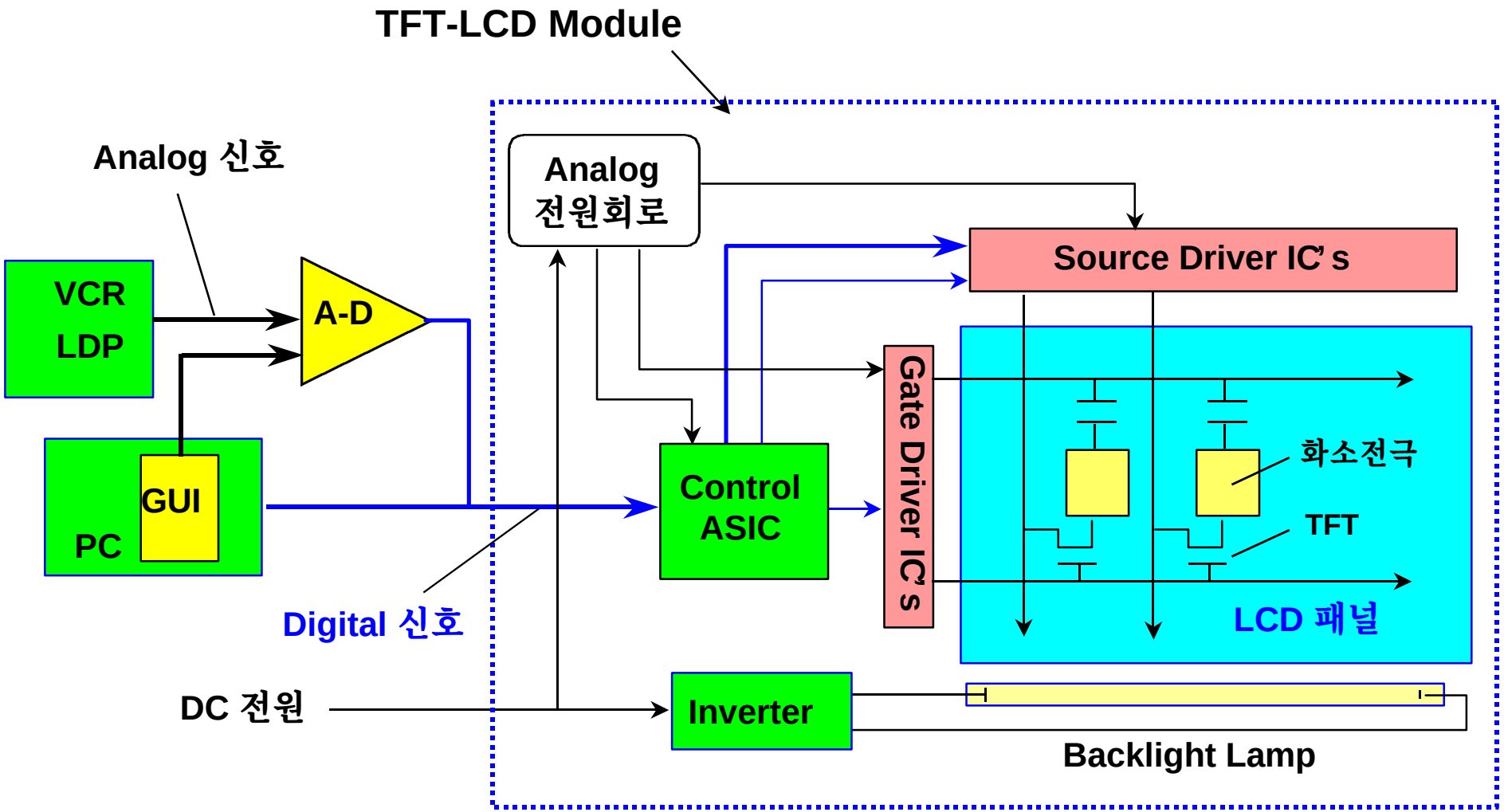
SVGA: 800 x 600
(2400 x 600) Matrix



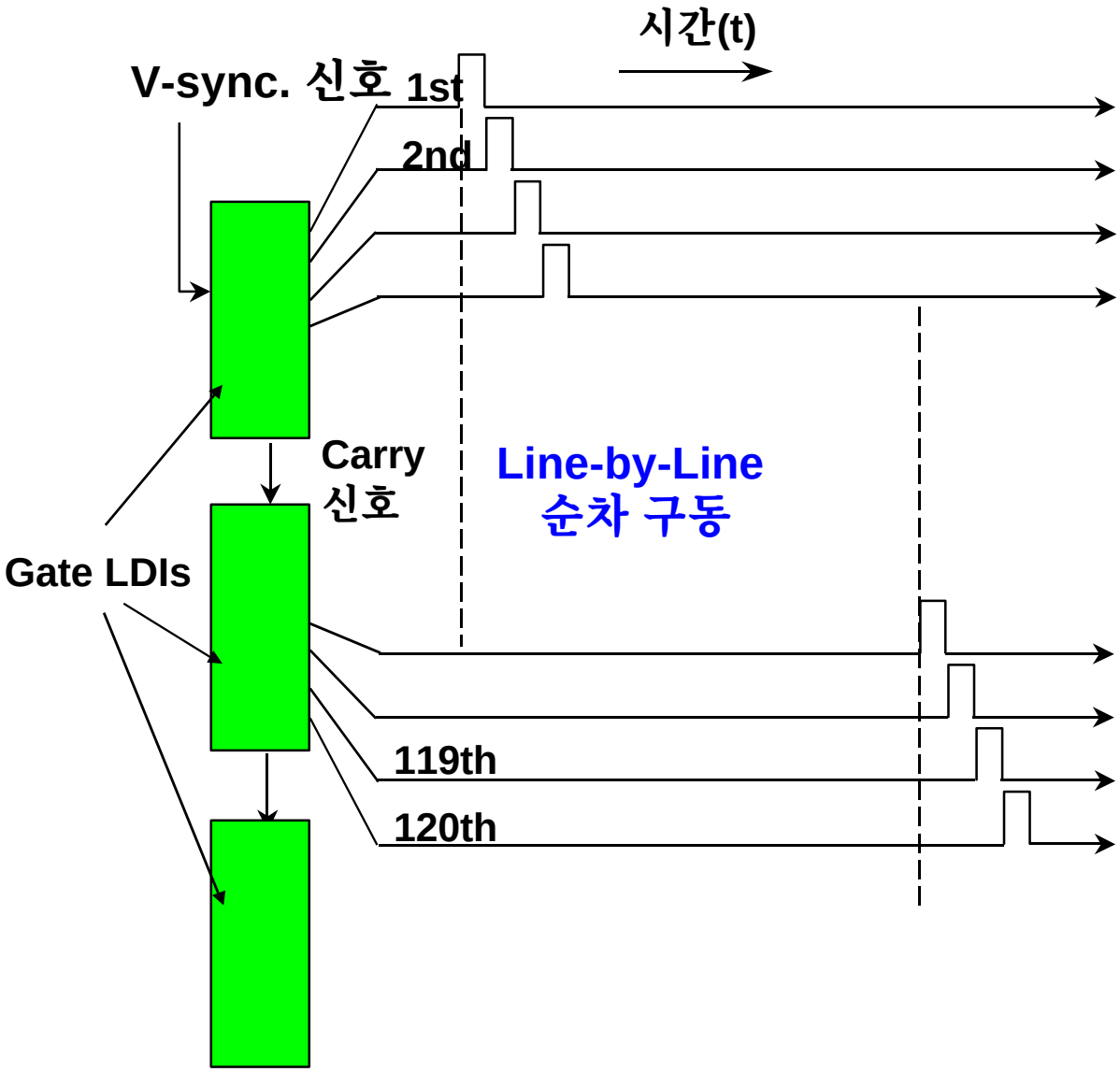
Unit Cell & 등가 회로

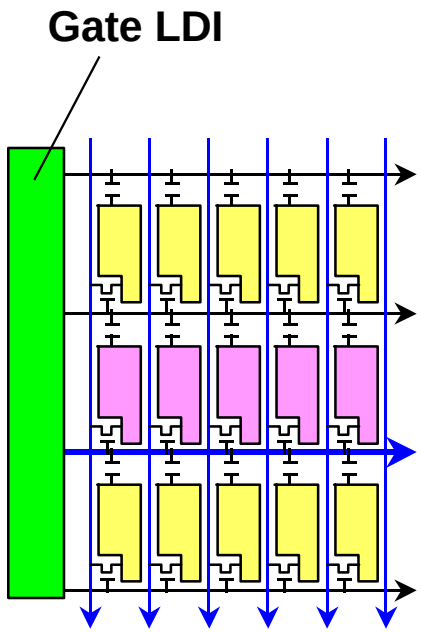


TFT-LCD Module의 구동 System 구성도



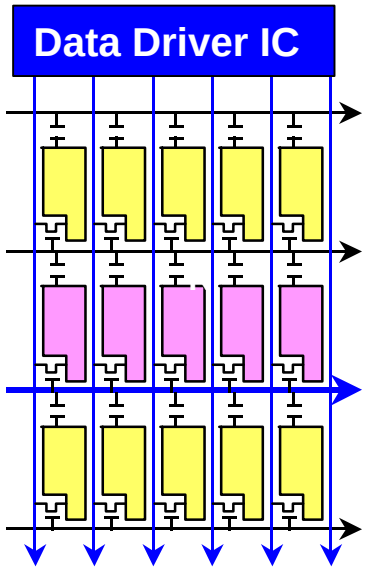
Gate 신호배선의 선택과 Scan Pulse 공급





Data Driver IC의 동작

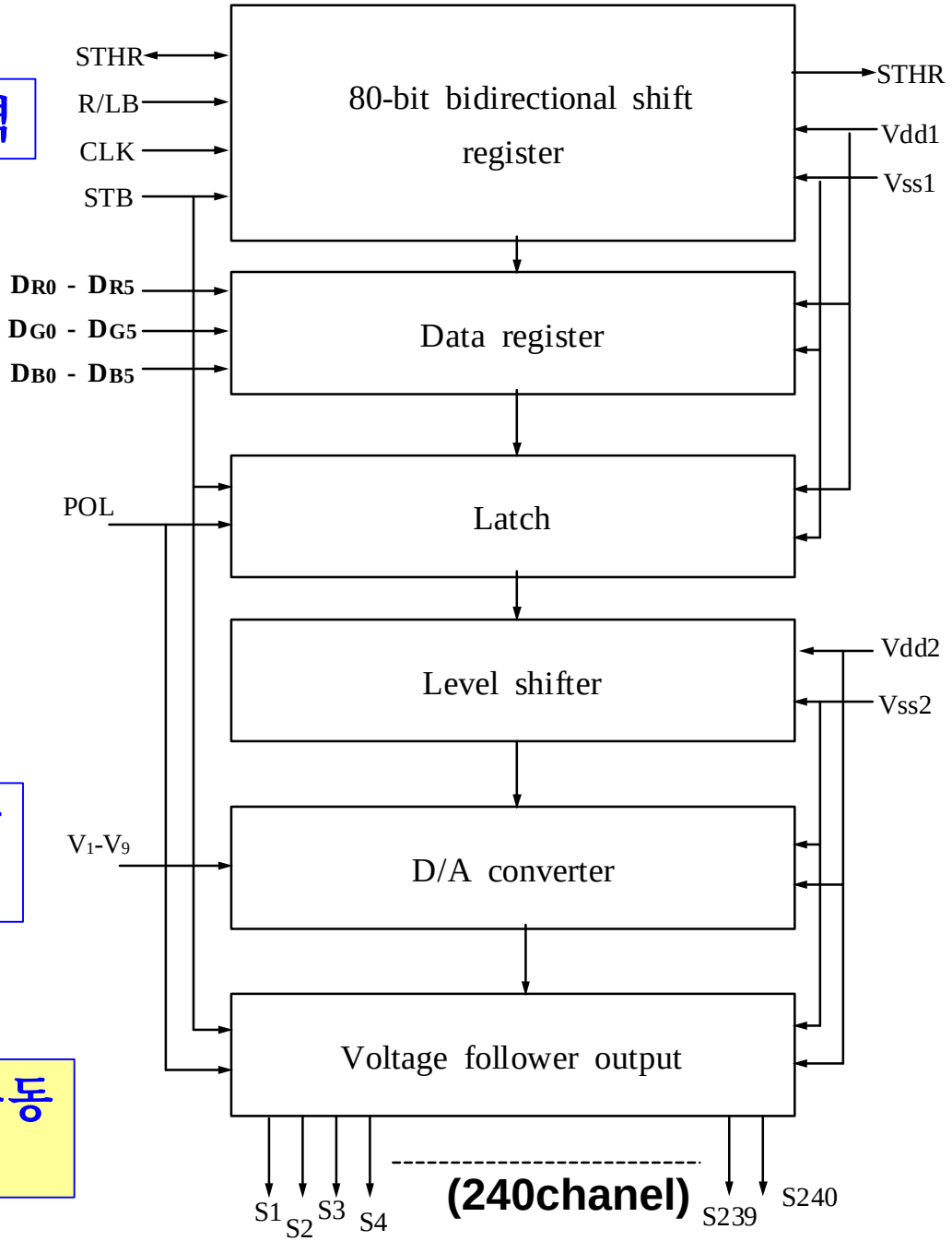
Control 신호 입력



18-bit digital data

계조 표준 전압 (V1~V9)

Line-by-Line 구동 (동시 출력)



7.3 Color TFT-LCD의 동작원리

7.3.1 TFT-Array의 구성 및 동작원리

7.3.2 중간계조 표현방법

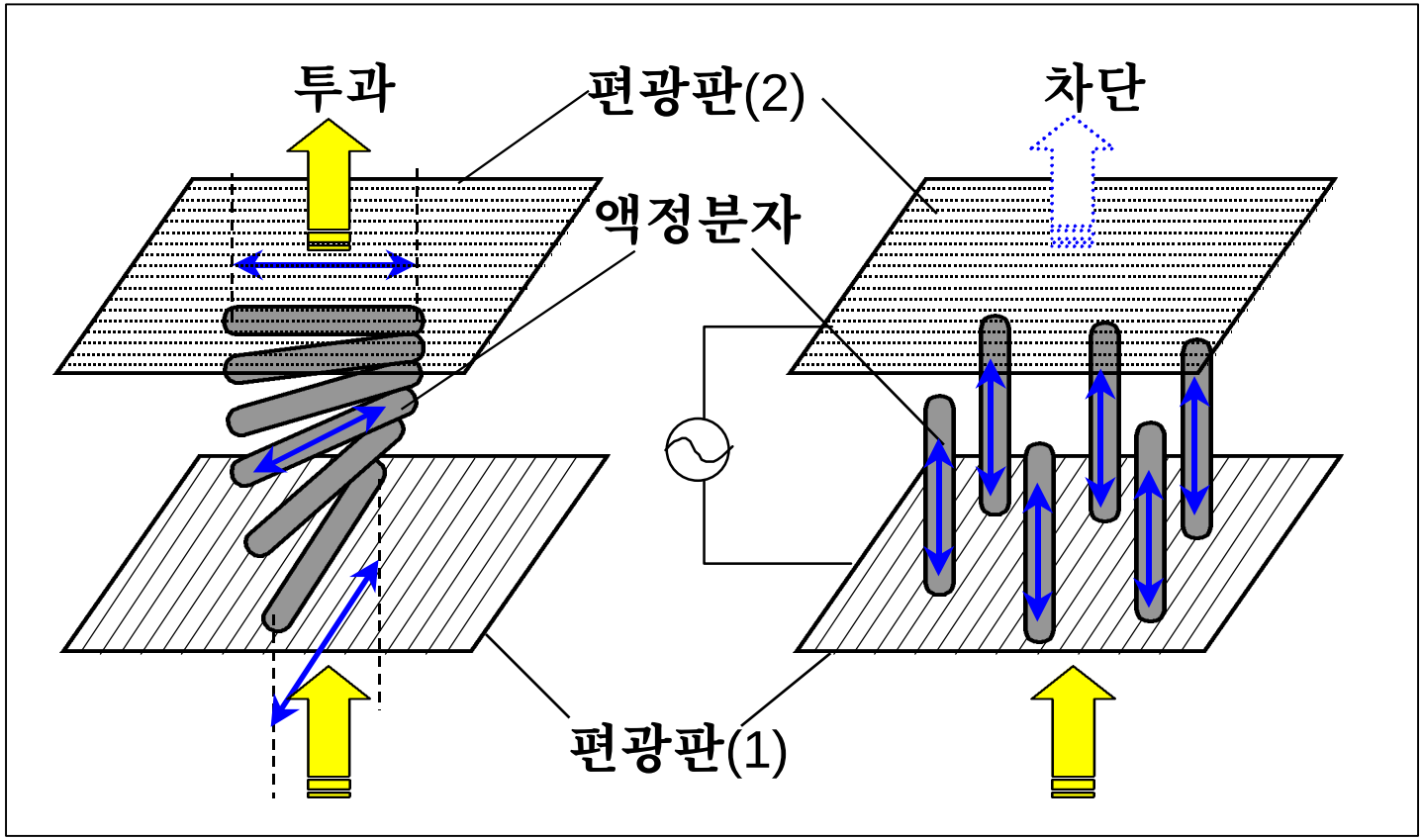
7.3.3 Color 표현방법

7.3.4 LCD의 표시성능

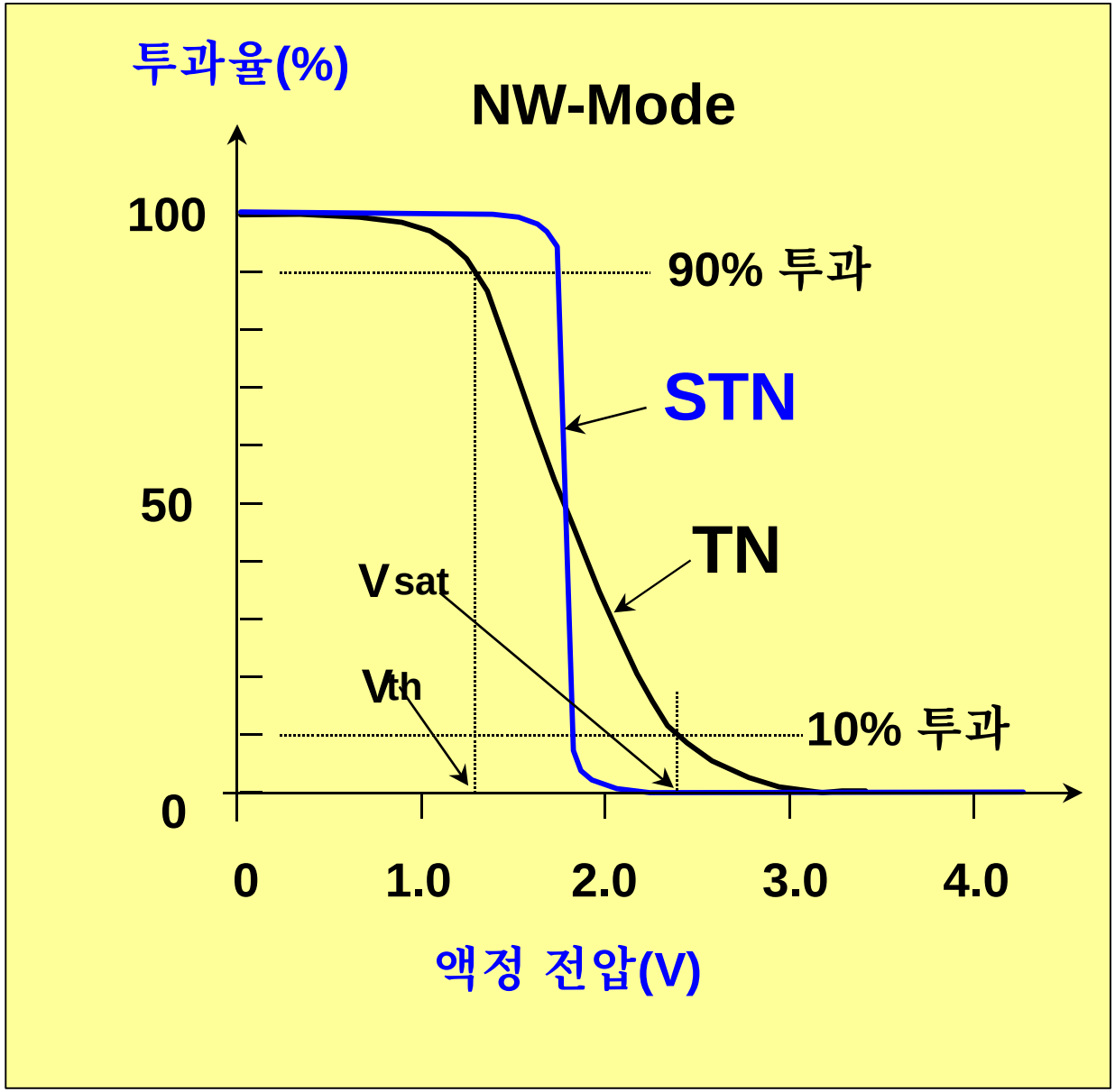
NW-Mode TN Cell의 동작

NW-Mode

- Higher C/R, True Black
- Less Cell Gap Dependent



액정 Cell의 V-T 특성



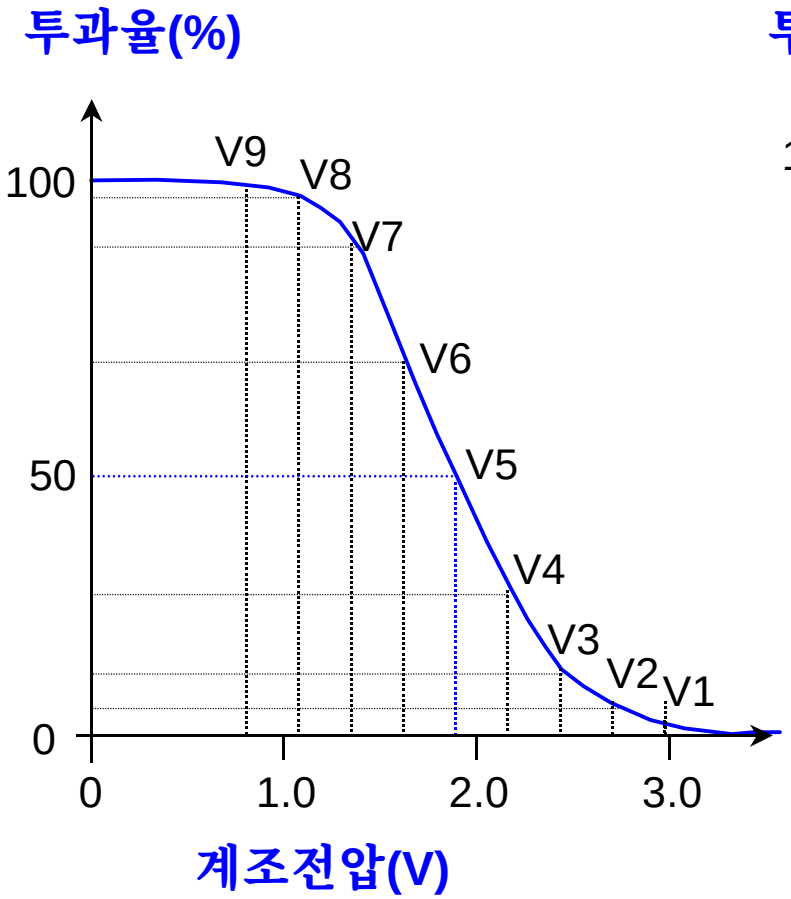
STN vs. TN

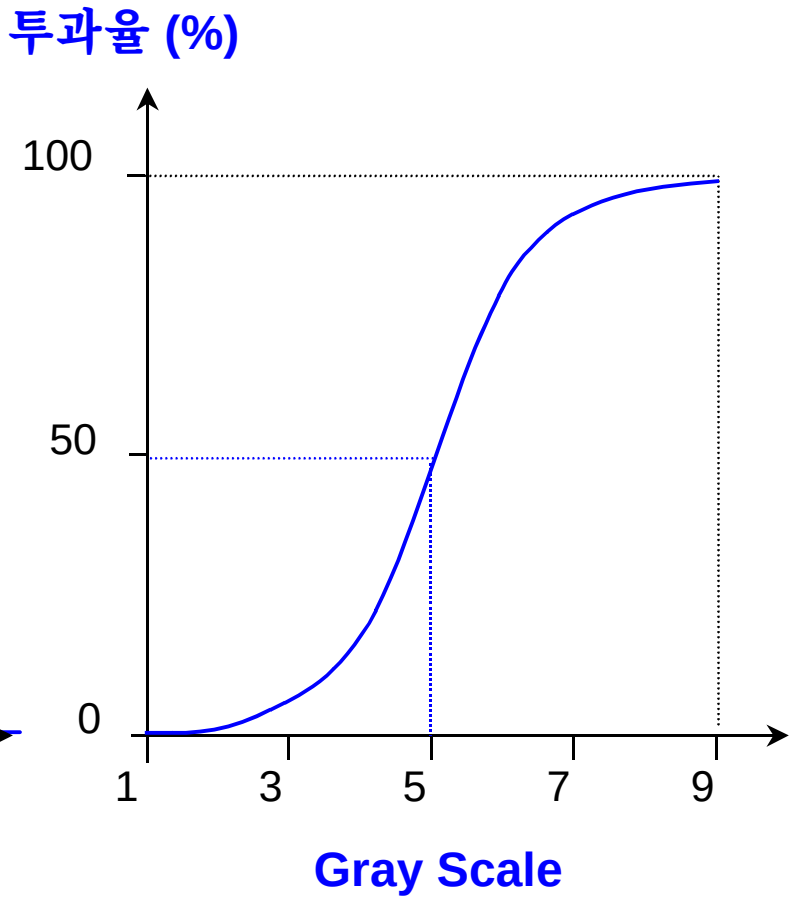
Gray Scale
급준성
Multiplex, 시분할 구동

Vth: Threshold Voltage
Vsat: Saturation Voltage

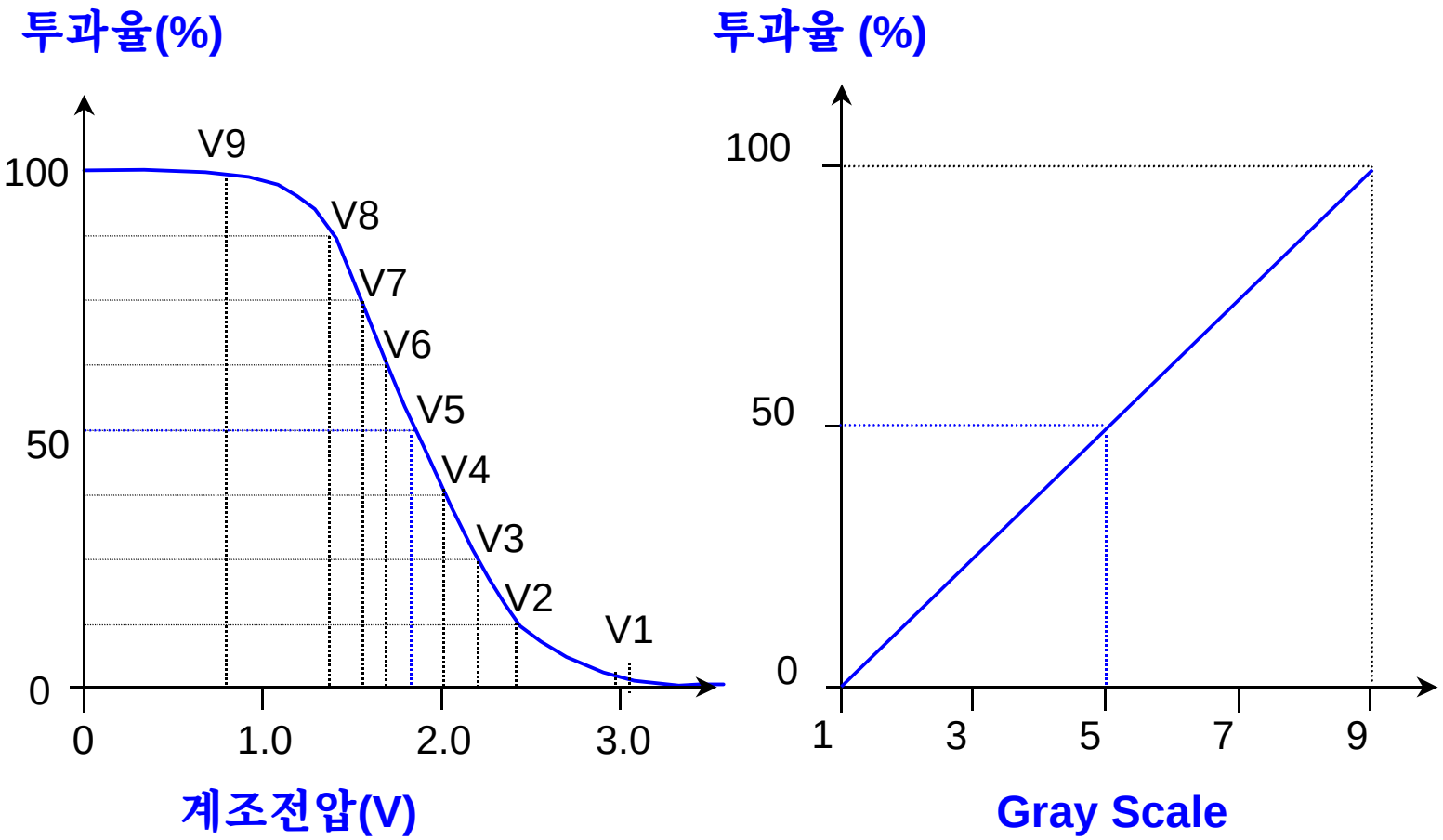
Dynamic Range & 소비전력

등간격 계조전압 투과율 특성



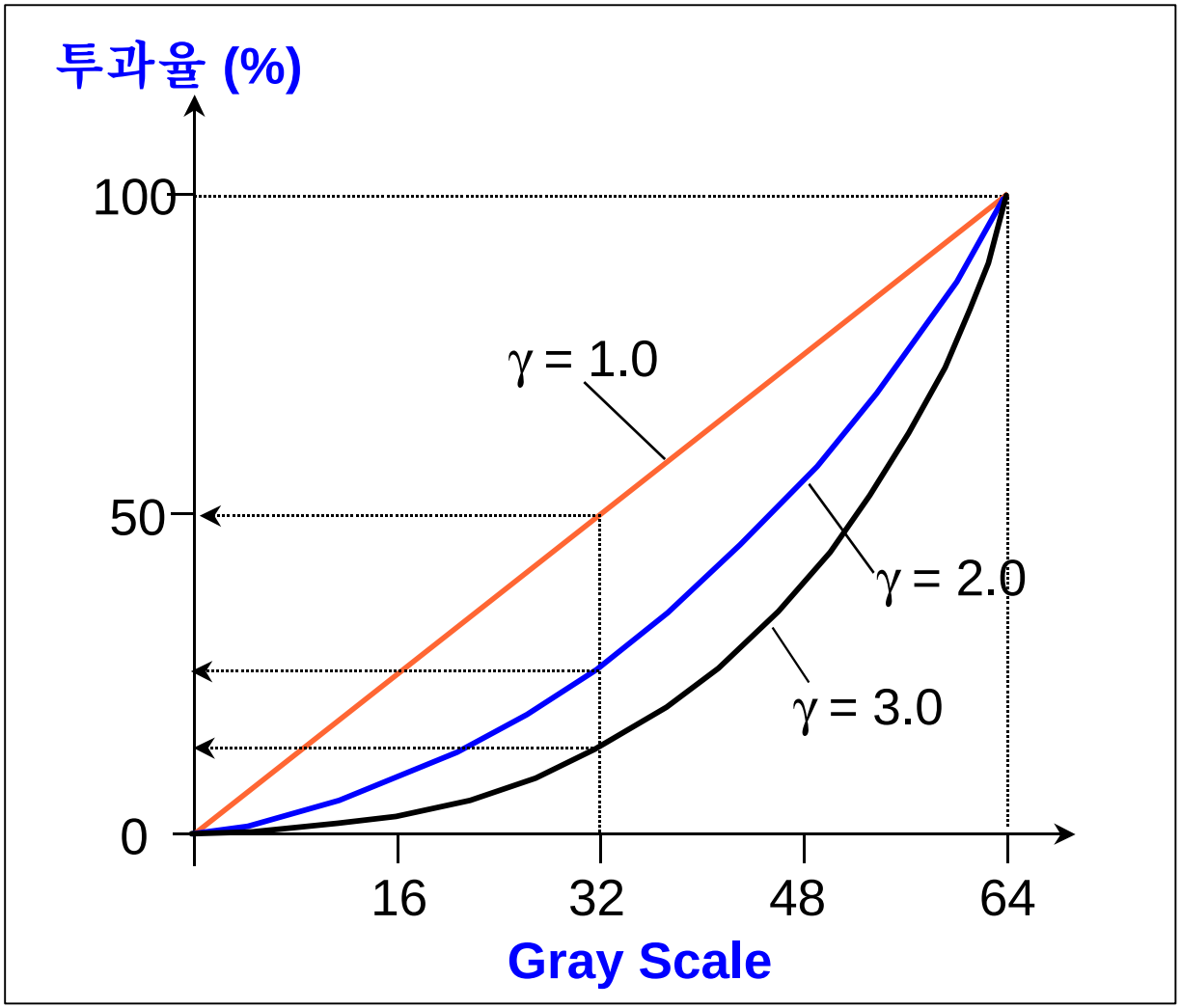


등간격 투과율 설정


투과율(%)
100
50
0
V9
V8
V7
V6
V5
V4
V3
V2
V1
0
1.0
2.0
3.0
계조전압(V)
투과율 (%)
100
50
0
1
3
5
7
9
Gray Scale

g -Correction & Gray Scale

$$T = T_{max} \times (\text{gray \#} / \text{Max. Gray})^{\gamma}$$



- **視感覺 特性**

  어두운 빛 & 밝은 빛 구분

7.3 Color TFT-LCD의 동작원리

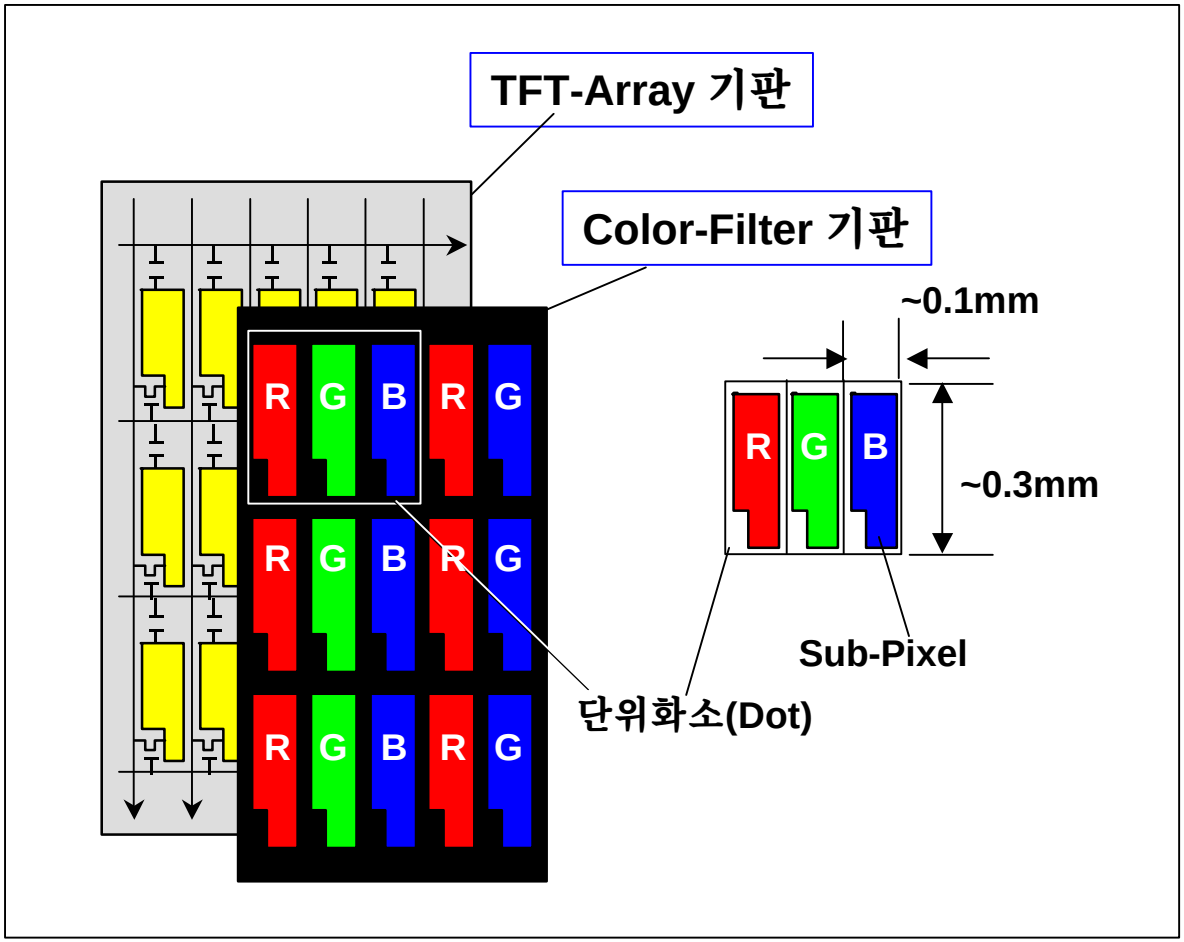
7.3.1 TFT-Array의 구성 및 동작원리

7.3.2 중간계조 표현방법

7.3.3 Color 표현방법

7.3.4 LCD의 표시성능

Color 표현방법



Primary Colors

- Red (R)
- Green(G)
- Blue(B)

A color = rR + gG + bB

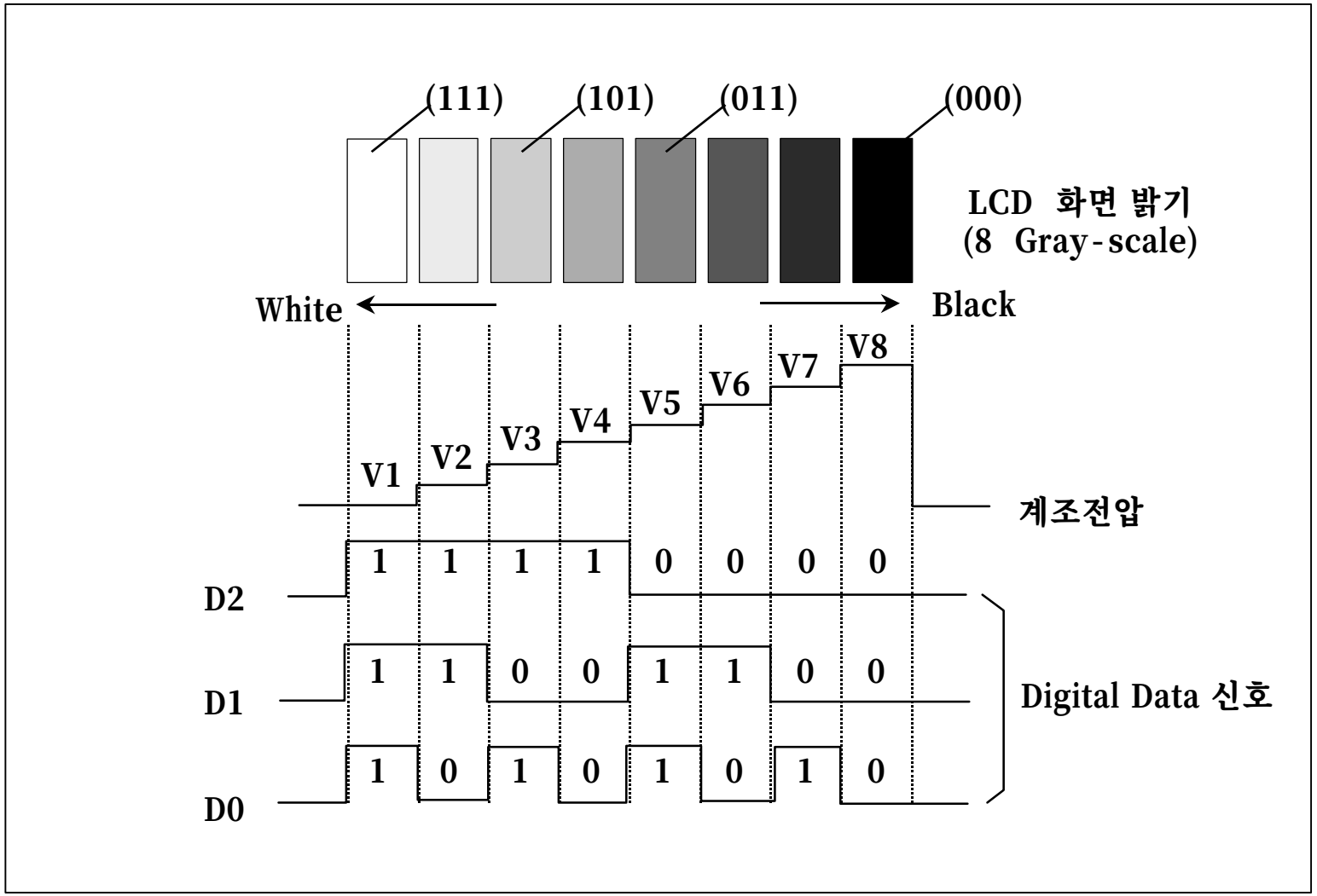
- r = R /(R + G + B)
- g = G /(R + G + B)
- b = B /(R + G + B)

r + g + b = 1

- 視覺 特性/분해능
- Color Blance/Real White
- Color Temperature(색온도)
- Color Coordinates(색좌표)

(r, g, b) ⇨ (x, y)

3-bit LDI를 이용한 8단계 Gray Scale 표현



Gray Scale & Color 표현

$$\#\ \text{of Color} = 2^{n}(R) \times 2^{n}(G) \times 2^{n}(B) = 2^{3n}$$

n= Source Driver IC의 bit 수

3 bit = 8-gray/RGB = 512 colors

4 bit = 16-gray/RGB = 4,096 colors

6 bit = 64-gray/RGB = 262,144 colors

8 bit = 256-gray/RGB = 16,777,216 colors

Analog IC = Continuous gray scale = full color

7.3 Color TFT-LCD의 동작원리

7.3.1 TFT-Array의 구성 및 동작원리

7.3.2 중간계조 표현방법

7.3.3 Color 표현방법

7.3.4 LCD의 표시성능

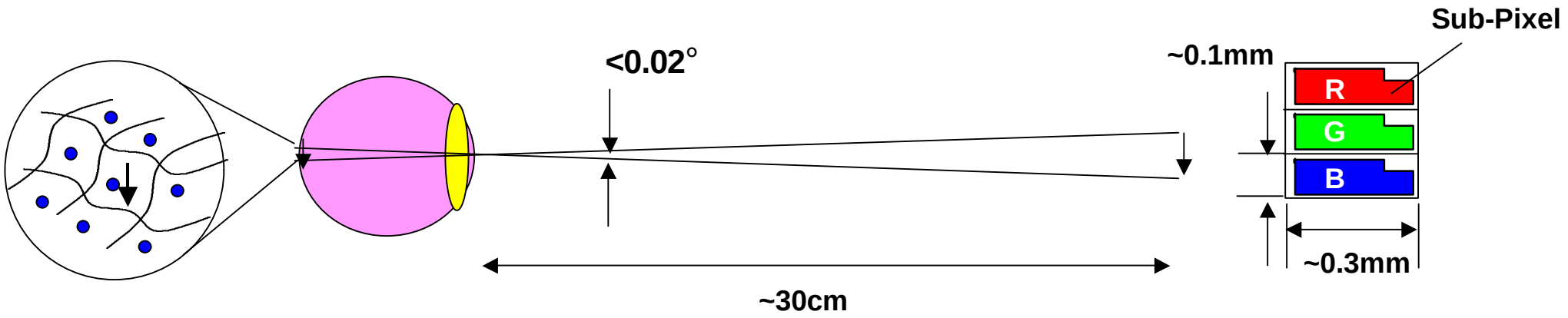
TFT-LCD 해상도

구분	해상도	Dot 수	Pixel 수	화면비	표준화
1	320 x 240	76,800	230,400	4:3	Quarter VGA
2	640 x 400	256,000	768,000	16:10	EGA
3	640 x 480	307,200	921,600	4:3	VGA
4	800 x 480	384,000	1,152,000	15:9	Wide VGA
5	800 x 600	480,000	1,440,000	4:3	SVGA
6	1024 x 600	614,400	1,843,200	~17:10	Wide SVGA
7	1024 x 768	786,432	2,359,296	4:3	XGA
8	1280 x 1024	1,310,720	3,923,160	5:4	SXGA
9	1400 x 1050	1,470,000	4,410,000	4:3	SXGA+
10	1600 x 1200	1,920,000	5,760,000	4:3	UXGA
11	1920 x 1080	2,073,600	6,220,800	16:9	HDTV
12	1920 x 1200	2,304,000	6,912,000	16:10	Wide UXGA
13	2048 x 1536	3,145,728	9,437,184	4:3	QXGA
14	3200 x 2400	7,680,000	23,040,000	4:3	QUXGA

Unit Pixel 크기

dpi : dot per inch

(a) 10.4인치 VGA : 0.3300mm (110.0μm x 330.0μm), 77.0 *dpi*
(b) 12.1인치 SVGA : 0.3075mm (102.5μm x 307.5μm), 82.6 *dpi*
(c) 14.1인치 XGA : 0.2795mm (93.0μm x 279.0μm), 90.9 *dpi*
(d) 15.0인치 SXGA+: 0.2175mm (72.5μm x 217.5μm), 116.8 *dpi*
(e) 17.0인치 SXGA : 0.2700mm (90.0μm x 270.0μm), 94.1 *dpi*
(f) 21.3인치 UXGA : 0.2700mm (90.0μm x 270.0μm), 94.1 *dpi*



7.4 TFT-LCD의 Design Simulation

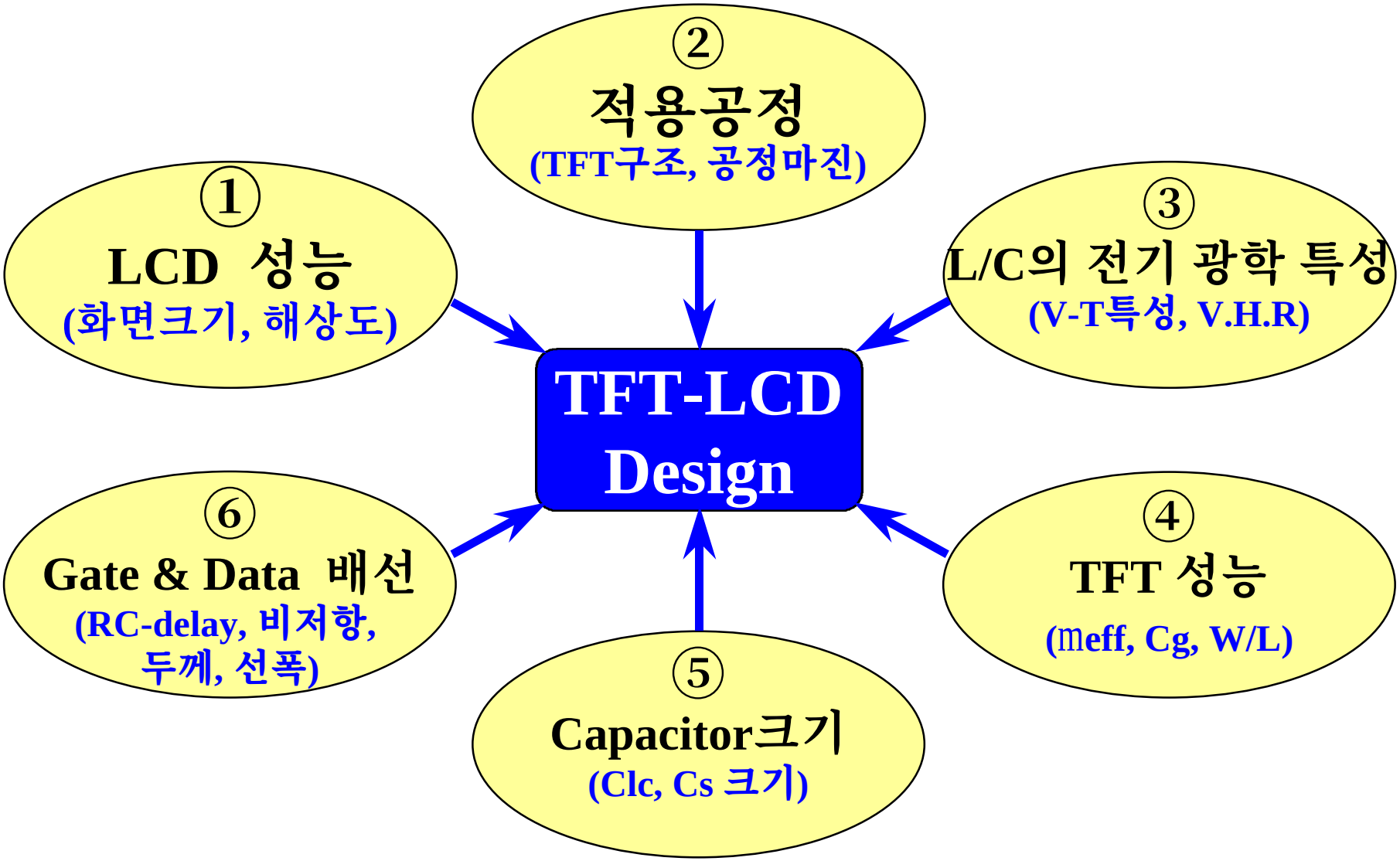
7.4.1 단위화소의 동작특성

7.4.2 TFT의 I-V 특성과 동작 Simulation

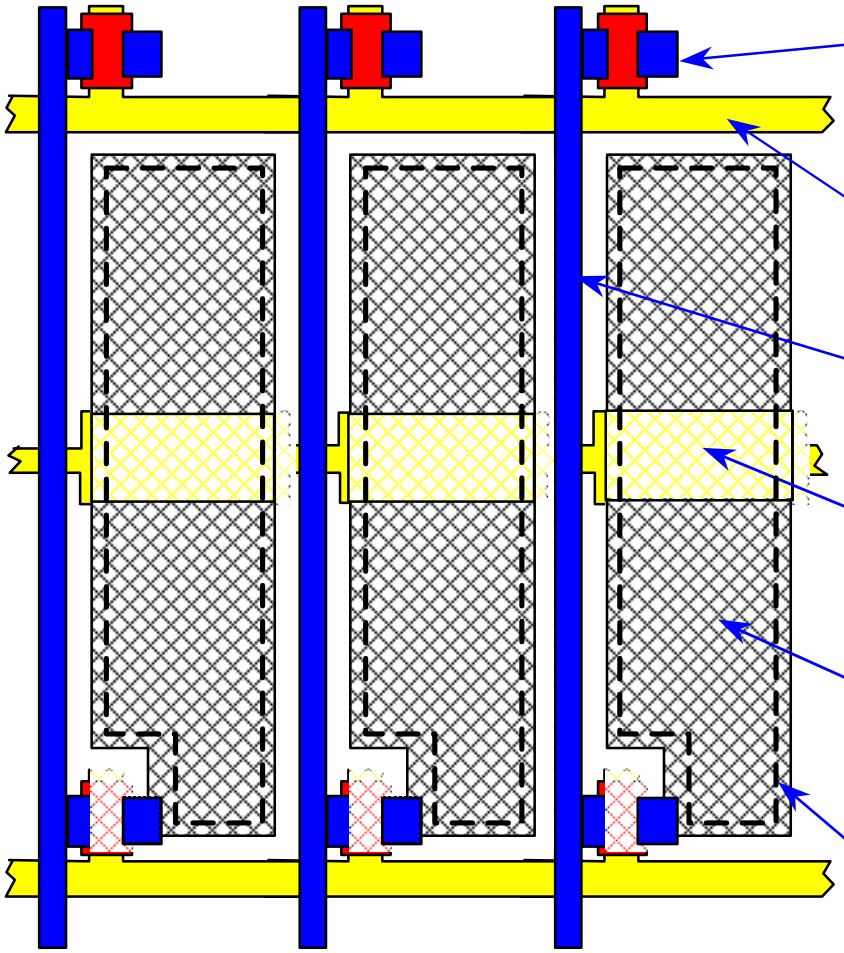
7.4.3 누설전류와 축적용량의 최적화

7.4.4 신호지연과 신호배선의 최적화

TFT-Array의 Design Parameters



TFT-LCD Array 설계 Parameters



① TFT
(구조, W/L, 크기)

② Gate 배선
(두께, 선폭)

③ Data 배선
(두께, 선폭)

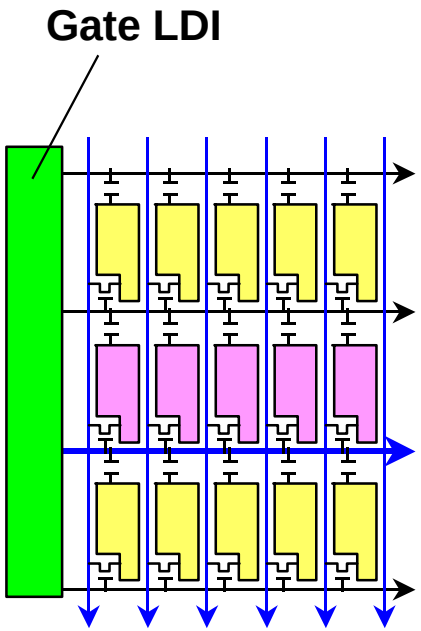
④ 축적용량
(구조, 전극 크기)

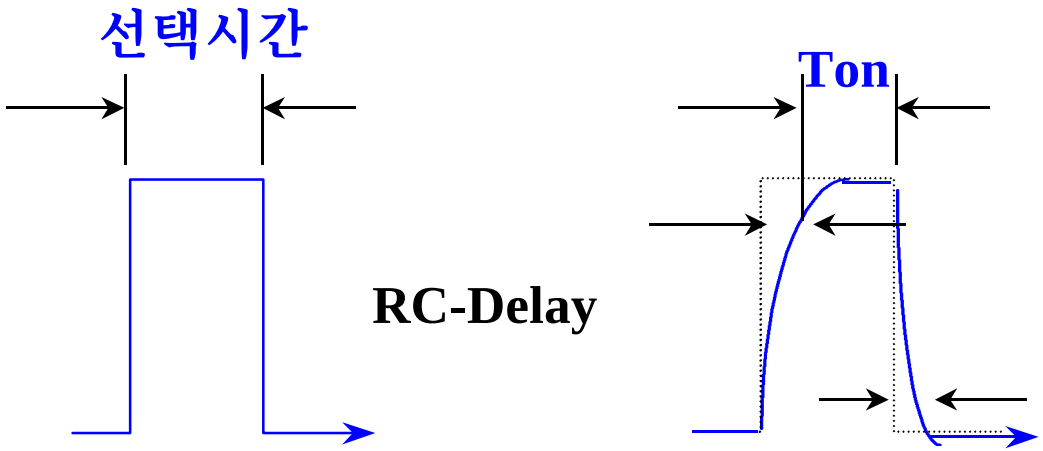
⑤ 화소전극
(ITO 크기, 배선 간격)

⑥ Black Matrix (CF기판)
(Aperture 크기, Align 마진)

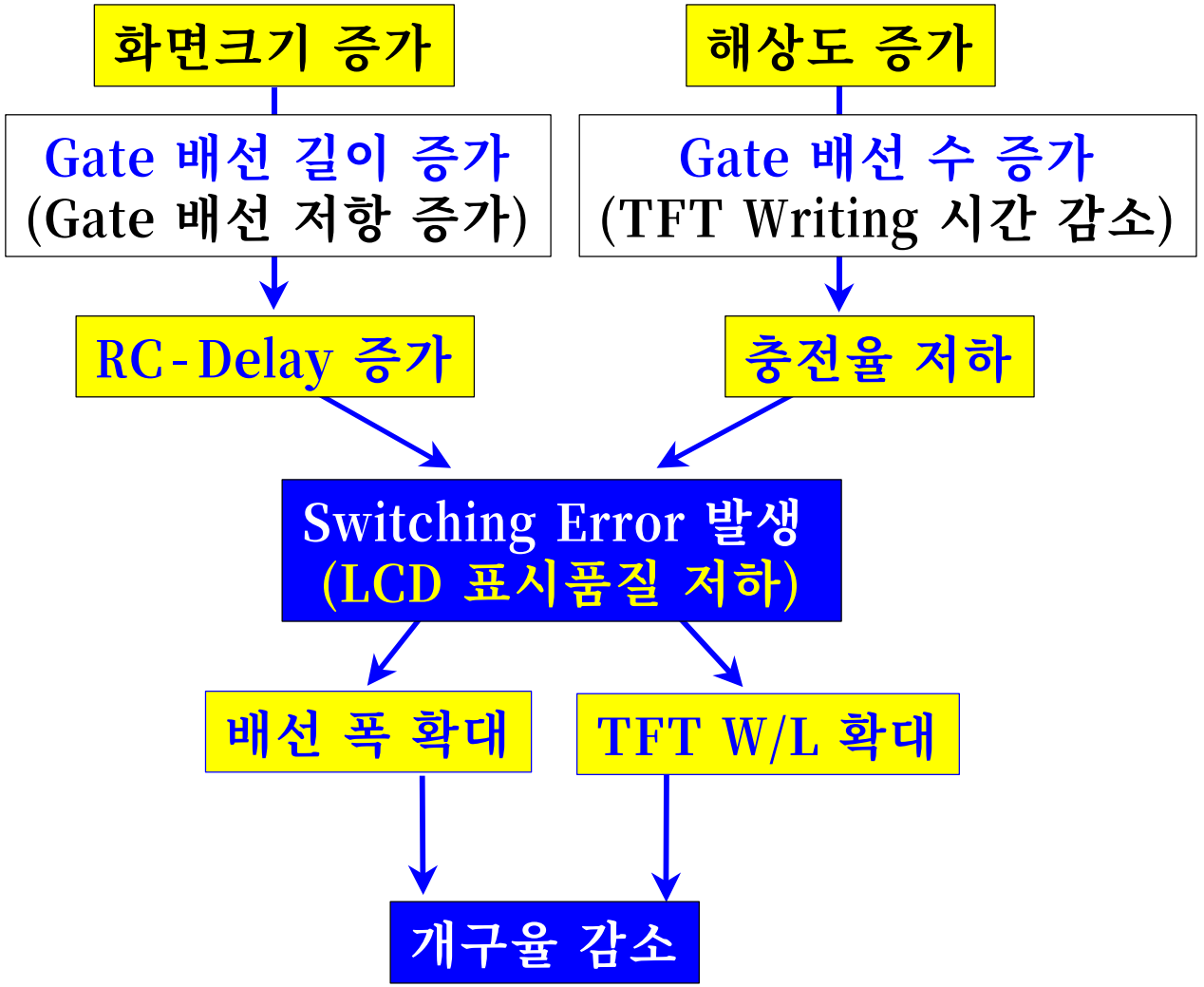
해상도별 Gate 신호배선 수 & 선택시간

해상도	화소배열	Gate신호배선	선택시간(60 frame/s)	화면 크기(예)
VGA	640 x 480	480개	34 ㎲ 이하	9.4", 10.4"
SVGA	800 x 600	600 개	27 ㎲ 이하	10.4", 12.1"
XGA	1024 x 768	768 개	21 ㎲ 이하	14.1", 15.0"
SXGA	1280 x 1024	1,024 개	16 ㎲ 이하	17.0", 18.1"
UXGA	1600 x 1200	1,200 개	13 ㎲ 이하	21.3", 30.0"

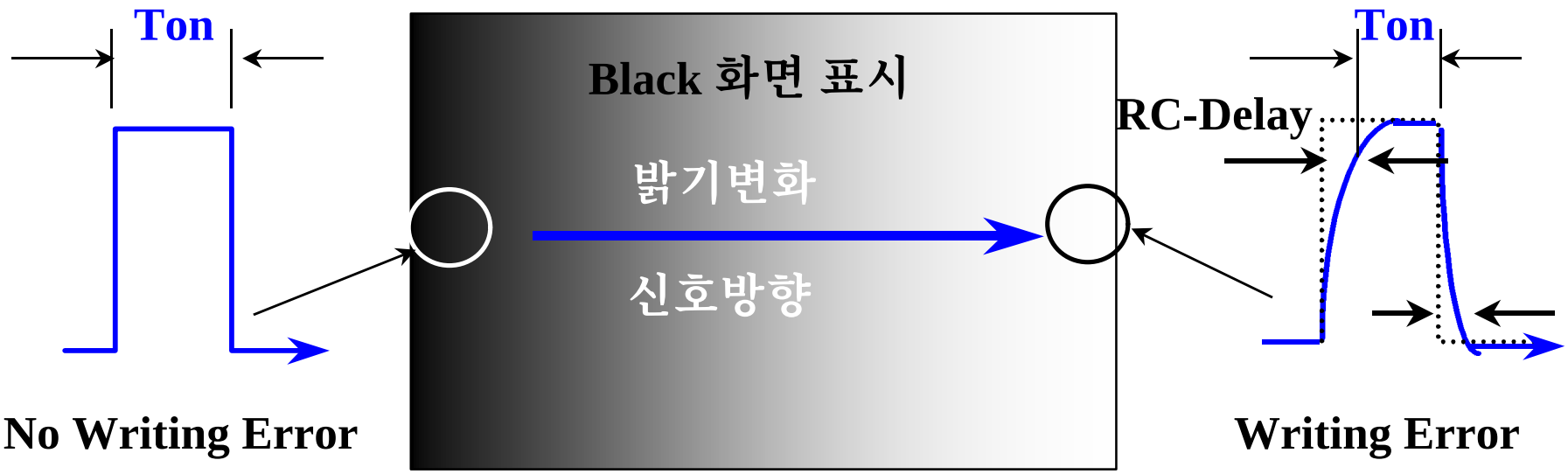




TFT-LCD의 화면 크기와 해상도의 한계



TFT의 Writing Error에 의한 Shading



7.4 TFT-LCD의 Design Simulation

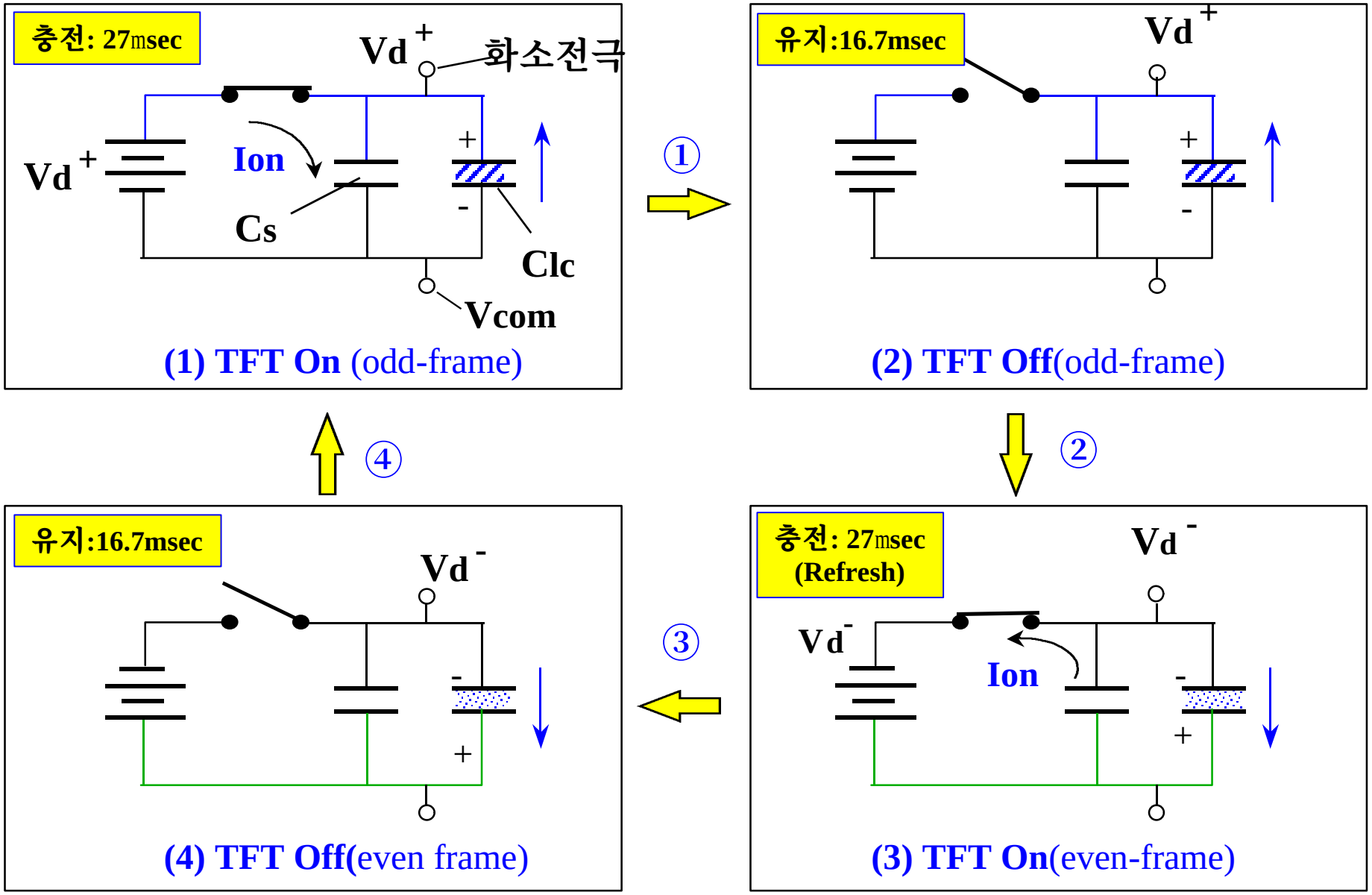
7.4.1 단위화소의 동작특성

7.4.2 TFT의 I-V 특성과 동작 Simulation

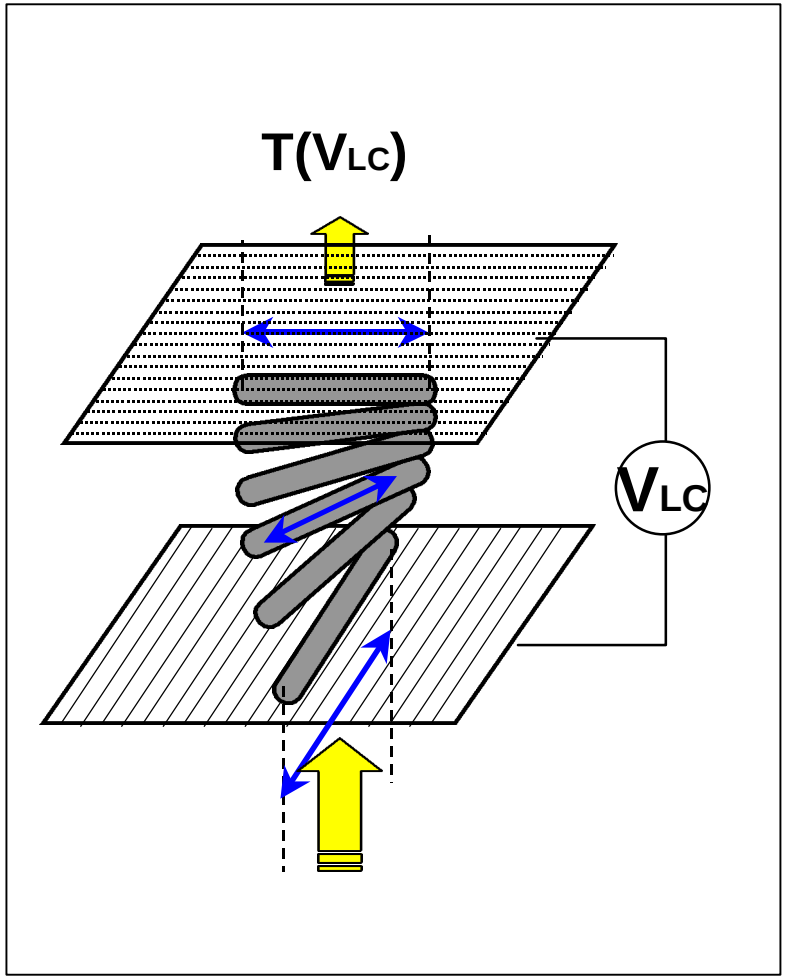
7.4.3 누설전류와 축적용량의 최적화

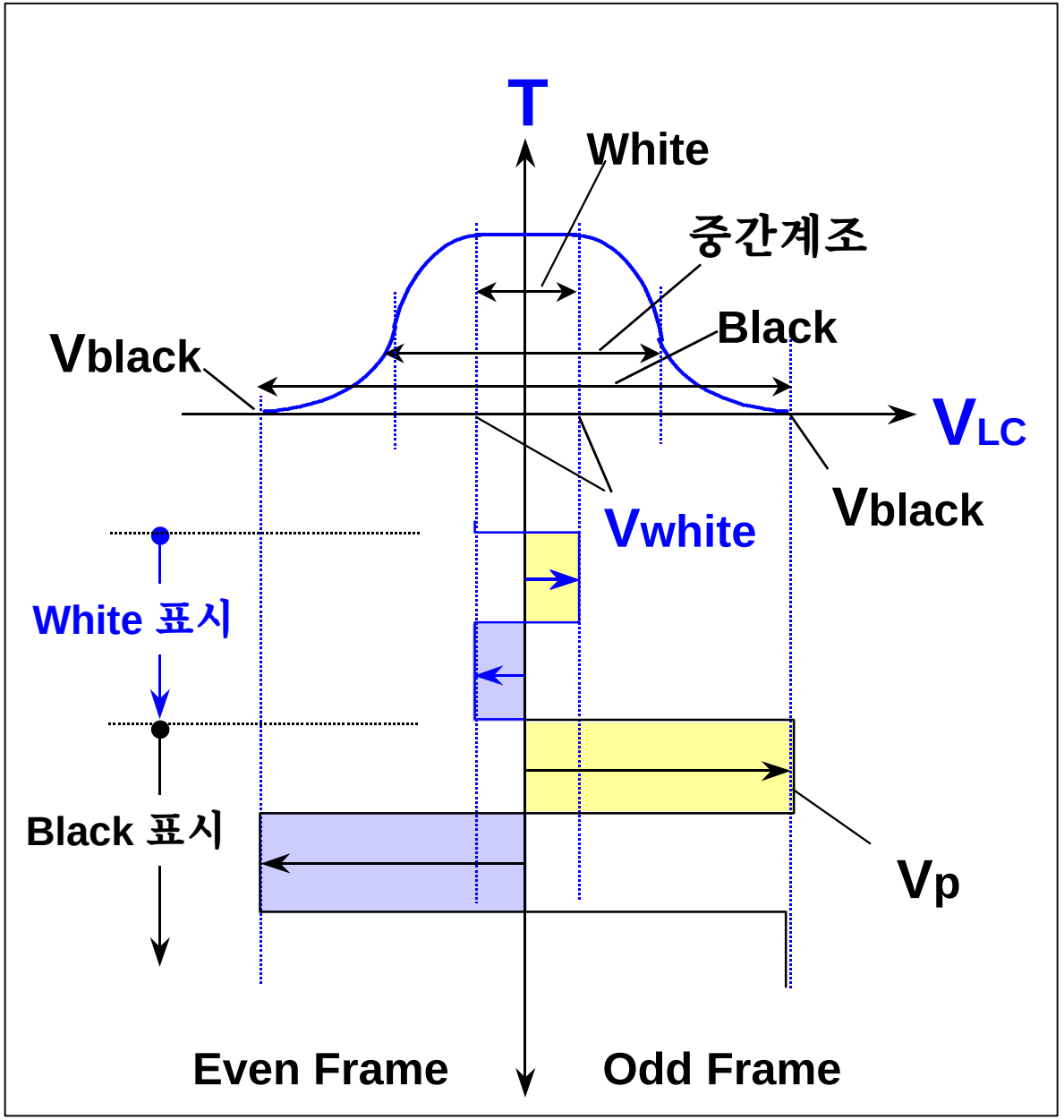
7.4.4 신호지연과 신호배선의 최적화

Switch 작용에 의한 Unit Cell의 동작원리



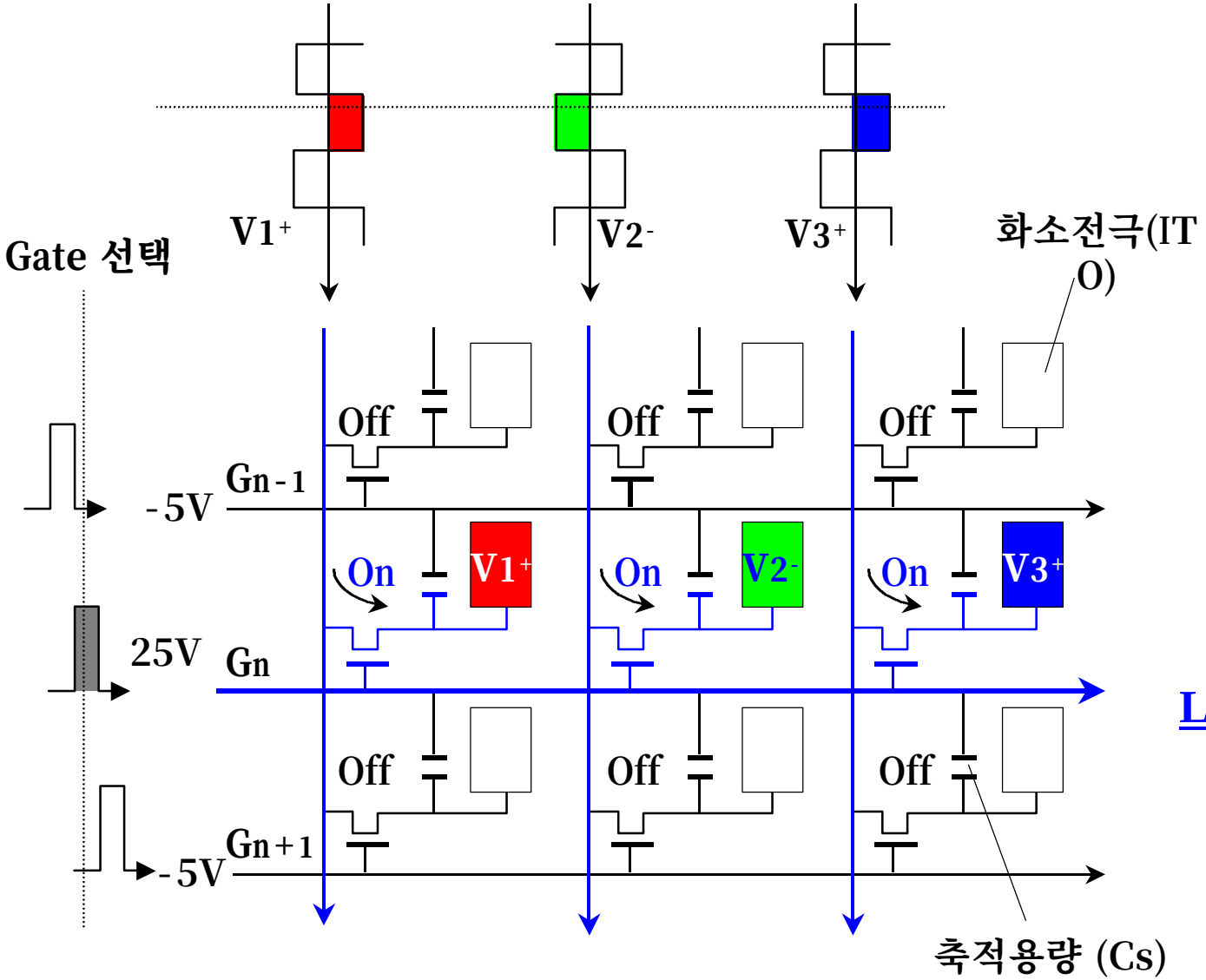
액정 Cell의 교류 동작





TFT-Array의 Active Addressing

(3x3 matrix)

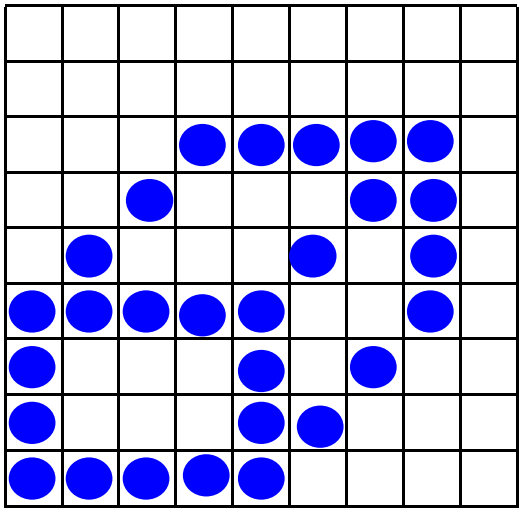


Line-by-Line Addressing

LCD의 Video Data 표현(Digital 구동)

0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	0
0	0	1	0	0	0	1	1	0
0	1	0	0	0	1	0	1	0
1	1	1	1	1	0	0	1	0
1	0	0	0	1	0	1	0	0
1	0	0	0	1	1	0	0	0
1	1	1	1	1	0	0	0	0

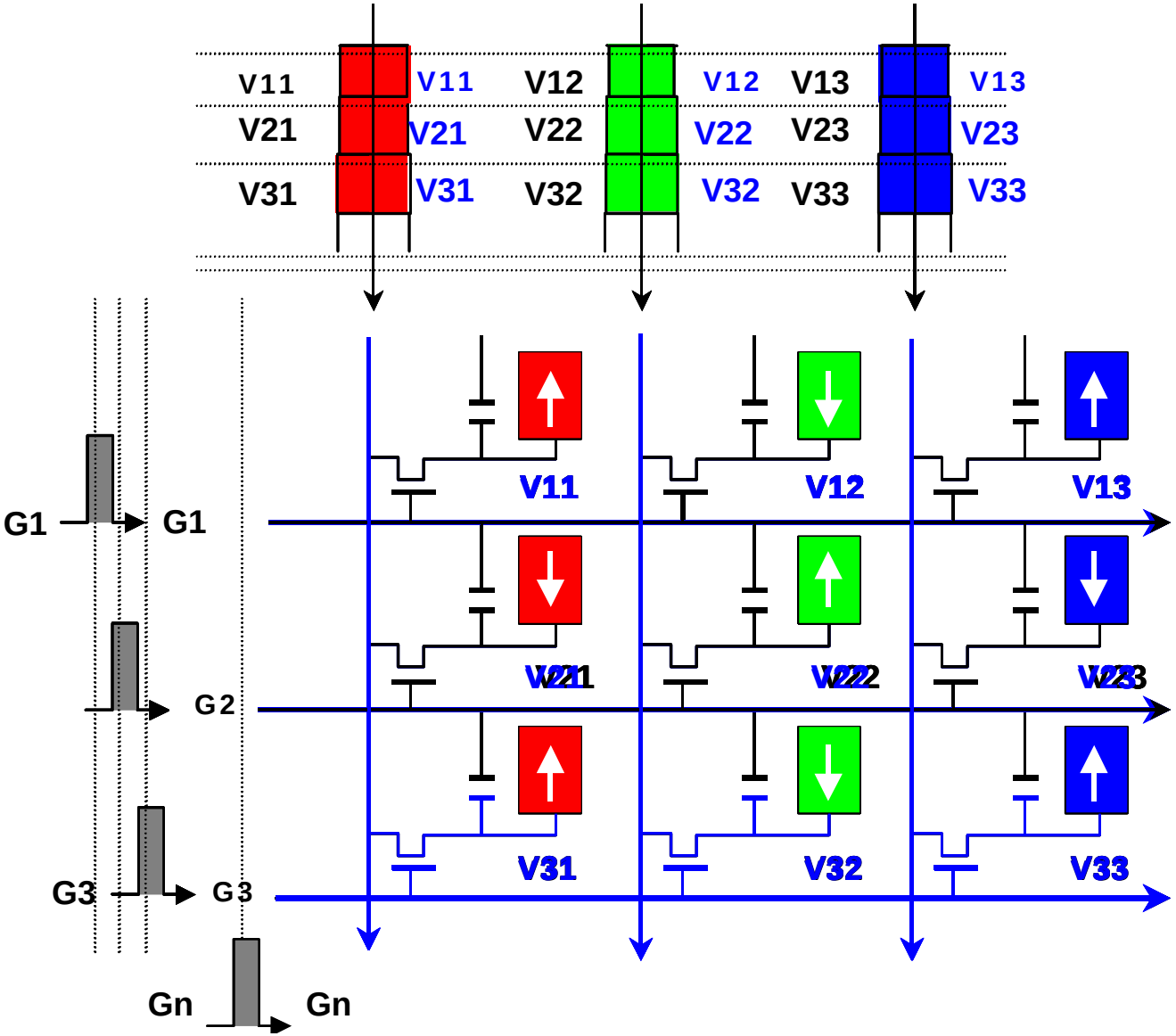
=



Bit Image in Memory

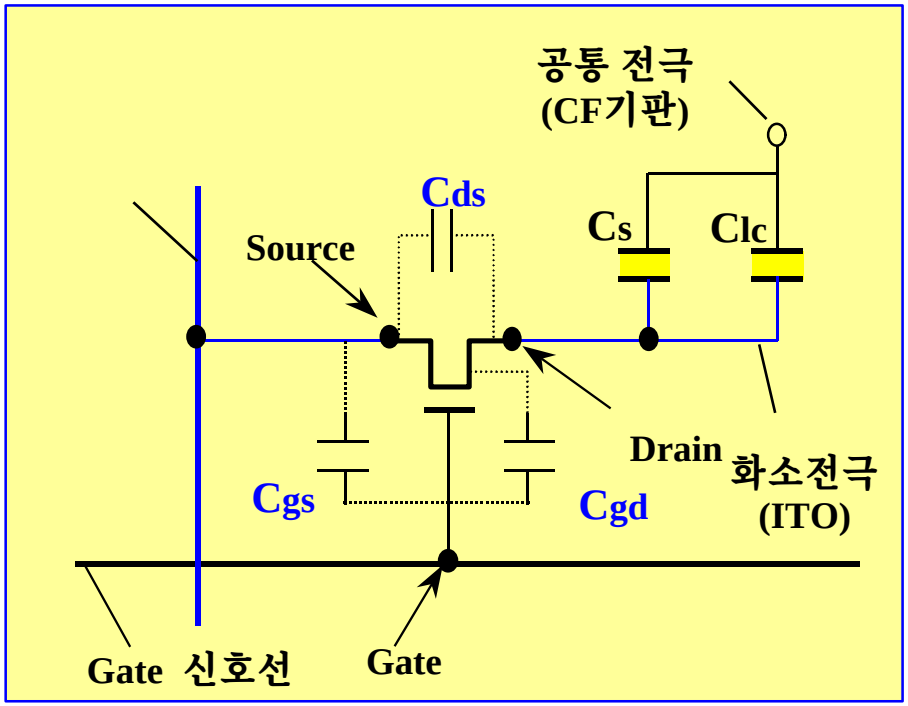
Pixels displayed on Screen

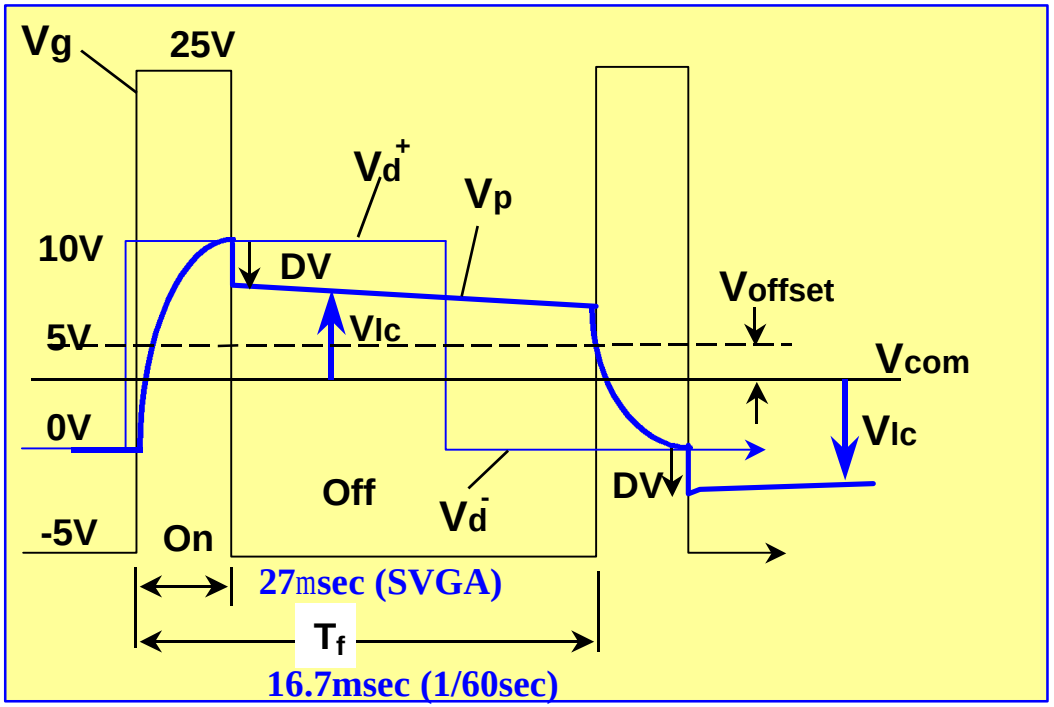
Animation of a (3x3) Matrix Operation



Even Frame

TFT의 기생용량 & Unit 화소의 동작 전압 파형

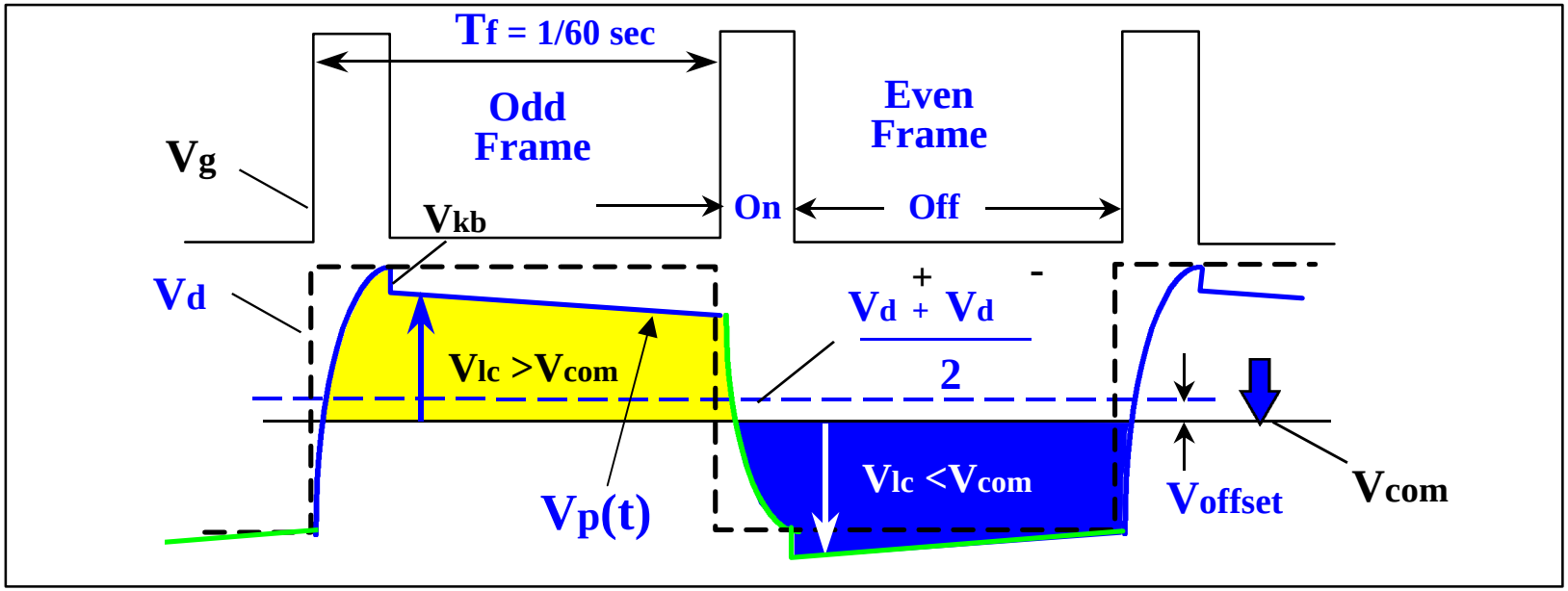




$$DV = \frac{C_{gd}}{\{C_{lc} + C_s + C_{gd}\}} \times V_{p\text{-}p} \quad \text{----} \quad (7.4.1)$$

$$\Delta V = \frac{C_{gd}(on)}{C_{lc}(V_d) + C_s + C_{gd}(off)} \times V_{p\text{-}p} - \frac{C_{gd}(on) - C_{gd}(off)}{C_{lc}(V_d) + C_s + C_{gd}(off)} \times (V_d + V_{th}) \qquad (7.4.4)$$

액정 Cell의 실효전압



$$\langle Vlc \rangle eff = \frac{1}{2\,Tf} \sqrt{\int_{t=0}^{2Tf} \{ Vp(t) - Vcom \}^2 dt} \qquad \text{---- (7.4.2)}$$

$$Voffset = \frac{Vd^{+} + Vd^{-}}{2} - Vcom \quad \Rightarrow \quad \text{DC 성분 보상}$$

7.4 TFT-LCD의 Design Simulation

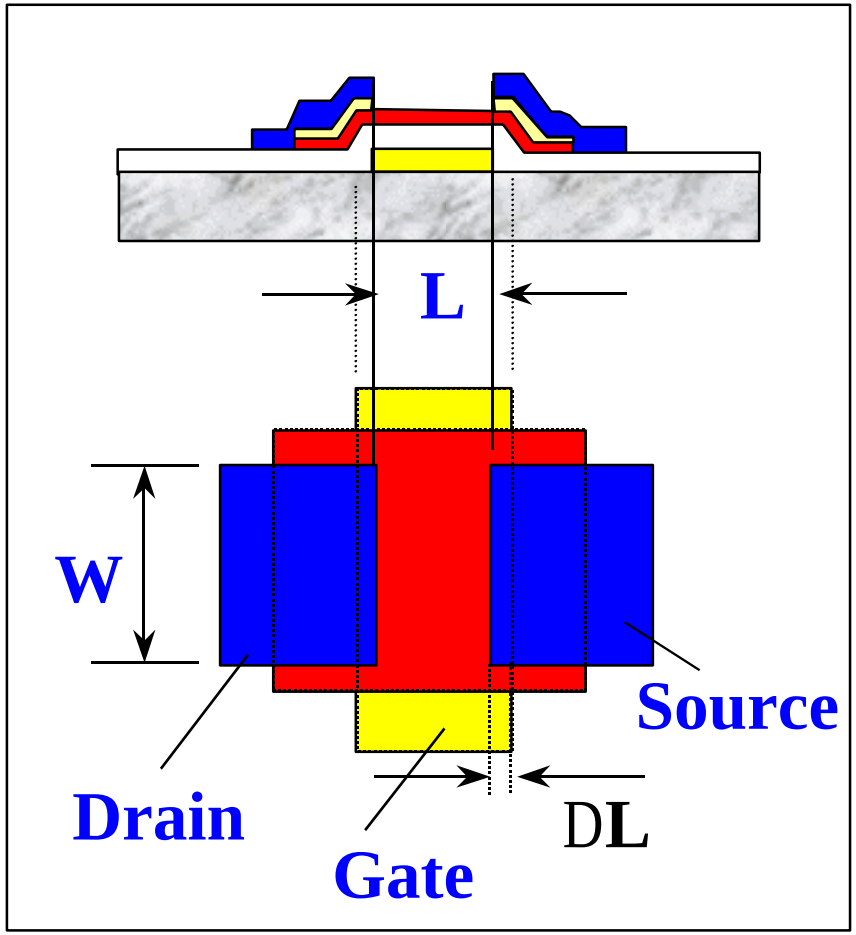
7.4.1 단위화소의 동작특성

7.4.2 TFT의 I-V 특성과 동작 Simulation

7.4.3 누설전류와 축적용량의 최적화

7.4.4 신호지연과 신호배선의 최적화

TFT의 W/L 설계



요구되는 전류이득 K 의 확보

$$K = (1/2)\ \mu_{eff}\ C_g\ (W/L)$$

MASK 설계

공정 변수

μ_{eff} : 전계효과 이동도

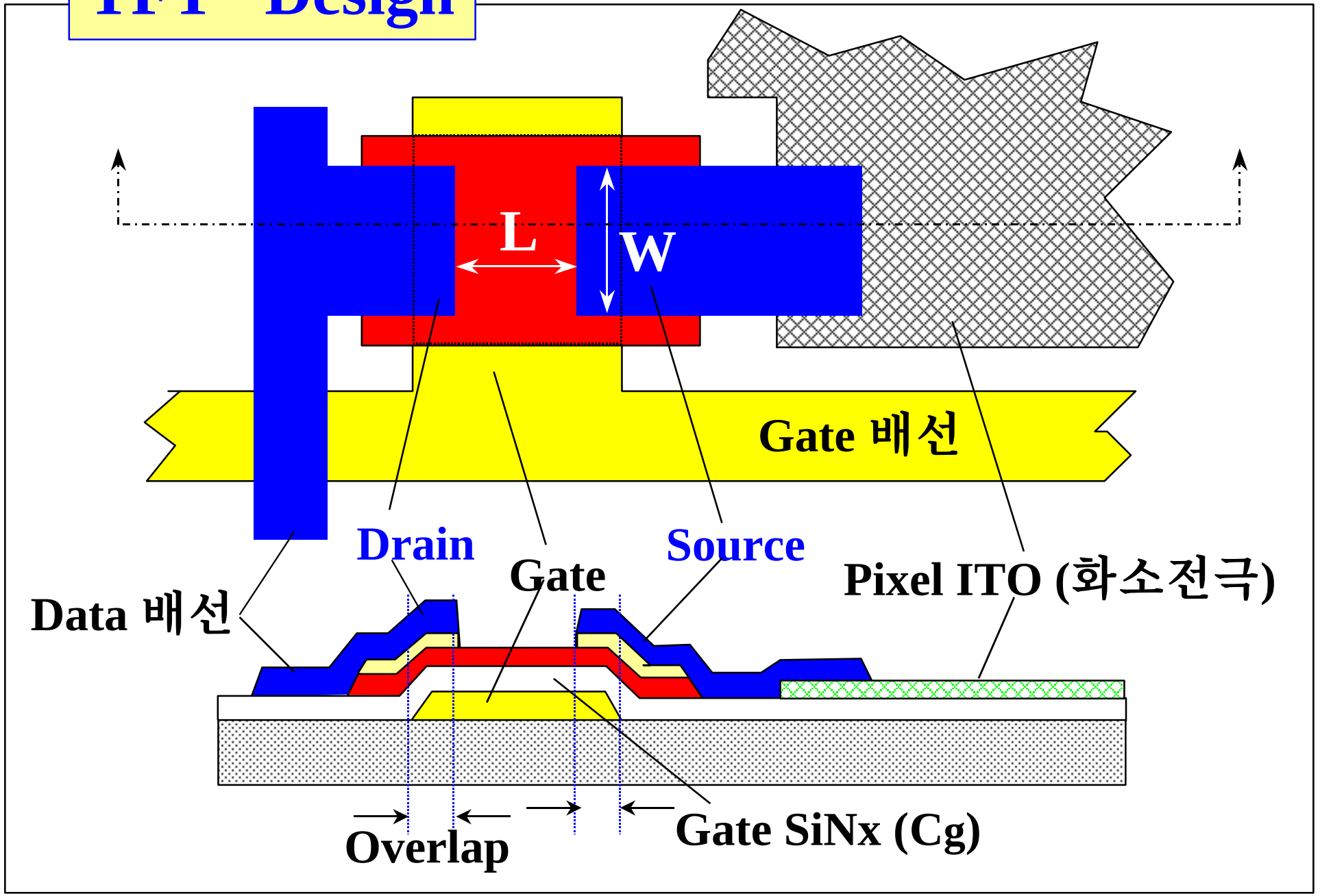
Typ. : 0.5 ~1.0 cm^2/ V-sec

Cg : 단위 면적 당 Gate 정전용량

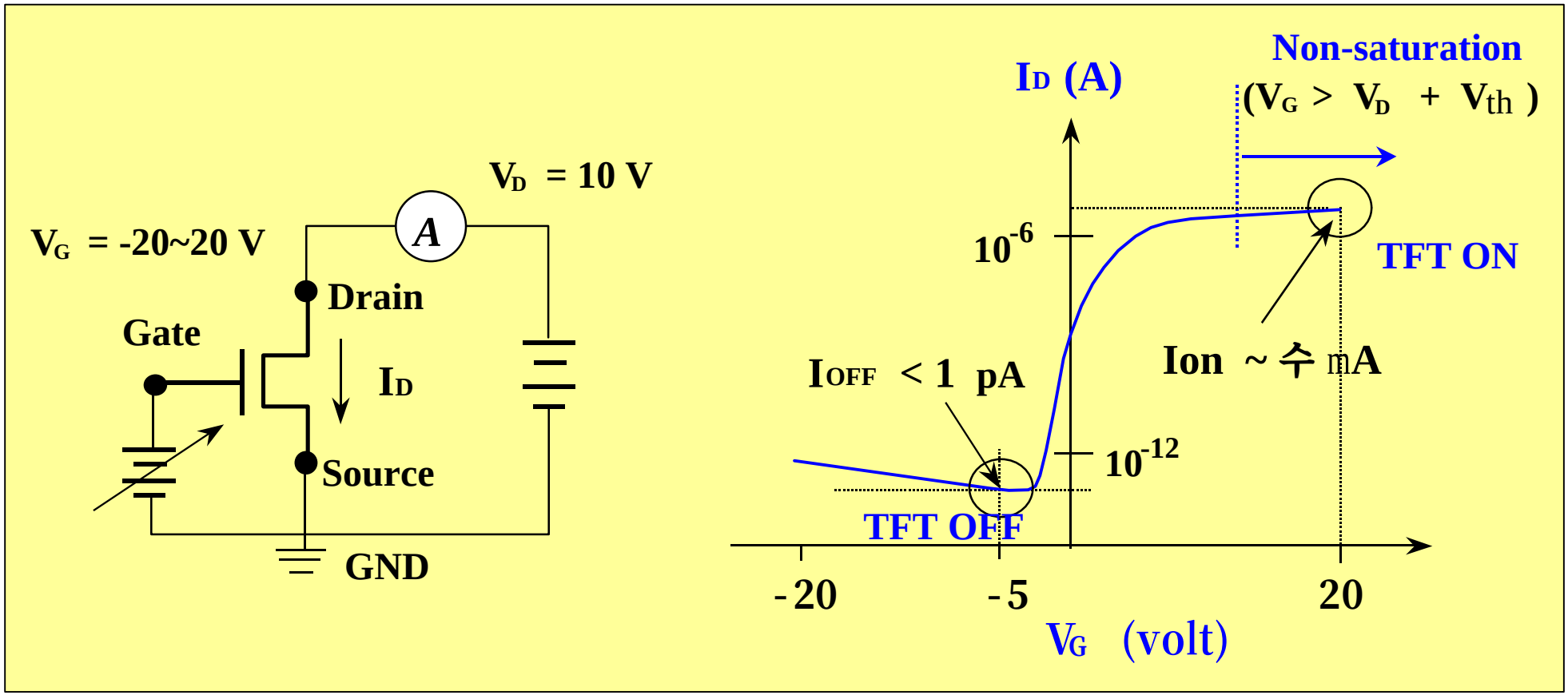
TFT Design Parameters: (W, L의 결정)

①전류이득(K), ② CD, ③Aligner 정도, ④개구율(TFT 크기)

TFT Design


L
W
Gate 배선
Drain
Source
Gate
Pixel ITO (화소전극)
Data 배선
Overlap
Gate SiNx (Cg)

TFT의 전류-전압(I-V) 특성과 측정방법

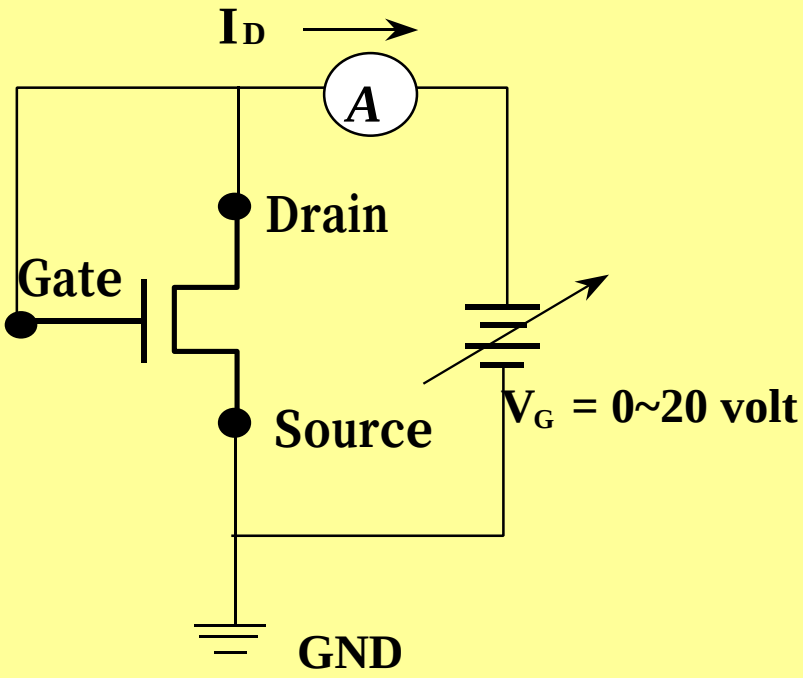


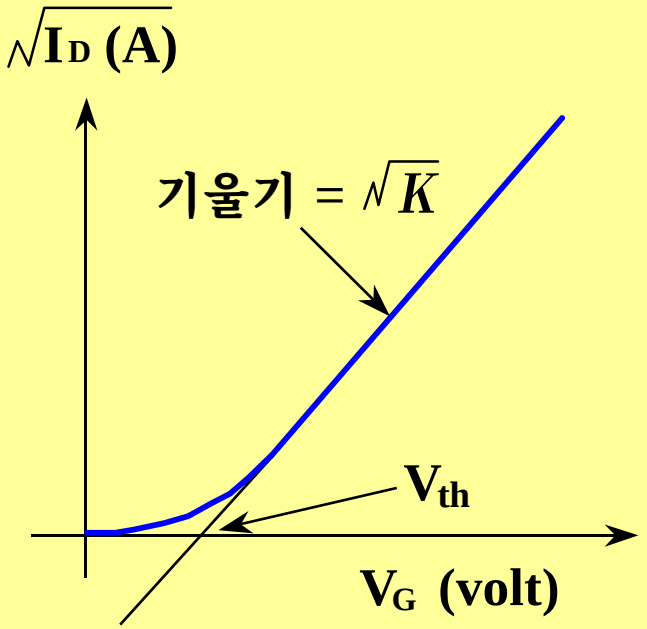
Non-saturation Condition

(V_G > V_D + V_{th})

$$I_d = K\left\{2\left(V_G - V_{th}\right) - V_D\right\} V_D \qquad (7.4.5)$$

TFT의 전류 구동능력(K) 측정방법





Saturation Condition

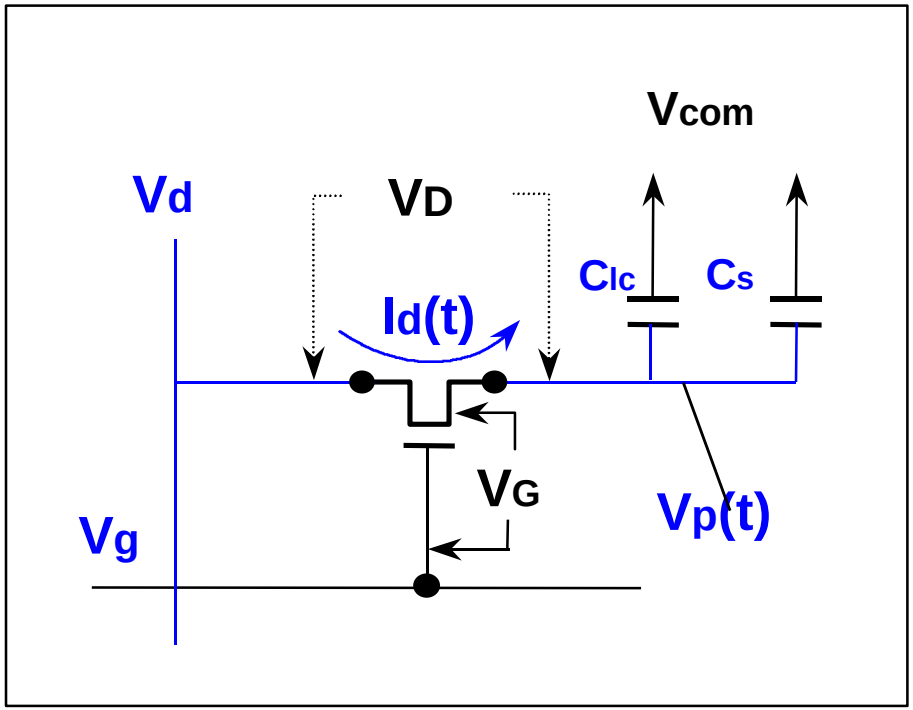
($V_G < V_D + V_{th}$)

$$I_d = K\left(V_G - V_{th}\right)^2 \qquad (7.4.6)$$

$$K = \frac{1}{2} m_{eff} C_g \frac{W}{L} \qquad (7.4.7)$$

$$\sqrt{I_d} = \sqrt{K}\left(V_G - V_{th}\right)$$

$$I_d = K\left\{2\left(V_G - V_{th}\right) - V_D\right\} V_D \qquad (7.4.5)$$



$$V_D = V_d - V_p(t)$$

$$V_G = V_g - V_p(t)$$

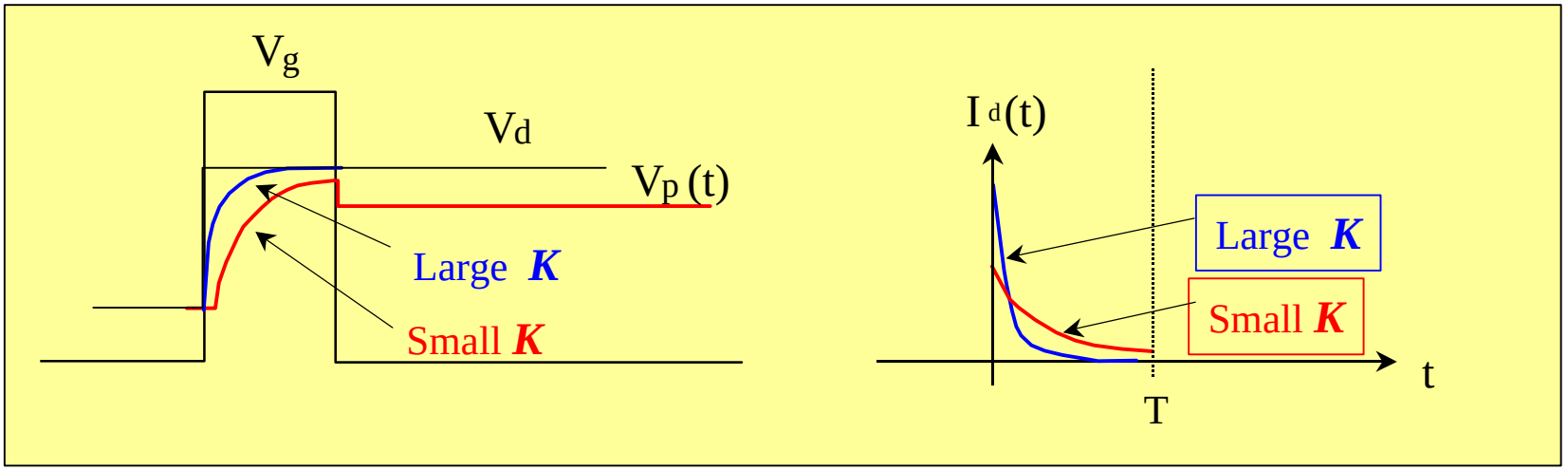
$$I_d(t) = K\left[2\left\{V_g - V_{th} - V_d\right\} + \left\{V_d - V_p(t)\right\}\right] \times \left[V_d - V_p(t)\right] \qquad (7.4.10)$$

$$K = \frac{I_d(t)}{2\left\{V_g - V_{th} - V_d\right\}} \times \left[\frac{1}{V_d - V_p(t)} - \frac{1}{2\left\{V_g - V_{th} - V_d\right\} + \left\{V_d - V_p(t)\right\}}\right] \qquad (7.4.11)$$

$$K = \frac{I_d(t)}{2\left\{V_g - V_{th} - V_d\right\}} \times \left[\frac{1}{V_d - V_p(t)} - \frac{1}{2\left\{V_g - V_{th} - V_d\right\} + \left\{V_d - V_p(t)\right\}}\right] \quad (7.4.11)$$

$$I_d(t) = C_t \times \frac{dV_p(t)}{dt} \quad (7.4.12)\,, \qquad C_t = C_{lc} + C_s$$

$$K = \frac{C_t}{2\left\{V_g - V_{th} - V_d\right\} t} \times Ln\left\{\frac{\left[2\left\{V_g - V_{th} - V_d\right\} + \left\{V_d - V_p(t)\right\}\right] \times \left[V_d - V_p(0)\right]}{\left[2\left\{V_g - V_{th} - V_d\right\} + \left\{V_d - V_p(0)\right\}\right] \times \left[V_d - V_p(t)\right]}\right\} \quad (7.4.13)$$



TFT의 전류구동능력(K) & W/L 설계

Example (SVGA급)

- **충전율=99%**
- **Vth=3.5V**
- **Vd=10V, Vp(0)=0V**
- **Vg=20V**
- **Ct=0.2pF+ 0.3pF**
- **μeff=0.45cm^2/sec-V**
- **Cg =1.06 x 10^{-8} F/cm**

$$K = \frac{1}{2}\, m_{\text{eff}}\, C_g\, \frac{W}{L}$$

$$R_{\text{charge}} = \frac{V_p(T)}{V_d - V_p(0)} \times 100\%$$

Vp(0)=0V 이므로 충전 개시 후 T=27μsec 경과 후 99% 충전 조건:
99% = Vp(T)/{10.0V-0V} ---------> Vp(T)=9.9V

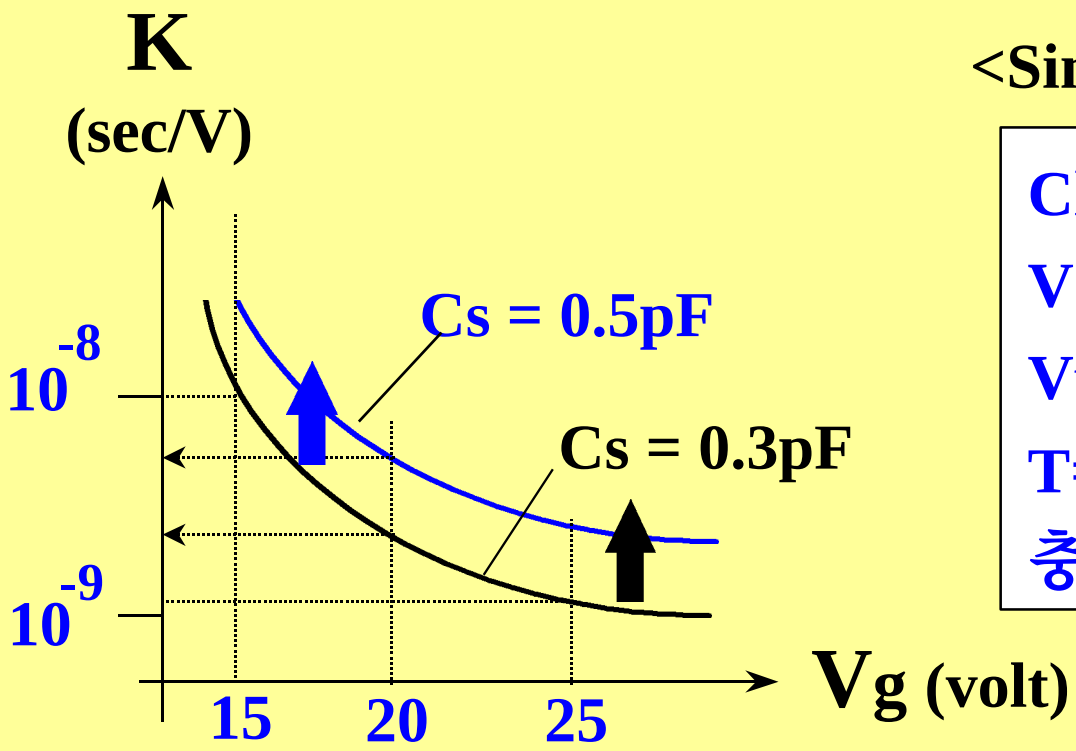
$$K > \frac{0.5pF}{2\{20v - 3.5v - 10v\}\ x27u\sec} \times Ln\left\{ \frac{\left[2\{20v-3.5-10v\}+\{10v-V_p(t)\}\right]\times[10v-0v]}{\left[2\{20v-3.5v-10v\}+\{10v-0v\}\right]\times\left[10v-V_p(t)\right]} \right\}$$

$$K \geq 5.76\times10^{-9}\ \text{sec/volt} \qquad (7.4.15)$$

$$\frac{W}{L} \geq \frac{2K}{m_{\text{eff}}\ C_{g_g}} = \frac{2\times(5.76\times10^{-9}\ \text{sec/v})}{(0.45\ \text{cm}^2/\text{sec}\cdot\text{v})\times(1.06^{-8}\ \text{F/cm})} = 2.42$$

전류 구동능력(K)의 Cs, Vg 의존성

(Design Simulation 예)



<Simulation 조건 >

Clc = 0.2pF

Vd = 10V

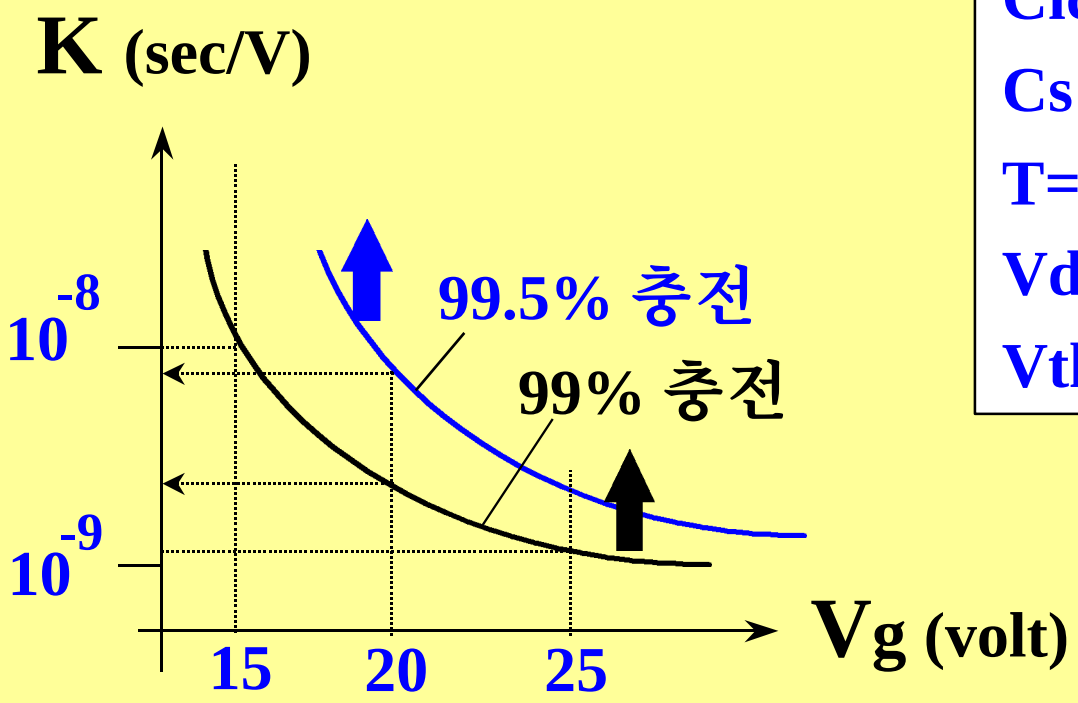
Vth = 3.5V

T=27 msec(SVGA)

충전률= 99%

전류 구동능력(K)의 충전률, Vg 의존성

(Design Simulation 예)



<Simulation 조건>

Clc = 0.2pF

Cs = 0.3pF

T=27 msec(SVGA)

Vd = 10V

Vth = 3.5V

7.4 TFT-LCD의 Design Simulation

7.4.1 단위 화소의 동작 특성

7.4.2 TFT의 I-V 특성

7.4.3 TFT의 최적 Design Simulation

7.4.4 누설전류와 축적용량 Design Simulation

7.4.5 신호지연과 신호배선 Design Simulation

Storage Capacitor (Cs) 의 역활

1.액정 Cell 전압 유지능력(VHR) 보조

2.Kickback 감소

3.Image Quality 향상

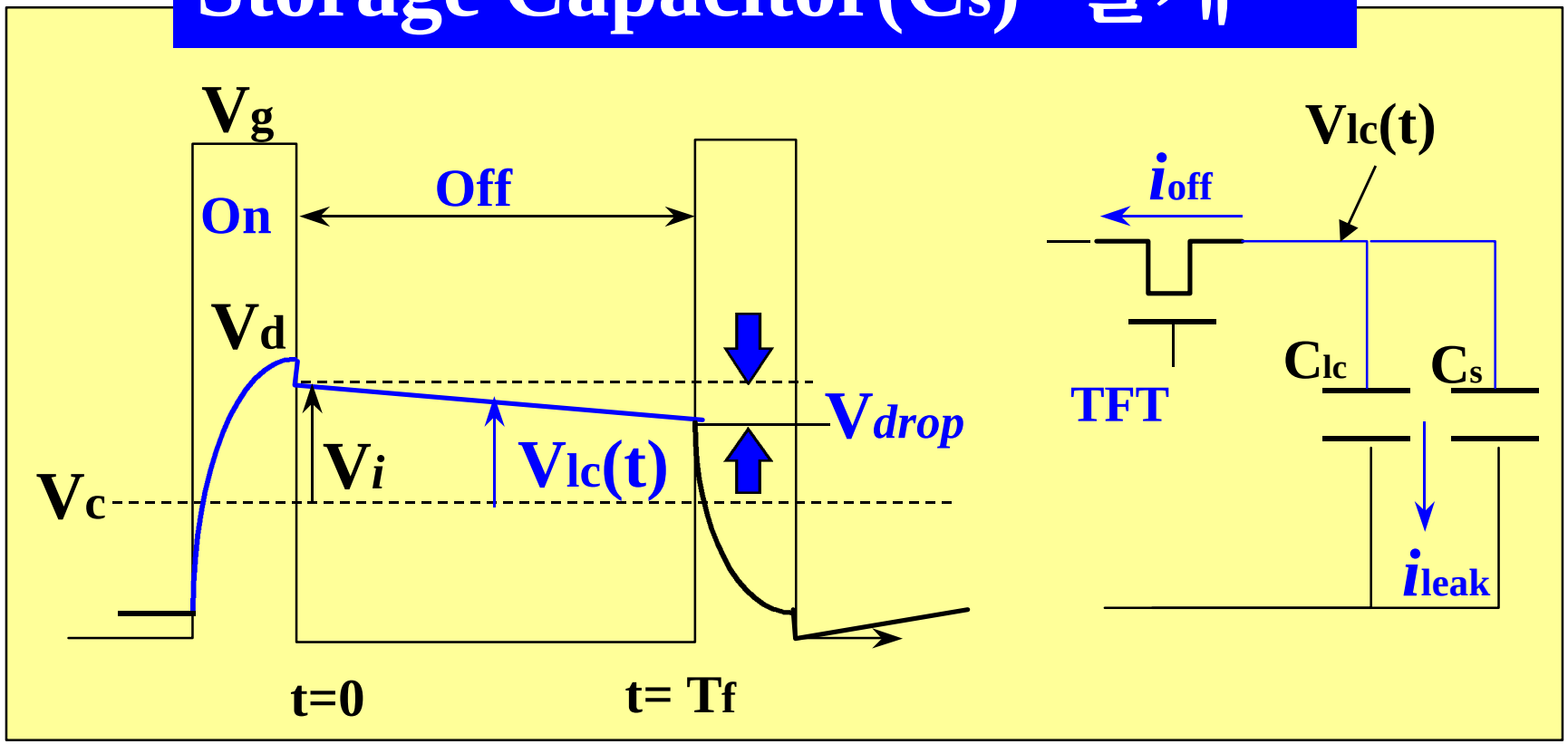
Contrast Ratio & Fllicker 특성

Cs 증가의 한계

TFT 부하 증가

개구율 감소

Storage Capacitor(C_s) 설계



V_i :충전 종료시 액정 전압 (Black 표시전압)

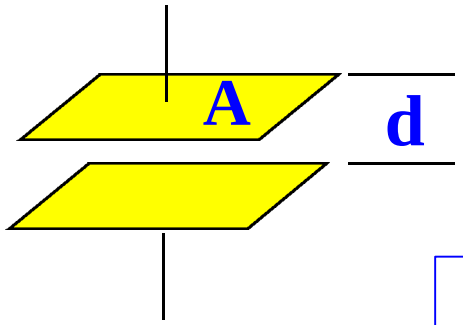
Tf: Frame 주기(TFT off 주기, 1/60sec)

V_{drop} :누설전류에 의한 전압 강하

액정의 비저항

$C_{LC} = \varepsilon_{LC} A_{ITO} / d_{LC}$

$R_{LC} = \rho_{LC} d_{LC} / A_{ITO}$



A_{ITO} = S/(m x n): 화소전극 크기

S: 표시면적(화면 크기)

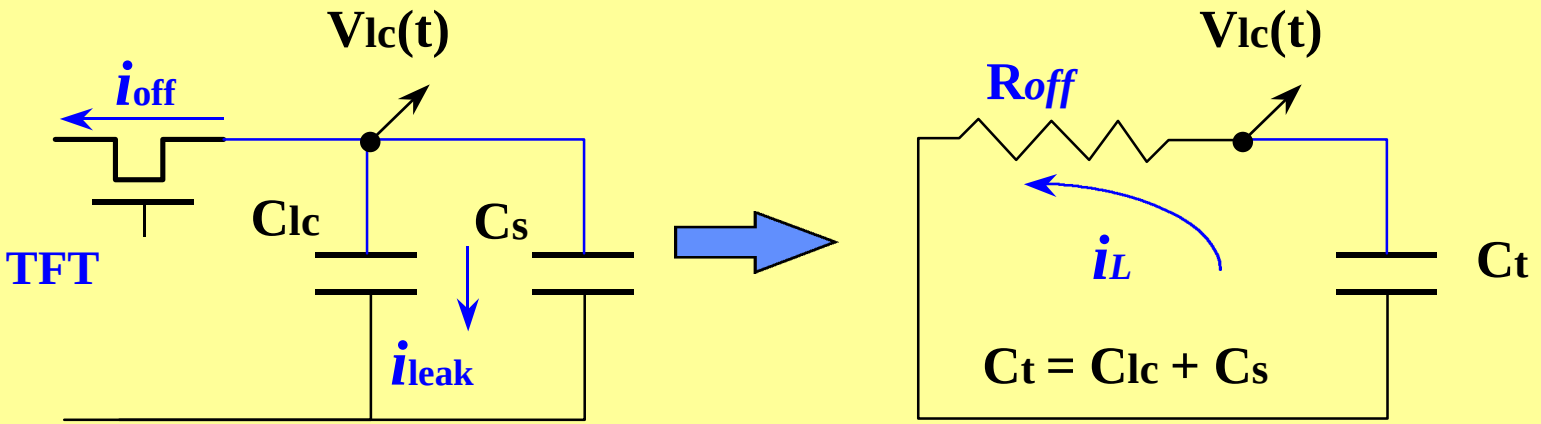
d_{LC} :Cell Gap

$R_{LC} C_{LC} = \rho_{LC} \varepsilon_{LC} << Tf$

ex) ε_{LC} = 5~10 ε_o, Tf = 1/60 sec

$\rho_{LC} >> 10^{10}$ W-cm

Ioff Margin & Cs 설계



$$V_{lc}(t) = V_{lc}(0)\,[\,\mathrm{Exp}(-t/R_{off}\,C_t)] \qquad (7.4.21)$$

$$V_{drop} = V_{lc}(0) - V_p(t)$$

$$V_{drop} = V_{lc}(0)\,[1 - \mathrm{Exp}(-T_f/R_{off}\,C_t)\,] \qquad (7.4.22)$$

$$R_{off} > (T_f / C_t) / \mathrm{Ln}\{V_{lc}(0) / (V_{lc}(0) - V_{drop})\} \qquad (7.4.23)$$

V_{drop} << 1 gray level (<20 mV for 64-gray scale)

Exemple (I_{off} Margin)

T_f = 16.7 msec (60 frame/sec)

$V_{lc(0)}$ = 5V (액정 전압, Black 표시)

C_{lc} = 0.2pF, C_s = 0.5pF 인 경우

V_{drop} < 20 mV 가 되는 허용 I_{off} 는 ?

From Eq.(7.4.23)

$$R_{off} > \frac{16.7 \times 10^{-3}\ \text{sec}}{(0.8 \times 10^{-12}\ \text{F}) \times \text{Ln}[5.0\text{V} / (5.0\text{V} - 0.02\text{V})]} = 5.21 \times 10^{12}\ \Omega$$

$$I_{off} < \frac{V_p(0)}{R_{off}} = \frac{5\ \text{V}}{5.21 \times 10^{12}\ \Omega} = 0.96 \times 10^{-12}\ \text{A}$$

7.4 TFT-LCD의 Design Simulation

7.4.1 단위 화소의 동작 특성

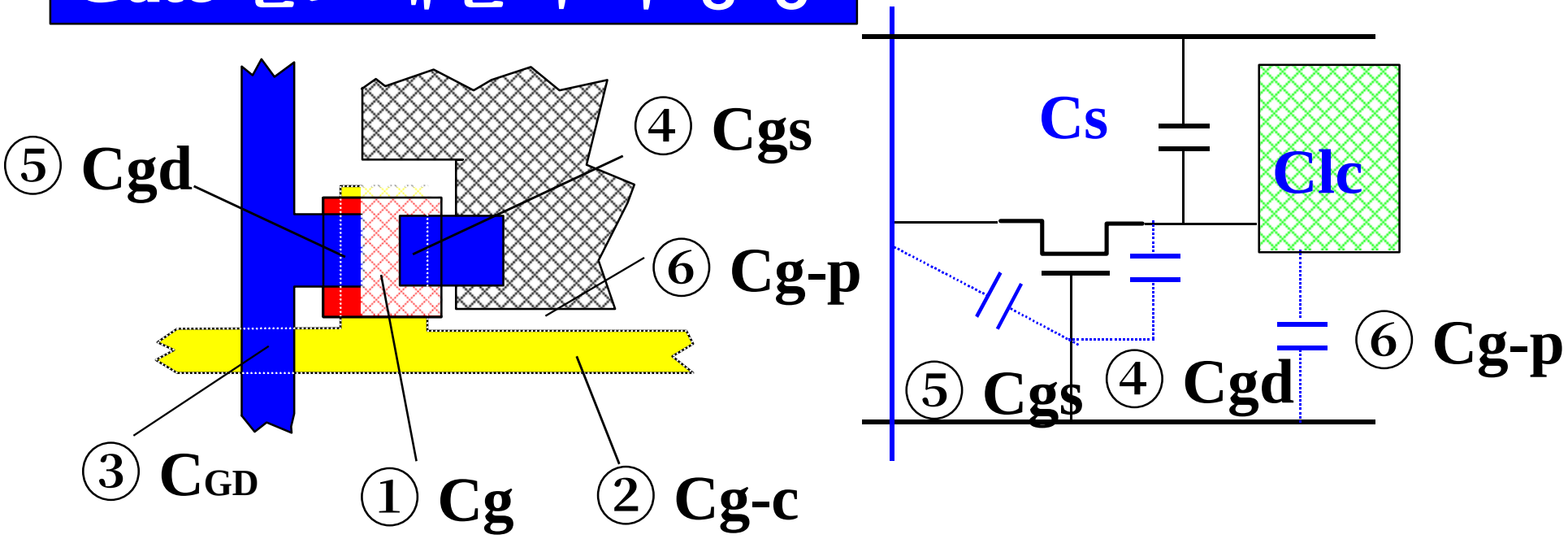
7.4.2 TFT의 I-V 특성

7.4.3 TFT의 최적 Design Simulation

7.4.4 누설전류와 축적용량 Design Simulation

7.4.5 신호지연과 신호배선 Design Simulation

Gate 신호배선 부하 용량



① Cg: TFT의 Gate 용량 (SiNx)

② Cg-c: Gate 신호배선- 대향전극간 용량(L/C)

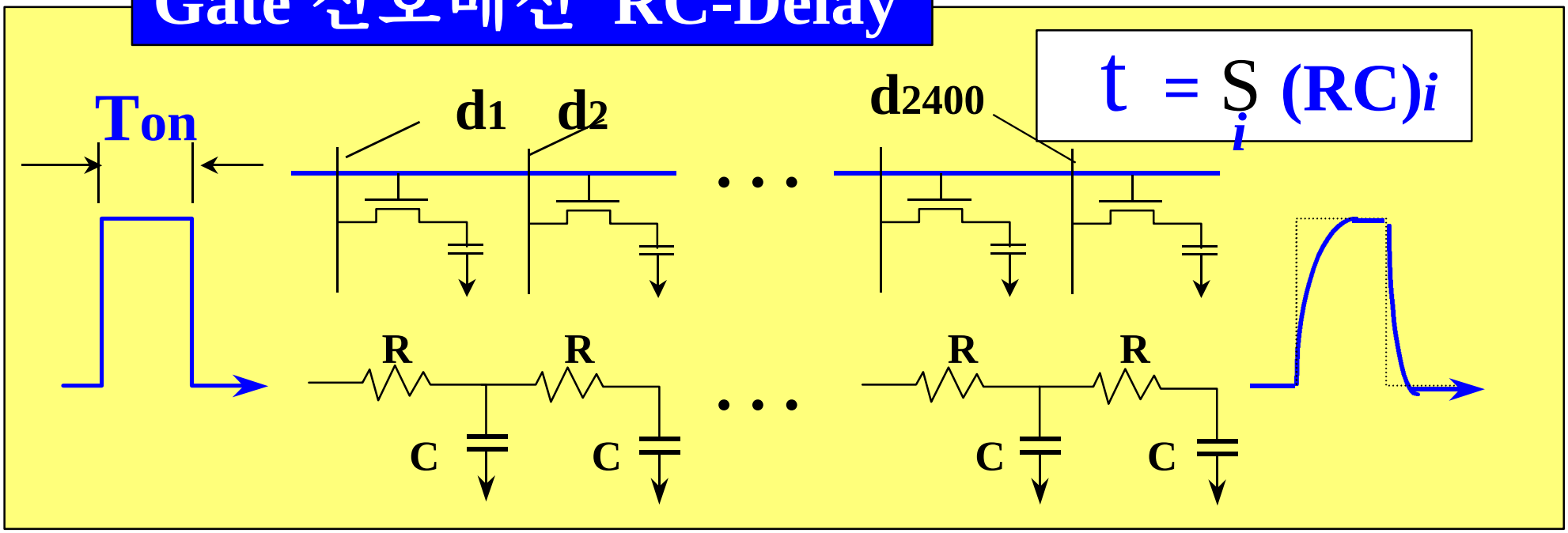
③ CGD: Gate 신호배선- Data 신호배선간 용량(SiNx)

④ Cgd: TFT의 Gate - Drain 간 용량(SiNx)

⑤ Cgs:TFT의 Gate - Source 간 용량(SiNx)

⑥ Cg-p: Gate 신호배선 - 화소전극간 용량 (L/C)

Gate 신호배선 RC-Delay



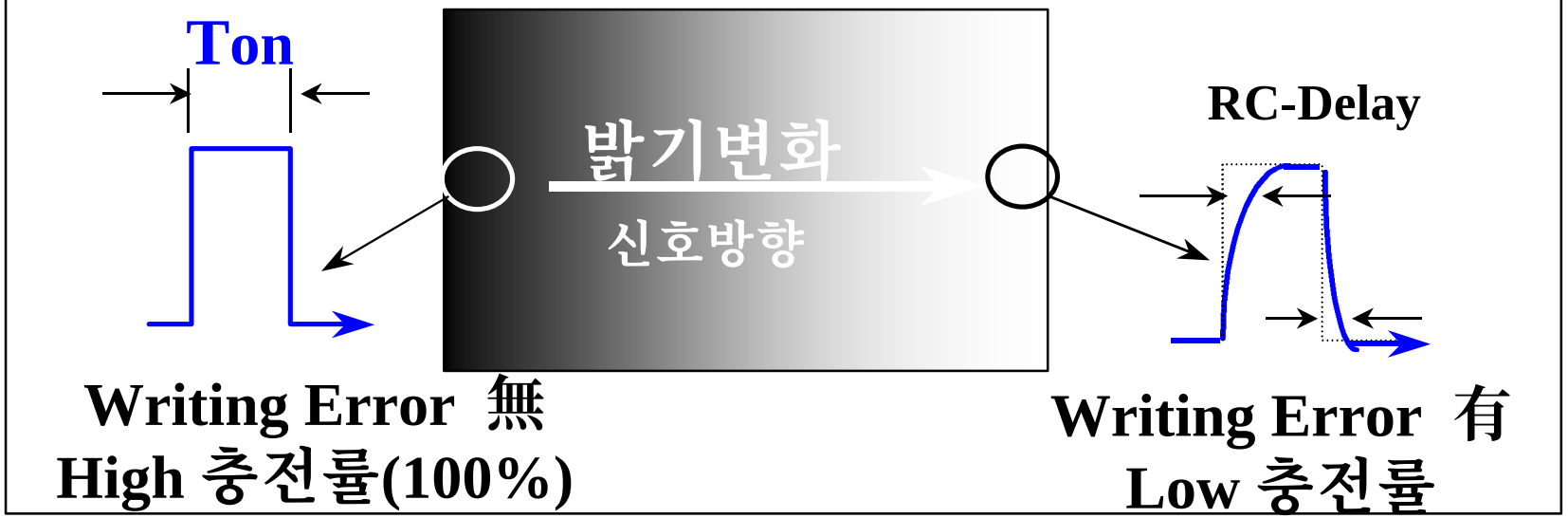
Effective TFT on time = Gate Pulse Width - RC Delay

Ex) SVGA (800 x 600)

Ton = 27 msec

Design Rule: RC< 20% of Ton ⟹ RC-Delay < 5 msec

Writing Error & Shading

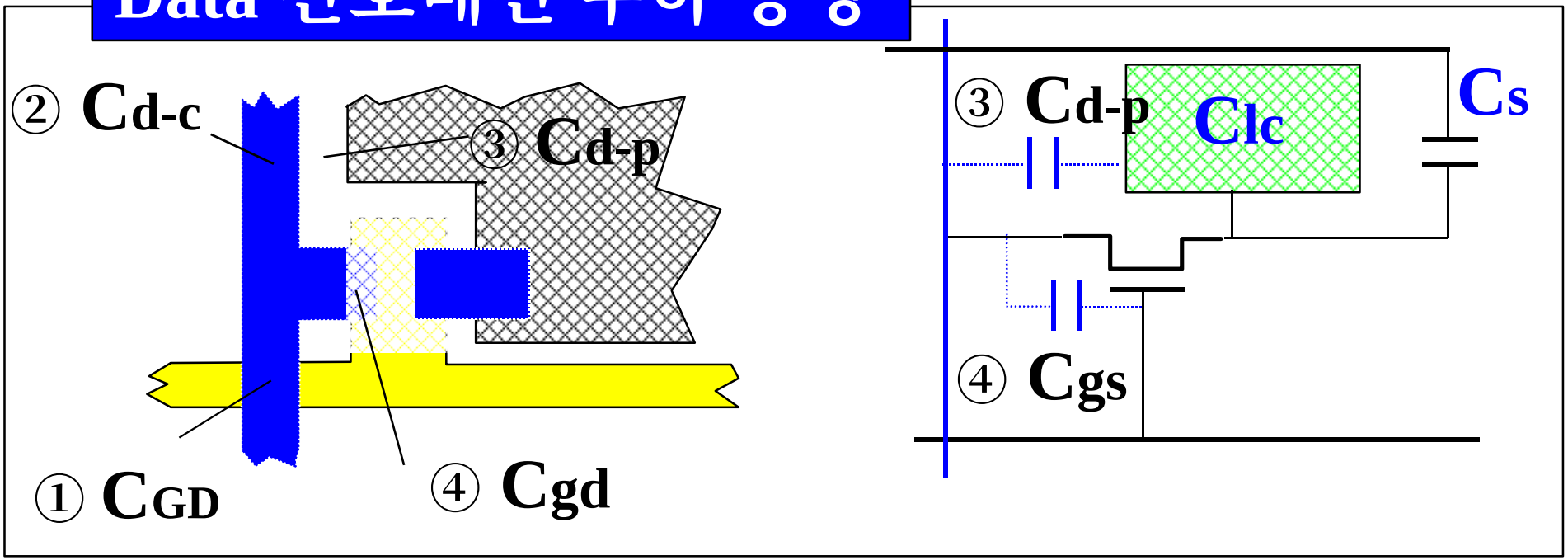


RC-delay Design Rule

* 허용 RC-Delay :
20% of Writing Time

AMLCD	Gate 배선	Matrix(Cell 수)	Writing Time	허용 RC
10.4” VGA	211.2 mm	480 x 640 x 3	32 msec	6.4 msec
12.1” SVGA	246.0 mm	480 x 640 x 3	27 msec	5.4 msec
13.3” XGA	270.3 mm	480 x 640 x 3	21 msec	4.2 msec
17.0” SXGA	337.9 mm	480 x 640 x 3	16 msec	3.2 msec
21.3” UXGA	432.0 mm	480 x 640 x 3	13 msec	2.6 msec

Data 신호배선 부하 용량



① CGD: Data 신호배선- Gate 신호배선간 용량(SiNx)

② Cd-c: Data 신호배선- 공통전극간 용량(L/C)

③ Cgs: TFT의 Gate - Source 간 용량(SiNx)

④ Cd-p: Data 신호배선 - 화소전극간 용량(L/C)

Home Work (II)

<연습문제, p338>

Due: 다음 강의시간 (4/21, 金)

5. 60 frame/sec 로 동작하는 12.1인치 SVGA급 TFT-LCD를 한 시간 동안 동작시는 경우 TFT-LCD에 내장된 한 개의 TFT의 총 누적 On 시간을 구하시오.
   또 같은 조건에서 XGA급의 TFT의 총 누적 On 시간을 구하시오.

10. 본문 식 7.4.15, 식 7.4.16의 결과는 같은 조건의 14.1인치 XGA급 LCD의 경우 어떻게 되겠는지 본문에 주어진 식을 이용하여 계산으로 구하시오.
    단, 허용되는 gate 신호배선의 RC-Delay는 4μsec 임