

5.0 V-Only Flash Memory Negative Gate Erase Technology



Advanced
Micro
Devices

Application Note

Advanced Micro Devices' Negative Gate Erase, 5.0 V-only technology is the most cost-effective and reliable approach to single-supply Flash memories. The innovative approach AMD has taken to 5.0 V-only technology provides designed-in reliability that is equal to that of its 12.0 V devices. In fact, transistor oxides are not subjected to any voltages higher than on AMD's 12.0 V devices. This approach minimizes internal power generating requirements which results in a negligible impact on die size because of the 5.0 V-only reprogramming capability.

The minimal power requirement of AMD's Negative Gate Erase, 5.0 V-only technology is made possible by design techniques which use the systems' V_{CC} power supply to provide the 10-20 mA (peak) current for Band-to-Band tunneling. Erase operations are performed when the system V_{CC} voltage is applied to the source terminal and the gate is pumped to a negative voltage. Less than 10 μA of current is required on the gate to enable Fowler-Nordheim tunneling.

Negative Gate Erase uses the same mechanism to erase a cell as the company's 12.0 V devices. Programming operations are performed with positive voltage pumped on the gate terminal at less than 10 μA of current. Hot channel electrons are injected into the floating gate in the same manner as 12.0 V devices.

The 5.0 V-only cell layout and geometry are comparable to the 12.0 V Flash memory cell. This ensures long term scalability equal to conventional 12.0 V flash designs without any penalty in die size. AMD added Dual Layer Metal (DLM) technology to implement its flexible sector erase architecture. AMD's unique sector isolation ensures reliable endurance cycling of at least 100K cycles for each sector whether erased individually or in combination.

AMD's innovative charge pump design techniques allow this device to consume less power than 12.0 V devices during write operations. Approximately 90% charge pump efficiency is achieved with AMD's unique diode V_t cancellation techniques. In addition, the charge pump design minimizes noise and ripple associated with voltage conversion circuits.

The culmination of these innovative design techniques makes this device ideal for power sensitive portable applications.

CHARGE PUMP CHARACTERISTICS— OVERVIEW

Before discussing the details of AMD's 5.0 V-only technology it is helpful to review the basic concepts of charge pump design. These concepts apply to stand alone DC/DC converters as well as charge pumps integrated into the device silicon. All charge pump designs share common characteristics. For instance the available current from a voltage pump is determined by the Z_{out} and V_{out} of the circuit.

- Z_{out} is proportional to $n/(C \cdot F)$
 - n = # of charge pump stages
 - C = capacitor size of each stage
 - F = clock rate
- V_{out} is proportional to $n \cdot (V_{CC} - V_{Diode})$
 - n = # of charge pump stages
 - V_{out} = Device V_{CC}
 - V_{Diode} = voltage drop of charge pump blocking diode
- Noise is proportional to $L \cdot (di/dt)$
 - L = bond wire inductance
 - di/dt = rate of current change

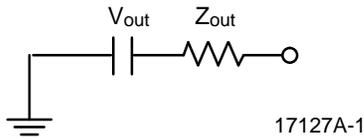
There are a number of issues to note about these relationships.

The silicon area of the charge pump is determined by the product of n and C (number of stages times the capacitor size). Efficient use of chip silicon requires this product to be as small as possible.

The efficiency of the voltage generated by the pump circuitry is increased as the effective voltage drop of the charge pump blocking diode is reduced ($V_{CC} - V_{Diode}$).

The voltage available at the output of the pump (when current is drawn) increases when Z_{out} decreases. Z_{out} decreases as either n is reduced or the product $C \cdot F$ increases. In addition, once a given Z_{out} is determined the values of C and F may vary in inverse proportion while maintaining the same product value.

Noise generated by the charge pump is minimized with a lower F (when $n \cdot C$ is large). But as F decreases C must increase in order to keep the product $C \cdot F$ constant.



Charge Pump Model

Negative Gate Erase Technology

Negative Gate Erase is used for erase operations in order to minimize the current drawn from the erase charge pump. In order to illustrate the importance of this, it is beneficial to first describe how today's 12.0 V V_{PP} Flash devices operate. Then conventional techniques of generating 12.0 V from a 5.0 V V_{CC} internally will be examined before discussing the benefits of Negative Gate Erase.

Today's 12.0 V Flash devices erase the memory cell at the Source terminal with 12.0 V applied. The gate is grounded and the drain is left floating. The external V_{pp} circuit supplies the V_{pp} current required for erase operations. This provides the 10-20 mA (peak) Band-to-Band tunneling current along with the Fowler-Nordheim tunneling current required to remove charge off the floating gate.

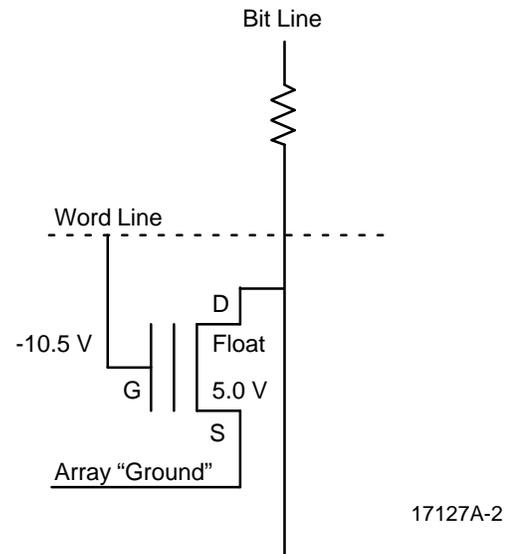
Conventional techniques in generating 12.0 V at the source terminal from a 5.0 V V_{CC} internal supply require huge charge pumps in order to supply the 10-20 mA (peak) of Band-to-Band tunneling current. This approach requires significant silicon real estate (charge pump area = n^2C) and consumes large amounts of power [$(12.0\text{ V} * 30\text{ mA}) \div \text{Efficiency} \geq 360\text{ mW}$].

Multiple transistor EEPROM 5.0 V-only technology uses charge pumps to internally raise the gate voltages to between 18 and 20 V at $< 10\ \mu\text{A}$. A multiple transistor approach requires one and a half to twice the silicon real estate as single-transistor approaches. Both conventional 12.0 V Flash and AMD's 5.0 V-only technology produce approximately half the electric field on the tunnel oxide as with EEPROM technology. The lower tunnel oxide fields extend the life of the oxide by orders of magnitude. In addition, EEPROM technology implements uniform channel tunneling instead of source-side tunneling as with conventional 12.0 V and AMD's 5.0 V-only technology. Uniform channel tunneling stresses

the entire oxide region while source-side tunneling only stresses a small region of the oxide.

AMD's Negative Gate Erase technique actually provides the same electric fields to the Flash memory cell and uses the same erase mechanisms as its 12.0 V Flash devices. Negative Gate Erase is used in order to reduce the current drawn from the erase charge pump. The Band-to-Band tunneling current (10-20 mA peak) comes directly from the system V_{CC} through the Array Ground terminal. This is the most efficient way to use an existing system V_{CC} supply. The current required from the Negative Gate Erase charge pump is less than $10\ \mu\text{A}$ at -10.5 V. This reduces the internal power consumption in relation to conventional 12.0 V approaches.

A circuit diagram of Negative Gate Erase is illustrated below.



Notes:

1. Gate terminal is pumped to -10.5 V @ $< 10\ \mu\text{A}$ current
2. 10-20 mA (peak) erase current is provided to the Source terminal by the system's V_{CC} supply

Key:

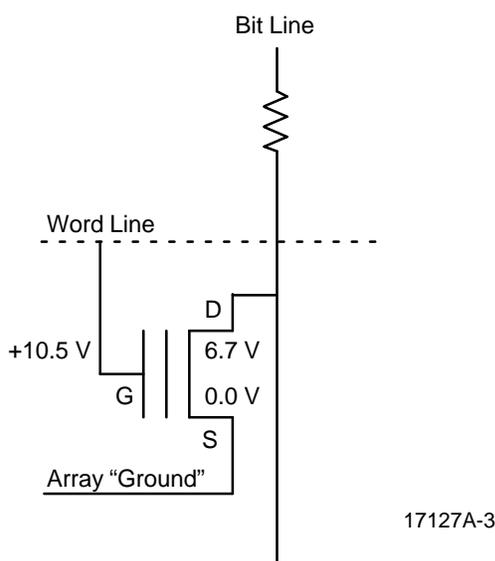
- D = Drain terminal
- G = Gate terminal
- S = Source terminal

5.0 V-Only Negative Gate Erase Circuitry

5.0 V-Only Programming

AMD's 5.0 V-only programming technique provides the same electric fields to the memory cell and uses the same programming mechanisms as its 12.0 V Flash devices. The drain is pumped to 6.7 V from 5.0 V and supplies approximately 0.5 mA of current per cell. The internal power generation required for the Channel Hot Electron injection mechanism is minimized because the charge pump only delivers a 34% voltage increase from the base V_{CC} supply. This also provides the benefit that the cell's programming characteristics remain constant even if the system V_{CC} supply varies. This current supplies the Channel Hot Electrons that are injected into the floating gate in order to program the memory cell. The current required by the gate voltage charge pump is less than $10\ \mu\text{A}$. This minimizes internal power consumption.

A circuit diagram of the programming circuitry is illustrated below.



Notes:

1. Gate terminal is pumped to +10.5 V @ $< 10\ \mu\text{A}$ current
2. Drain terminal is pumped to 6.7 V from 5.0 V V_{CC} supply @ 0.5 mA

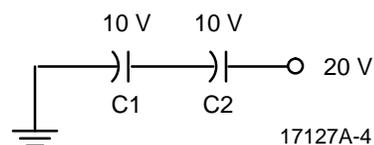
5.0 V-Only Drain Programming

AMD's 5.0 V-ONLY DEVICE EQUALS THE RELIABILITY OF 12.0 V DEVICES

Equivalent Electric Fields Charge Pump Circuitry

One component of device reliability is related to the electric fields applied across internal device transistors. Very high electric fields may cause oxide breakdown and hence reliability problems. One of the main design and reliability requirements in AMD's 5.0 V-only circuit implementation was the maintenance of electric fields across the charge pump oxides equivalent to those of the oxides subject to high voltage in the 12.0 V device. AMD's techniques minimize the electric fields across the oxides to be equivalent to those across the device transistor oxides during standard Read operations of the 12.0 V device. This ensures that the 5.0 V-only design will not be more susceptible to oxide failures than 12.0 V devices. There has never been any physical damage to an oxide from the high voltages internal to AMD's 12.0 V Flash device.

One way to maintain low electric fields across transistor oxides is to stack multiple capacitors together. This circuit technique delivers a large output voltage while maintaining low electric fields across each oxide. As an example, with an oxide that is able to reliably withstand voltages of 10 V, a circuit can be constructed to provide 20 V by stacking (in series) two capacitors with 10 V across each oxide. This circuit ensures that the electric fields remain within the specified limits.



Capacitors Charge Pump Model

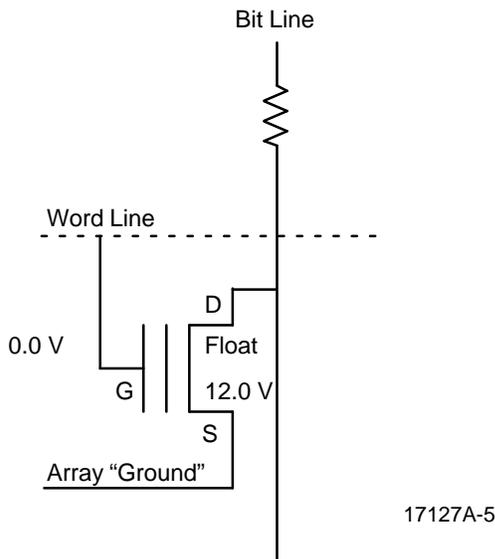
Memory Cell Circuitry

It is important to note that the electric fields applied to the data storage memory cells of the 5.0 V-only device are the same as that of the 12.0 V device. This ensures that the 5.0 V-only design will not be more susceptible to oxide failures than 12.0 V devices. An observable measure that the electric fields are indeed the same is found in the erase time parameter. Erase time depends upon the electric field across the floating gate and the thickness of the tunnel oxide (T_{OX}). T_{OX} and the erase time of the 5.0 V-only device are the same as in the 12.0 V device. Therefore the electric field is the same in both devices.

The electric fields of the 5.0 V circuit are also demonstrated by analyzing the coupling ratios in the memory cell transistor. However, it is first beneficial to discuss the coupling ratios of standard 12.0 V Flash circuitry. We will use the erase circuit as an example. The same concepts apply to the programming circuitry.

Electric Fields in Standard 12.0 V V_{PP} Erase Circuits

The standard Flash memory cell applies 12.0 V to the Source terminal. The Gate terminal is grounded and the drain is left floating. The actual electric field seen by the tunnel oxide is a superposition of three components. One is because the field generated by the trapped electrons on the floating gate. This is the state of a programmed memory cell prior to erase. The other two result from coupling of the voltage between the word line (Gate terminal)/floating gate and between the source terminal/ floating gate. In the case of standard 12.0 V V_{pp} programming, the only component from the voltage coupling is between the source terminal and the floating gate. There is no coupling from the word line because it is at a zero voltage potential. The resulting electric field never exceeds a peak value of 10 mV/cm.



Notes:

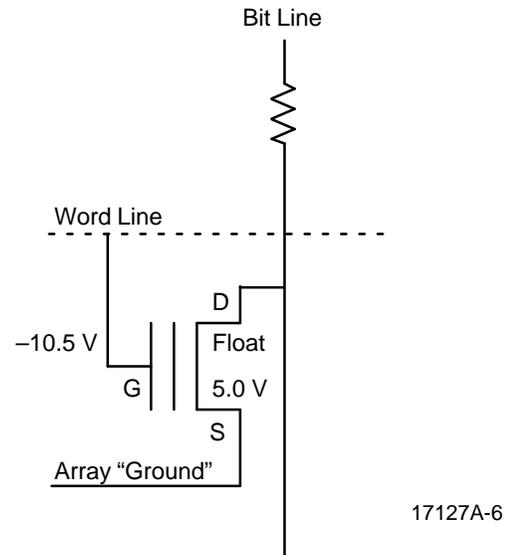
1. Tunnel oxide (T_{ox}) electric field is determined by superposition.
 - Floating Gate Voltage from stored electrons reduces voltage across T_{ox}
 - Source Coupling Voltage on the floating gate reduces the voltage across the T_{ox}
2. Total electric field across T_{ox} due to superposition is <10 mV/cm.

Standard 12.0 V V_{PP} Erase

Equivalent Electric Fields in AMD's 5.0 V-Only Negative Gate Erase Circuitry

AMD's Negative Gate Erase circuitry applies the same electric fields to the memory cell as the 12.0 V device. The Gate terminal is negatively pumped to -10.5 V and the source terminal is at 5.0 V supplied by the system V_{CC} supply. The drain terminal is left floating. The actual electric field seen by the tunnel oxide is a superposition of three components. One is due to the field generated by the trapped electrons on the floating gate. This is the state of a programmed memory cell prior to erase. The other two result from coupling of the voltage between the word line (Gate terminal)/ floating gate and between the source terminal/ floating gate. This time there is voltage coupling from both the Source terminal and word line. The resulting electric field is the same as in the 12.0 V device. The electric field is always ≤ 10 mV/cm.

In addition, the Negative Gate Erase approach actually produces a lower electric field across the cell junctions. This is because the source terminal is subjected to 5.0 V levels instead of 12.0 V.



Notes:

1. Tunnel oxide T_{ox} electric fields determined by superposition.
 - Floating Gate Voltage from stored electrons reduces the voltage across the T_{ox}
 - Gate Coupling Voltage on the floating gate reduces the voltage across the T_{ox}
 - Source Coupling Voltage on the floating gate reduces the voltage across the T_{ox}
2. Total electric field across the T_{ox} due to superposition is < 10 mV/cm.

5.0 V-Only Negative Gate Erase

DATA INTEGRITY

Ruggedized Programmability

AMD's 5.0 V-only approach is designed not to be sensitive to variations in the system V_{CC} supply during programming operations.

This is achieved by pumping the drain terminal to 6.7 V. The device actually compensates for any system level variations in the V_{CC} supply. During programming the word line is pumped to +10.5 V and the source terminal is grounded. These voltage conditions and resulting electric field are the same as in 12.0 V devices.

Sector Write Protection

AMD implements a Dual Layer Metal (DLM) bussing technique in order to provide the most cost-effective and reliable method to individually isolate sectors during sector erase operations. This technique inhibits the presence of high voltage in non-addressed sectors from disturbing fixed data. Data in non-addressed sectors is isolated from all other sector program and erase operations.

Minimizing Charge Pump Noise and Voltage Ripple

Minimizing Noise

AMD's charge pump circuitry minimizes noise with a multi-stage pump design. Each stage has the same clock rate but is out of phase with all other stages. The phase shifting minimizes potential noise from any of the individual pumps. This technique delivers a very smooth and constant source of power. A V-8 automobile engine serves as an excellent analogy. Each of the eight stages of the charge pump is 45° out of phase. Each packet of charge is delivered in a way to provide a smooth flow of current.