ADVANCE INFORMATION

Am29F080B

8 Megabit (1 M x 8-Bit)
CMOS 5.0 Volt-only, Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10%, single power supply operation**
  - — Minimizes system level power requirements
- **Manufactured on 0.35µm process technology**
  - — Compatible with 0.5 µm Am29F080 device
- **High performance**
  - — Access times as fast as 70 ns
- **Low power consumption**
  - — 25 mA typical active read current
  - — 30 mA typical program/erase current
  - — 1 µA typical standby current (standard access time to active mode)
- **Flexible sector architecture**
  - — 16 uniform sectors of 64 Kbytes each
  - — Any combination of sectors can be erased.
  - — Supports full chip erase
  - — Group sector protection:

    A hardware method of locking sector groups to prevent any program or erase operations within that sector group

    Temporary Sector Group Unprotect allows code changes in previously locked sectors
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies bytes at specified addresses
- **Minimum 100,000 write/erase cycles guaranteed**
- **Package options**
  - — 40-pin TSOP
  - — 44-pin SO
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply Flash standard
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase cycle completion
- **Ready/Busy output (RY/BY#)**
  - — Provides a hardware method for detecting program or erase cycle completion
- **Erase Suspend/Resume**
  - — Suspends a sector erase operation to read data from, or program data to, a non-erasing sector, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Resets internal state machine to the read mode

GENERAL DESCRIPTION

The Am29F080B is an 8 Mbit, 5.0 volt-only Flash memory organized as 1,048,576 bytes of 8 bits each. The 1 Mbyte of data is divided into 16 sectors of 64 Kbytes each for flexible erase capability. The 8 bits of data appear on DQ0–DQ7. The Am29F080B is offered in 40-pin TSOP and 44-pin SO packages. The Am29F080B is manufactured using AMD's 0.35 µm process technology. This device is designed to be programmed in-system with the standard system 5.0 volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

This device is functionally equivalent to the Am29F080 device, and is intended to be fully interchangeable with it. All specifications remain the same as for the Am29F080.

The standard device offers access times of 70, 90, 120, and 150 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus conten-

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tion, the device has separate chip enable (CE#), write enable (WE#), and output enable (OE#) controls.

The device is entirely command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 volt Flash or EPROM devices.

The device is programmed by executing the program command sequence. This invokes the Embedded Program algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The device is erased by executing the erase command sequence. This invokes the Embedded Erase algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. A sector is typically erased and verified within one second. The device is erased when shipped from the factory.

The hardware sector group protection feature disables both program and erase operations in any combination of the eight sector groups of memory. A sector group consists of four adjacent sectors.

The Erase Suspend feature enables the system to put erase on hold for any period of time to read data from, or program data to, a sector that is not being erased. True background erase can thus be achieved.

The device requires only a single 5.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The host system can detect whether a program or erase cycle is complete by using the RY/BY# pin, the DQ7 (Data# Polling) or DQ6 (toggle) status bits. After a program or erase cycle has been completed, the device automatically returns to the read mode.

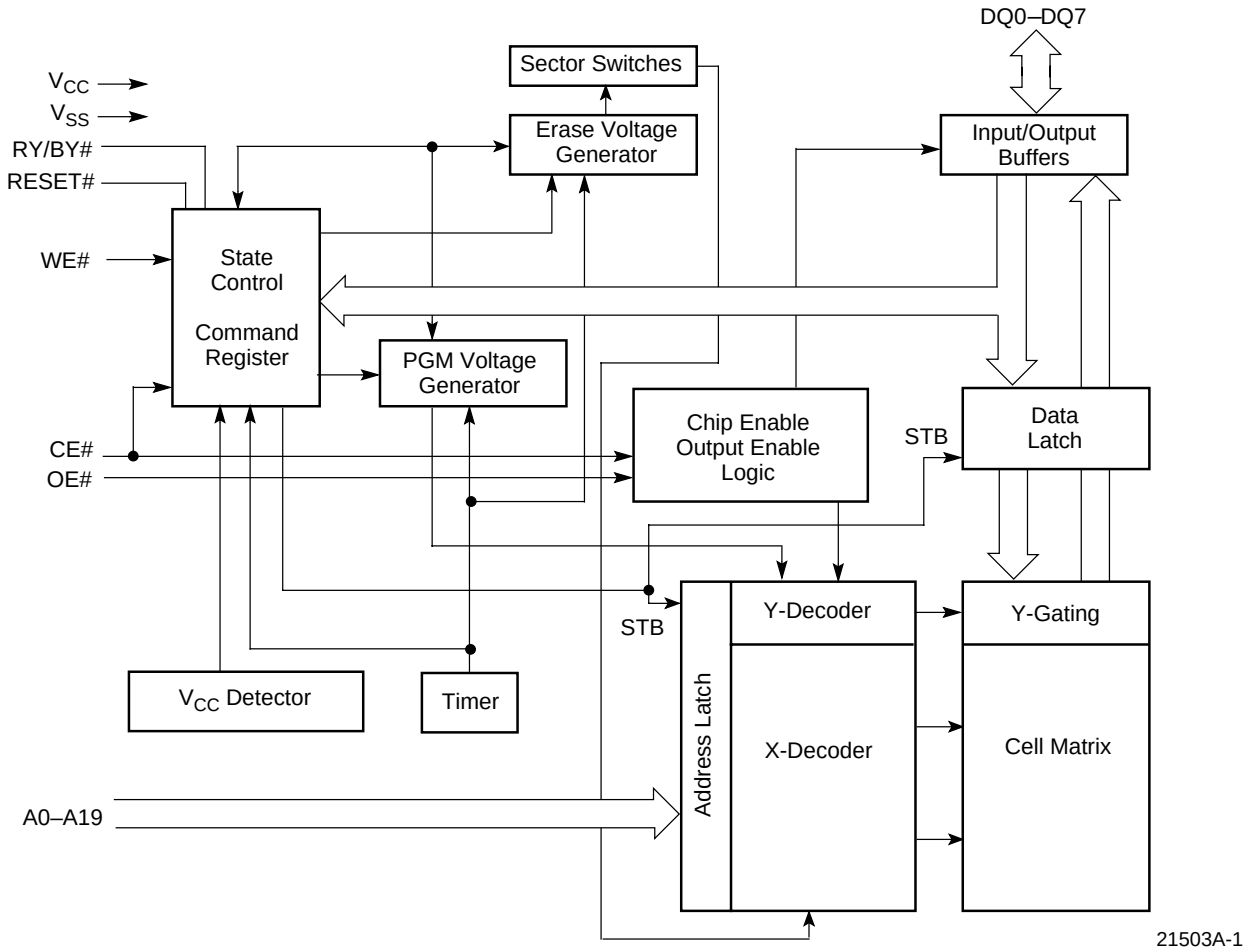
A hardware RESET# pin terminates any operation in progress. The internal state machine is reset to the read mode. The RESET# pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during either an Embedded Program or Embedded Erase algorithm, the device is automatically reset to the read mode. This enables the system's microprocessor to read the boot-up firmware from the Flash memory.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

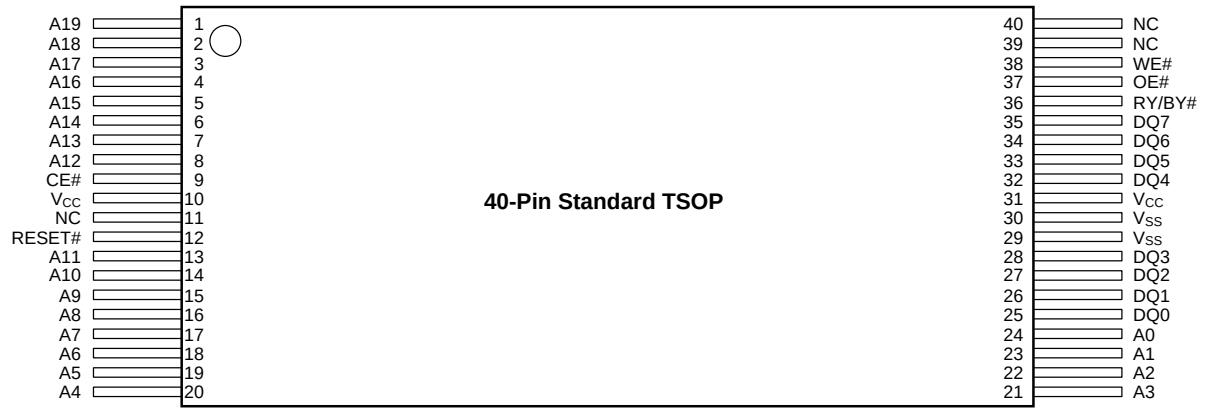
PRODUCT SELECTOR GUIDE

Family Part No.		Am29F080B			
Ordering Part No:	V_{CC} = 5.0 V ± 5%	**-75**			
	V_{CC} = 5.0 V ± 10%		**-90**	**-120**	**-150**
Max Access Time, ns (t_{ACC})		70	90	120	150
CE# Access, ns (t_{CE})		70	90	120	150
OE# Access, ns (t_{OE})		40	40	50	75

BLOCK DIAGRAM



CONNECTION DIAGRAMS



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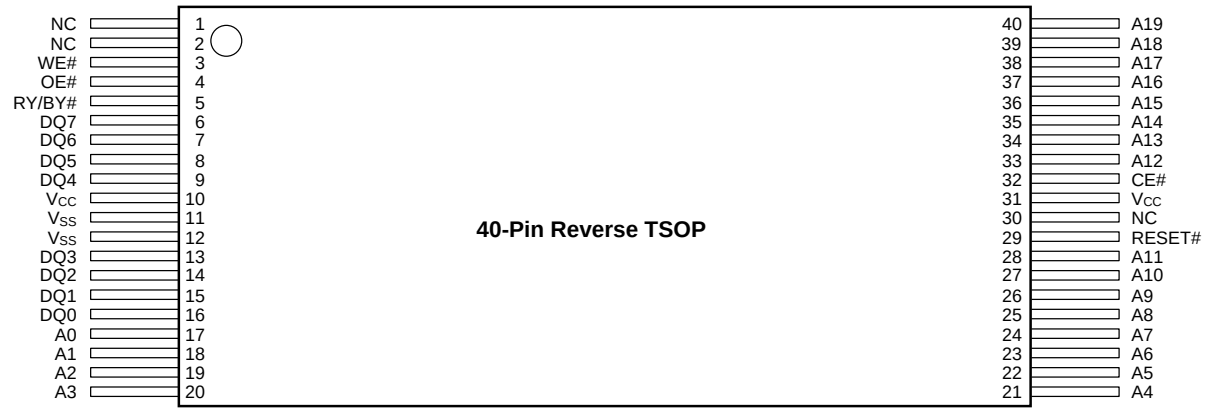

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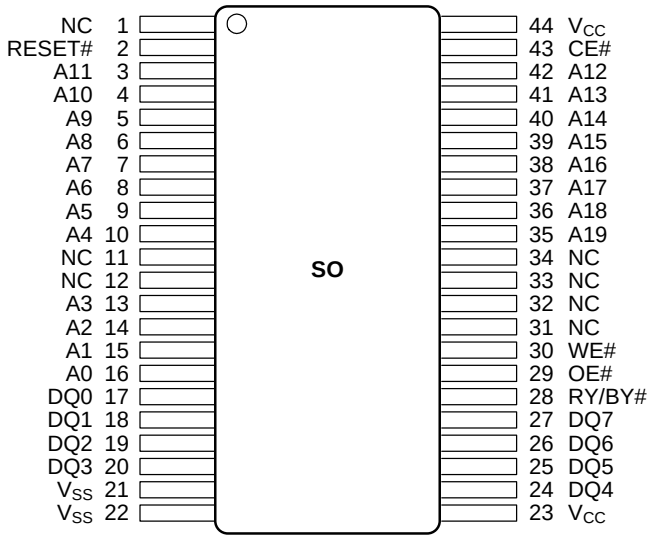

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PIN CONFIGURATION

A0–A19 = 20 Addresses

DQ0–DQ7 = 8 Data Inputs/Outputs

CE# = Chip Enable

WE# = Write Enable

OE# = Output Enable

RESET# = Hardware Reset Pin, Active Low

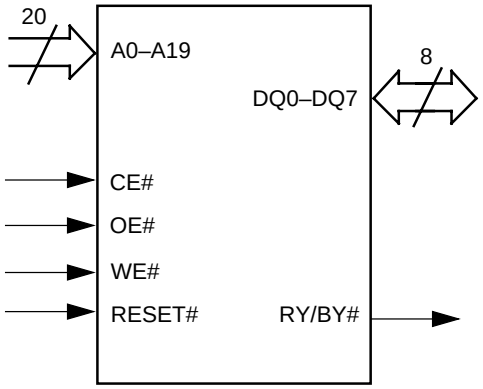
RY/BY# = Ready/Busy Output

V_{CC} = +5.0 V single power supply
(±10% for -90, -120, -150) or
(±5% for -75)

V_{SS} = Device Ground

NC = Pin Not Connected Internally

LOGIC SYMBOL



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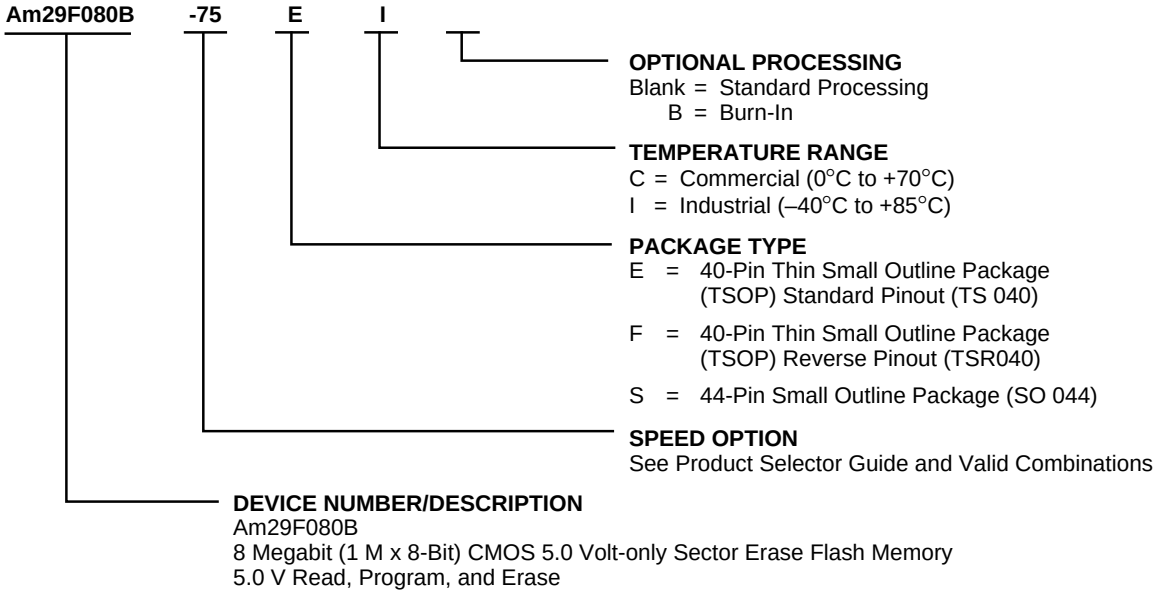
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
Am29F080B-75	EC, EI, FC, FI, SC, SI
Am29F080B-90	EC, ECB, EI, EIB, FC, FCB, FI, FIB SC, SCB, SI, SIB
Am29F080B-120	
Am29F080B-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 2 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Read Mode

To read data from the DQ0–DQ7 outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates data to the output pins. WE# should remain at V_{IH}.

The device automatically enters the read mode after device power-up, ensuring that no spurious alteration of device data occurs during the power transition. In the read mode, no command is necessary to obtain data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See “Reading Data” for more information. Refer to the AC Read-only Operations table for timing specifications and to Figure 9 for the timing diagram. I_{CC1} in the DC Characteristics tables represents the CMOS- or TTL/NMOS-compatible active current specification for the read mode.

Write Mode

To erase or program the device, the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}. While programming occurs one byte at a time, data is erased one sector at a time. Table 1 indicates the address space that each sector contains.

The Command Definitions section provides the requirements for initiating program and erase operations. Refer to AC Characteristics, Write (Erase/Program) Operations table for timing specifications. Figure 11 shows the timing diagram for erase operations, and Figure 12 shows the timing diagram for program operations. I_{CC2} in the DC Characteristics tables represents the CMOS- or TTL/NMOS-compatible active current specification for the write mode.

Table 1. Sector Address Table

	A19	A18	A17	A16	Address Range
SA0	0	0	0	0	000000h–00FFFFh
SA1	0	0	0	1	010000h–01FFFFh
SA2	0	0	1	0	020000h–02FFFFh
SA3	0	0	1	1	030000h–03FFFFh
SA4	0	1	0	0	040000h–04FFFFh
SA5	0	1	0	1	050000h–05FFFFh
SA6	0	1	1	0	060000h–06FFFFh
SA7	0	1	1	1	070000h–07FFFFh
SA8	1	0	0	0	080000h–08FFFFh
SA9	1	0	0	1	090000h–09FFFFh
SA10	1	0	1	0	0A0000h–0AFFFFh
SA11	1	0	1	1	0B0000h–0BFFFFh
SA12	1	1	0	0	0C0000h–0CFFFFh
SA13	1	1	0	1	0D0000h–0DFFFFh
SA14	1	1	1	0	0E0000h–0EFFFFh
SA15	1	1	1	1	0F0000h–0FFFFFh

Note: *All sectors are 64 Kbytes in size.*

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, power consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input. There are two methods of placing the device in the standby mode: one using both the CE# and RESET# pins; the other via the RESET# pin only.

The device enters the CMOS standby mode when CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when CE# and RESET# pins are both held at V_{IH}. The device tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. This mode is “CE# controlled,” since CE# determines whether the device is active or in the standby mode, while RESET# is held at $V_{CC} \pm 0.3$ V. (That is, during normal read and write operations the system would not need to use the hardware reset function.) The device requires standard access time (t_{CE}) for read access when the device is in either of these standby mode.

The device also enters the CMOS standby mode when the RESET# pin is held at $V_{SS} \pm 0.3$ V, or the TTL standby mode when the RESET# pin is held at V_{IL}. This mode is “RESET# controlled,” since CE# is don’t care under this condition. Once the RESET# pin is set high, the device requires 50 ns of wake up time in addition to the standard access time (t_{CE}) for reading

data. This method also halts any operation in progress and resets the device.

In the CMOS and TTL/NMOS-compatible DC Characteristics tables, I_{CC3} represents the CE#-Controlled standby current specification; I_{CC4} represents the RESET#-controlled standby current specification.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

RESET#: Hardware Reset

The RESET# pin provides a hardware method of resetting the device to the read mode. The RESET# pin must be driven to V_{IL} for at least a period of t_{RP}. **The device immediately terminates any operation in progress and resets the internal state machine to the read mode.** Any operation that was interrupted should be reinitiated once the device has returned to the read mode, to ensure data integrity.

The reset operation is complete t_{READY} after the RESET# pin is asserted low. The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

The RESET# pin may be tied to the system reset input. A system reset would thus also reset the Flash memory to the read mode, enabling the system to read the boot-up firmware from the Flash memory.

The system may use the RESET# pin to force the device into the standby mode. Refer to the Standby Mode section for more information.

Refer to the AC Characteristics tables for RESET# parameters, and to Figure 10 for the timing diagram.

Table 2. Am29F080B Device Bus Operations

Operation		CE#	OE#	WE#	RESET#	A0–A19	DQ0–DQ7
Read		L	L	X	H	A_{IN}	D_{OUT}
Write		L	H	L	H	A_{IN}	D_{IN}
TTL Standby	CE# Controlled	H	X	X	H	X	HIGH Z
	RESET# Controlled	X			L		
CMOS Standby	CE# Controlled	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	X	HIGH Z
	RESET# Controlled	X			$V_{SS} \pm 0.3$ V		
Output Disable		L	H	H	H	X	HIGH Z
Hardware Reset		X	X	X	V_{IL}	X	HIGH Z
Temporary Sector Group Unprotect (See Note)		X	X	X	V_{ID}	A_{IN}	X

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, D_{OUT} = Data Out, D_{IN} = Data In, A_{IN} = Address In, X = Don't Care. See DC Characteristics for voltage levels.

Note: *See the sections on Sector Group Protection and Temporary Sector Unprotect for more information.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector group protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 3. In addition, when verifying sector group protection, the sector group address must appear on the appropriate highest order address bits (see Table 4). Table 3 also shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 5. This method does not require V_{ID} on an address line. Refer to the Autoselect Command Sequence section for more information.

Table 3. Am29F080B Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A19 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29F080B	L	L	H	X	X	V_{ID}	X	L	X	L	H	D5h
Sector Group Protection Verification	L	L	H	SGA	X	V_{ID}	X	L	X	H	L	01h (protected)
												00h (unprotected)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SGA = Sector Group Address, X = Don't care.*

Note: *The system may also autoselect information in-system via the command register. See Table 5.*

Sector Group Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in a sector group. Each sector group consists of four adjacent sectors grouped as shown in Table 4. Any combination of one to all sector groups may be protected. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection are both accomplished using programming equipment. Details on implementing sector protection/unprotection are provided in a supplement, publication number 19945. Contact an AMD representative to obtain a copy of this document.

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the appropriate highest order address bits (see Table 4) indicate the desired sector group address, produces a logical "1" at DQ0 for a protected sector group, and a logical "0" for an unprotected sector group.

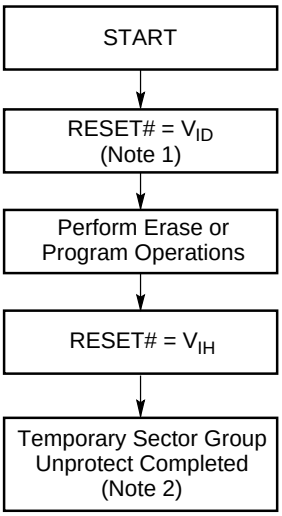
Table 4. Sector Group Addresses

Sector Group	A19	A18	A17	Sectors
SGA0	0	0	0	SA0–SA1
SGA1	0	0	1	SA2–SA3
SGA2	0	1	0	SA4–SA5
SGA3	0	1	1	SA6–SA7
SGA4	1	0	0	SA8–SA9
SGA5	1	0	1	SA10–SA11
SGA6	1	1	0	SA12–SA13
SGA7	1	1	1	SA14–SA15

Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID} (11.5 V – 12.5 V). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are

protected again. Figure 1 shows the algorithm, and Figure 16 shows the timing diagrams, for this feature.



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Notes:

1. *All protected sector groups unprotected.*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

HARDWARE DATA PROTECTION

The command sequence requirement of unlock cycles for programming or erasing provides data protection. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO} (see DC Characteristics for voltage levels), the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled. Under this condition the device resets to the read mode. Subsequent writes are ignored until the V_{CC} level is greater than V_{LKO}. The system must ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be at V_{IL} while OE# is at V_{IH}.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 5 defines the valid register command sequences. **Writing incorrect address and data values or writing them in the improper sequence resets the device to the read mode**.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the AC Characteristics section for timing diagrams.

Reading Data

The device automatically enters the read mode after device power up. No commands are required to retrieve data in this mode.

The device automatically returns to the read mode after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data. The device returns to the erase-suspend-read mode after completing an erase-suspend-program operation. See the Erase Suspend/Erase Resume Commands for more information.

The system must issue the reset command to return the device to the read mode if DQ5 goes high, or while in the autoselect mode.

See also the Read Mode section for more information. The Read-only Operations table provides the read parameters, and Figure 9 shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to the read mode. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read

mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written when the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Refer to the AC Characteristics section for parameters, and to Figure 9 section for the timing diagram.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector group is protected. Table 5 shows the address and data requirements. This method is an alternative to that shown in Table 2, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector group address (SGA) and the address 02h returns 01h if that sector group is protected, or 00h if it is unprotected. Refer to Table 4 for valid sector group addresses.

The system must write the reset command to return to the read mode.

Byte Program Command Sequence

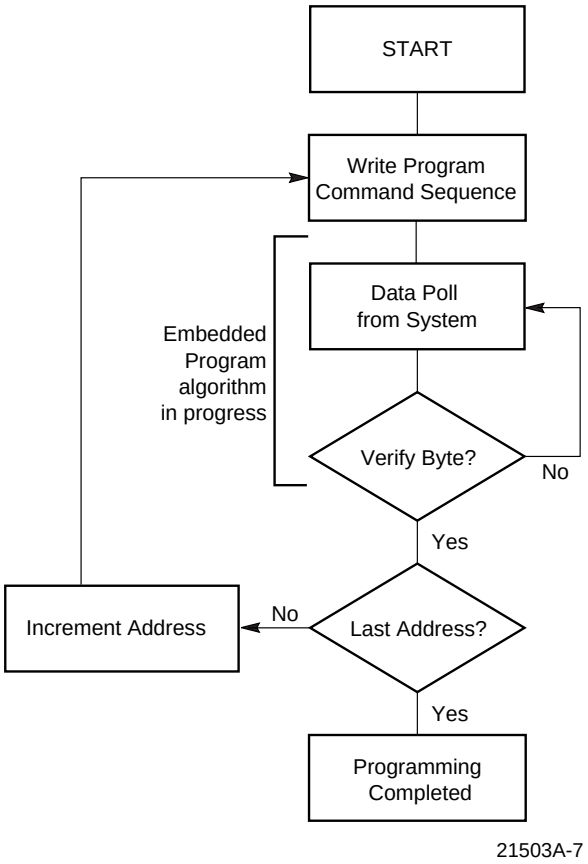
The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. The byte program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. Table 5 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a “0” back to a “1”.** Attempting to do so may halt the operation and set DQ5 to “1,” or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.

Figure 2 illustrates the algorithm for the program operation. Refer to the Write (Erase/Program) Operations table in the AC Characteristics section for parameters, and to Figure 12 for the timing diagram.



Note: *See Table 5 for program command sequence.*

Figure 2. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 5 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched.

Figure 3 illustrates the algorithm for the erase operation. Refer to the Write (Erase/Program) Operations tables in the AC Characteristics section for parameters, and to Figure 11 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 5 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** The system must rewrite the command sequence and any additional sector addresses and commands.

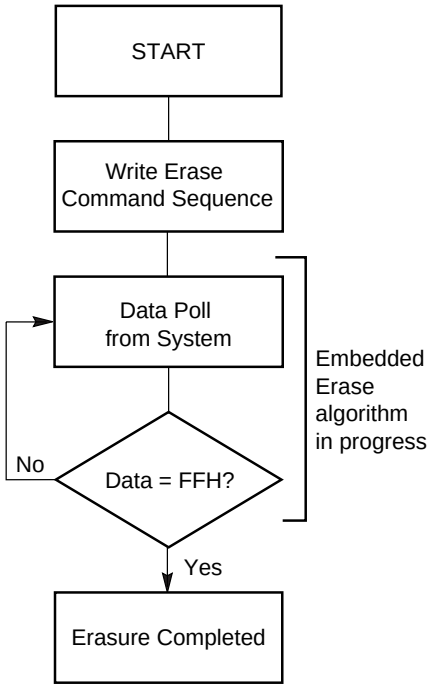
The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should

be reinitiated once the device has returned to the read mode, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to the Write Operation Status section for information on these status bits.)

Figure 3 illustrates the algorithm for the erase operation. Refer to the Write (Erase/Program) Operations tables in the AC Characteristics section for parameters, and to Figure 11 for timing diagrams.



Notes:

1. *See Table 5 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 3. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Byte Program operation. Refer to the Write Operation Status section for more information.

The system may also write the autoselect command sequence when the device is in the erase-suspend read mode. See the Autoselect Command Sequence section for more information.

The system must write the Erase Resume command (address bits are “don’t care”) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Table 5. Am29F080B Command Definitions

Command Sequence Read/Reset	Bus Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 3)	1	RA	RD										
Reset (Note 4)	1	XXX	F0										
Autoselect Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
Autoselect Device ID	4	555	AA	2AA	55	555	90	X01	D5				
Autoselect Sector Group Protect Verify (Note 5)	4	555	AA	2AA	55	555	90	SGA X02	00				
									01				
Byte Program	4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 6)	1	XXX	B0										
Erase Resume (Note 7)	1	XXX	30										

Legend:

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE# or CE# pulse.

PD = Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse.

SA = Address of the sector to be erased. Address bits A19–A16 uniquely select any sector.

SGA = Address of the sector group to be verified.

Notes:

1. *All values are in hexadecimal.*
2. *See Table 2 for descriptions of bus operations.*
3. *No unlock or command cycles required when device is in read mode.*
4. *The Reset command is required to return to the read mode when the device is in the autoselect mode or if DQ5 goes high.*
5. *The data is 00h for an unprotected sector group and 01h for a protected sector group. The complete bus address in the fourth cycle is composed of the sector group address (A19–A17), A1 = 1, and A0 = 0.*
6. *Read and program functions in non-erasing sectors are allowed in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
7. *The Erase Resume command is valid only during the Erase Suspend mode.*
8. *Unless otherwise noted, address bits A19–A11 are don't care.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 6 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

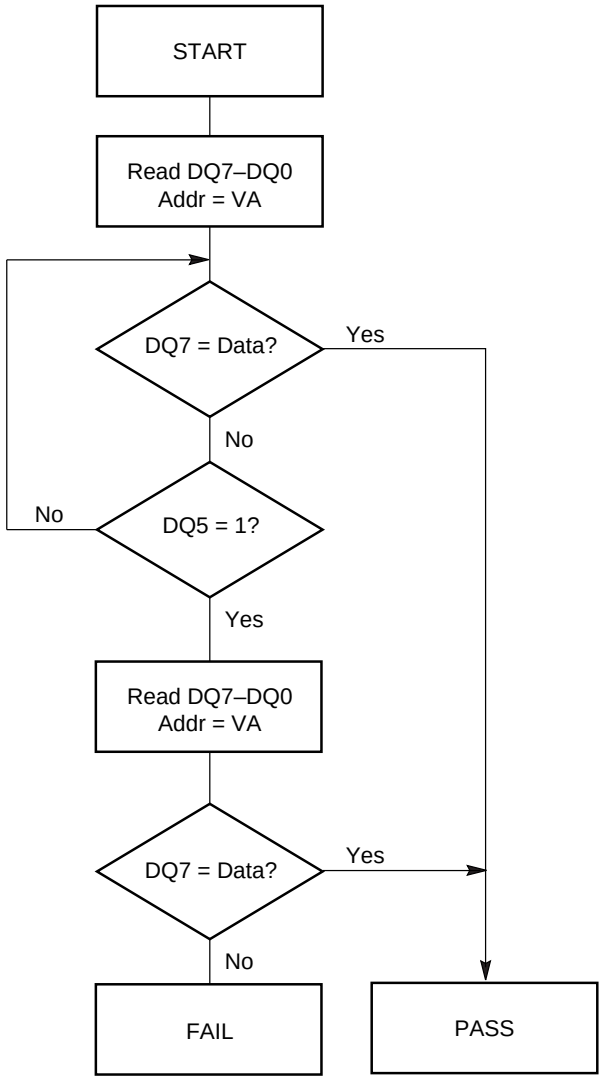
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. At the instant the device completes the Embedded Program or Erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 6 shows the outputs for Data# Polling on DQ7. Figure 4 shows the Data# Polling algorithm. Figure 13 in the AC Characteristics section shows the Data# Polling timing diagrams.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector group address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 4. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or the erase-suspend-read mode.

Table 6 shows the outputs for RY/BY#. The AC Characteristics section contains timing diagrams that show the waveforms for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 2 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 6 shows the outputs for Toggle Bit I on DQ6. Figure 5 shows the toggle bit algorithm. Figure 14 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 15 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. The device toggles DQ2 with each OE# or CE# read cycle.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for DQ2 and DQ6.

Figure 5 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 14 shows the toggle bit timing diagram. Figure 15 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 5 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system

must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 5)..

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed.

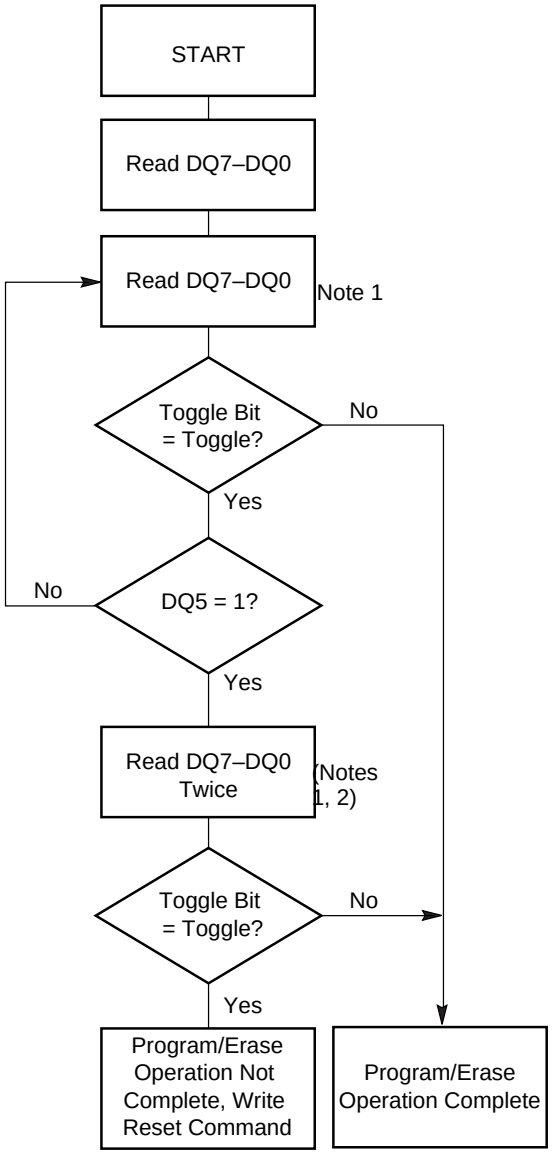
The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.”

Under both these conditions, the system must issue the reset command to return the device to the read mode (or to the erase-suspend-read mode if the device was previously in the erase-suspend program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from “0” to “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is “1”, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0”, the device will accept additional sector erase commands. To ensure the command has been accepted, the system



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to “1” . See text.*

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Figure 5. Toggle Bit Algorithm

software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 6 shows the outputs for DQ3.

Table 6. Write Operation Status

Operation			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +125°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –2.0 V to +7.0 V

A9, OE#, RESET# (Note 2) . . . . –2.0 V to +13.0 V

All other pins (Note 1) . . . . . –2.0 V to +7.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figures 6 and 7.*
2. *Minimum DC input voltage on A9, OE#, RESET# pins is –0.5 V. During voltage transitions, A9, OE#, RESET# pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9, OE#, and RESET# is 13.0 V which may overshoot to 13.5 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses greater than those listed in this section may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C). . . . . .0°C to +70°C

Industrial (I) Devices

Case Temperature (T_C). . . . . .–40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for Am29F080B-75 . . . . . +4.75 V to +5.25 V
V_{CC} for Am29F080B-90, 120, 150 +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

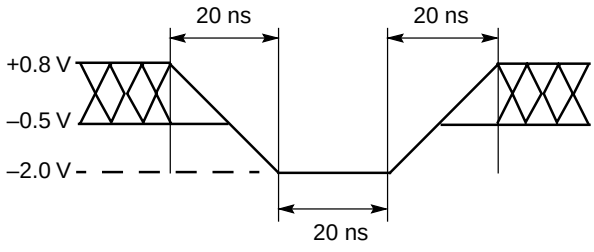


Figure 6. Maximum Negative Overshoot Waveform

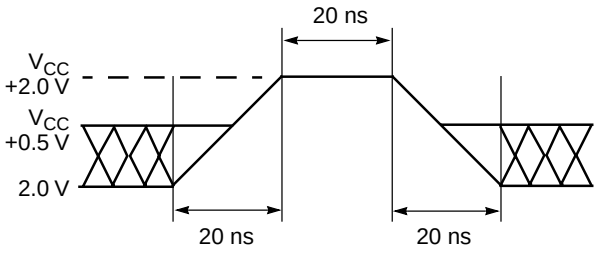


Figure 7. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.0 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}		25	40	mA
I_{CC2}	V_{CC} Write Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}		40	60	mA
I_{CC3}	V_{CC} Standby Current (CE# Controlled)	$V_{CC} = V_{CC}$ Max, CE# = V_{IH}, RESET# = V_{IH}		0.4	1.0	mA
I_{CC4}	V_{CC} Standby Current (RESET# Controlled)	$V_{CC} = V_{CC}$ Max, RESET# = V_{IL}		0.4	1.0	mA
V_{IL}	Input Low Level		–0.5		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V	11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH}	Output High Level	I_{OH} = –2.5 mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		4.2	V

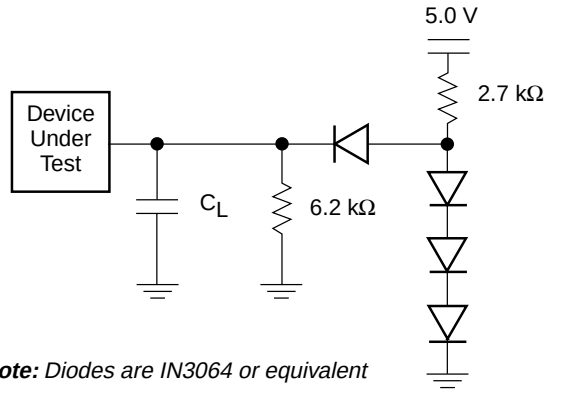
CMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.0 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}		25	40	mA
I_{CC2}	V_{CC} Write Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}		30	40	mA
I_{CC3}	V_{CC} Standby Current (CE# Controlled)	$V_{CC} = V_{CC}$ Max, CE# = V_{CC} ± 0.3 V, RESET# = V_{CC} ± 0.3 V		1	5	µA
I_{CC4}	V_{CC} Standby Current (RESET# Controlled)	$V_{CC} = V_{CC}$ Max, RESET# = V_{SS} ± 0.3 V		1	5	µA
V_{IL}	Input Low Level		–0.5		0.8	V
V_{IH}	Input High Level		0.7x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V	11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC} – 0.4			V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		4.2	V

Notes for DC Characteristics (both tables):

1. *The I_{CC} current listed includes is typically less than 1 mA/MHz, with OE# at V_{IH}.*
2. *I_{CC} active while Embedded Program or Embedded Erase algorithm is in progress.*
3. *Not 100% tested.*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

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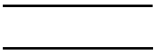
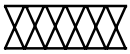
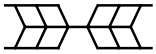
Figure 8. Test Setup

Table 7. Test Specifications

Test Condition	-75	All others	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5	20	ns
Input Pulse Levels	0.0–3.0	0.45–2.4	V
Input timing measurement reference levels	1.5	0.8, 2.0	V
Output timing measurement reference levels	1.5	0.8, 2.0	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

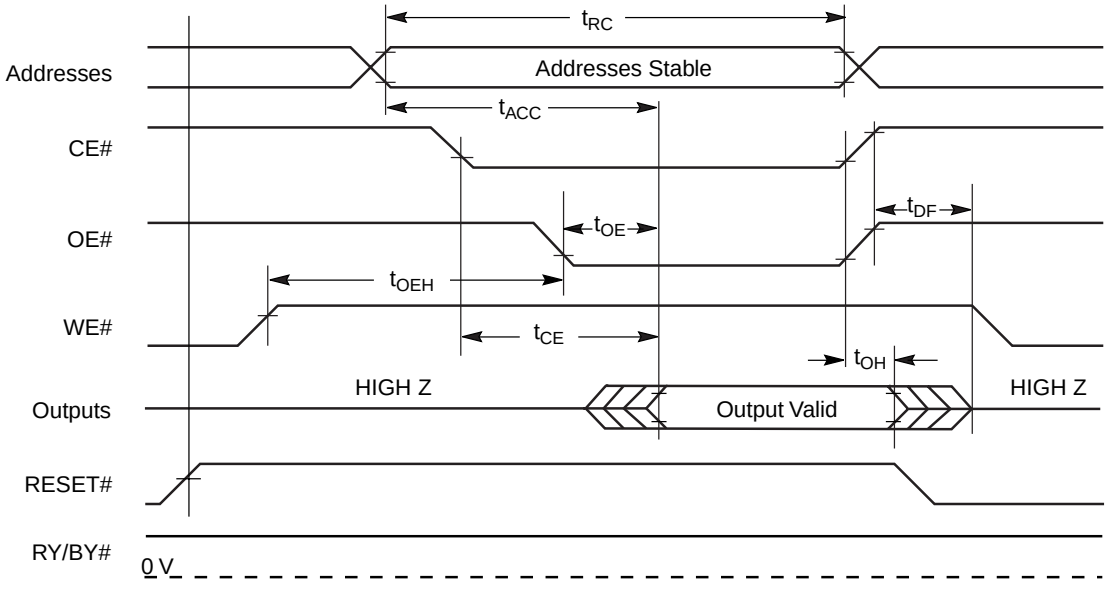
AC CHARACTERISTICS

Read-only Operations

Parameter Symbol		Parameter Description		Test Setup		Speed Options				Unit
JEDEC	Standard					-75	-90	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 2)			Min	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$CE\# = V_{IL}$ $OE\# = V_{IL}$	Max	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$OE\# = V_{IL}$	Max	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	40	40	50	55	ns
	t_{OEH}	Output Enable Hold Time (Note 2)	Read		Min	0	0	0	0	ns
			Toggle and Data# Polling		Min	10	10	10	10	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 2)			Max	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 2)			Max	20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses CE# or OE# Whichever Occurs First			Min	0	0	0	0	ns
	t_{Ready}	RESET# Pin Low to Read Mode (Note 2)			Max	20	20	20	20	µs

Notes:

1. *Output driver disable time.*
2. *Not 100% tested.*
3. *Refer to Figure 8 and Table 7 for test specifications.*



21503A-14

Figure 9. Read Operation Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note: *Not 100% tested.*

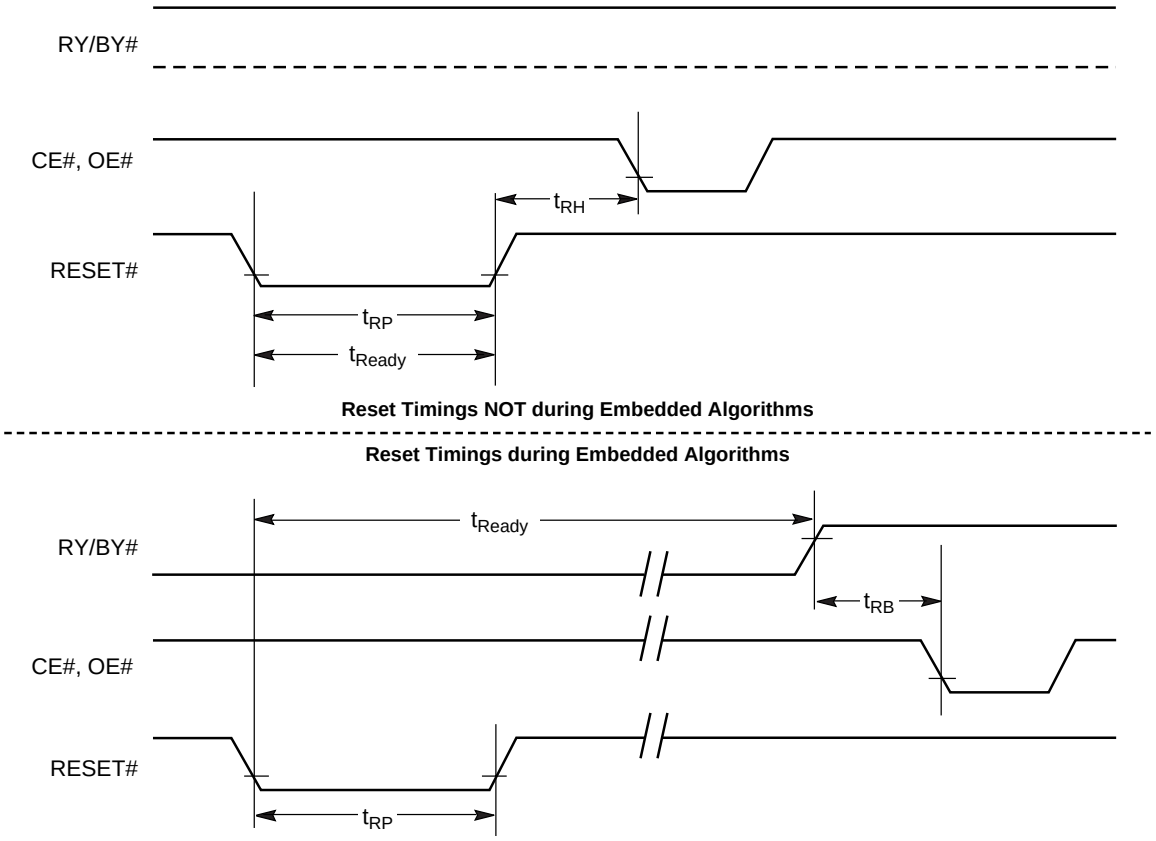


Figure 10. RESET# Timings

AC CHARACTERISTICS

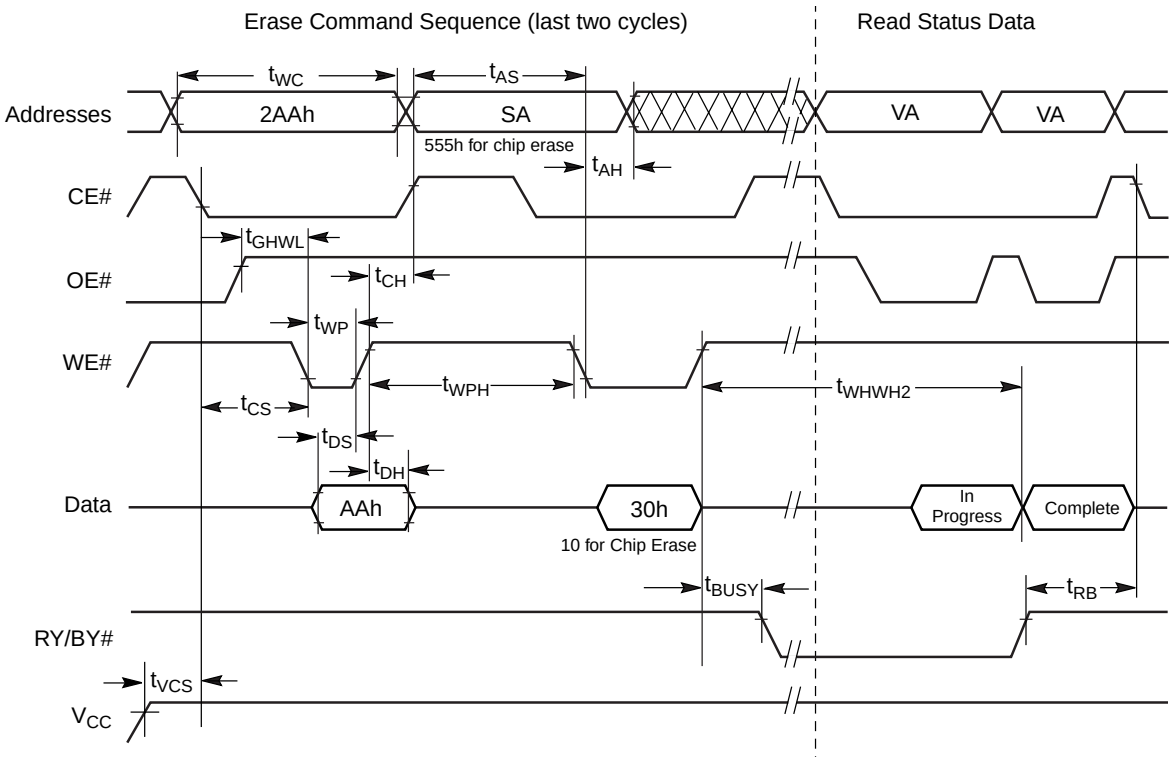
Write (Erase/Program) Operations

Parameter		Parameter Description		Speed Options				Unit
JEDEC	Std			-75	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write (OE# high to WE# low)	Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	7	7	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1	1	1	1	sec
			Max	8	8	8	8	sec
	t_{VCS}	V_{CC} Set Up Time (Note 1)	Min	50	50	50	50	µs
	t_{OES}	Output Enable Setup Time (Note 2)	Min	0	0	0	0	ns
	t_{BUSY}	WE# to RY/BY# Valid	Min	40	40	50	60	ns
	t_{RP}	RESET# Pulse Width	Min	500	500	500	500	ns
	t_{VIDR}	V_{ID} Rise and Fall Time for Temporary Sector Unprotect (Note 1)	Min	500	500	500	500	ns

Notes:

1. *Not 100% tested.*
2. *This does not include the preprogramming time.*

AC CHARACTERISTICS

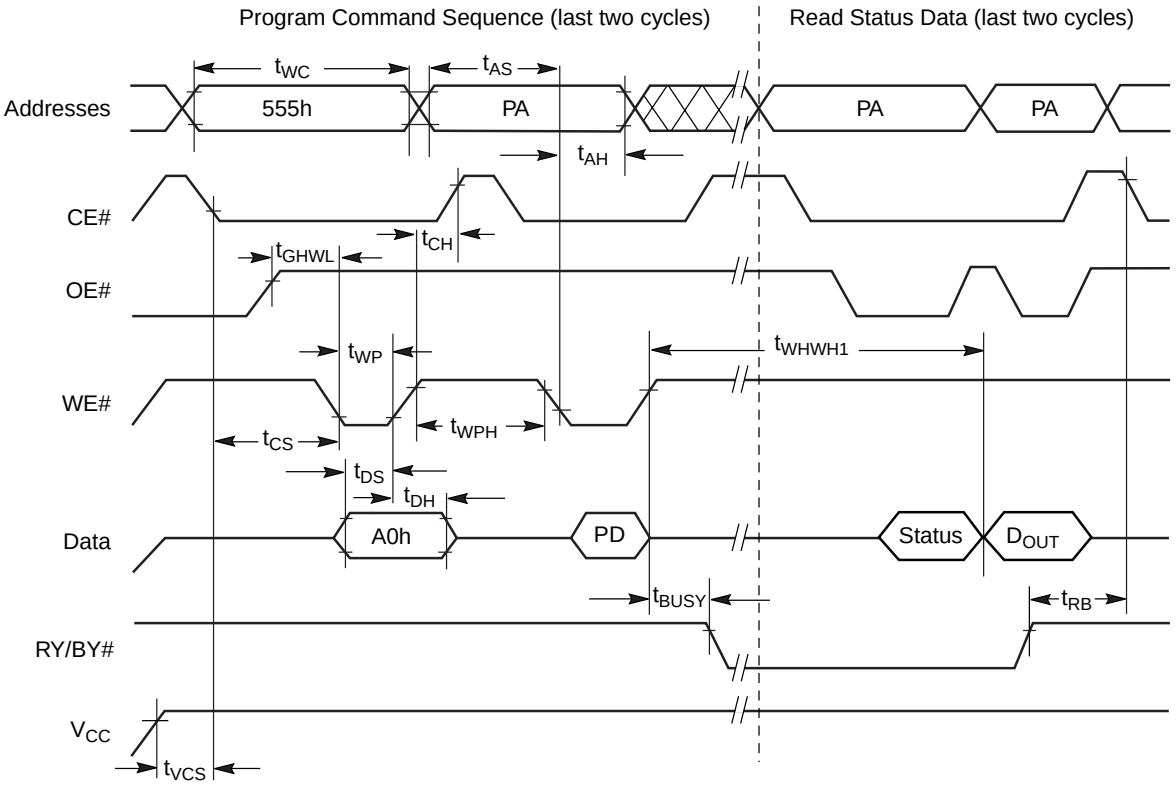


Note: *SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase. Address and data values are in hexadecimal.*

21503A-16

Figure 11. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS



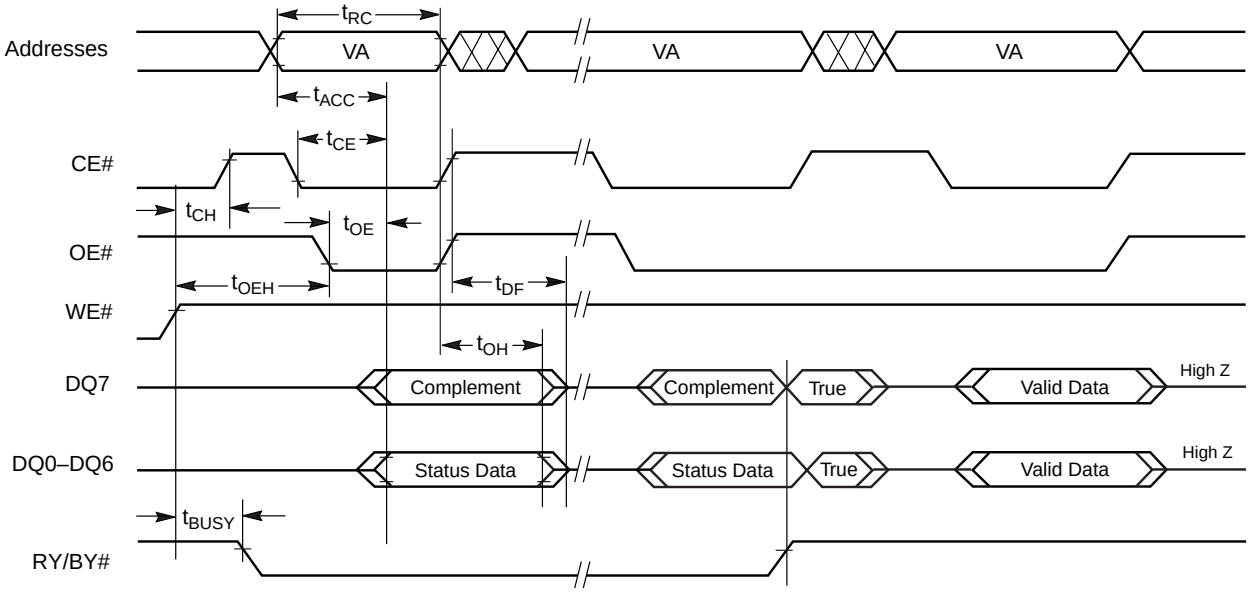
Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in byte mode.*

21503A-17

Figure 12. Program Operation Timings

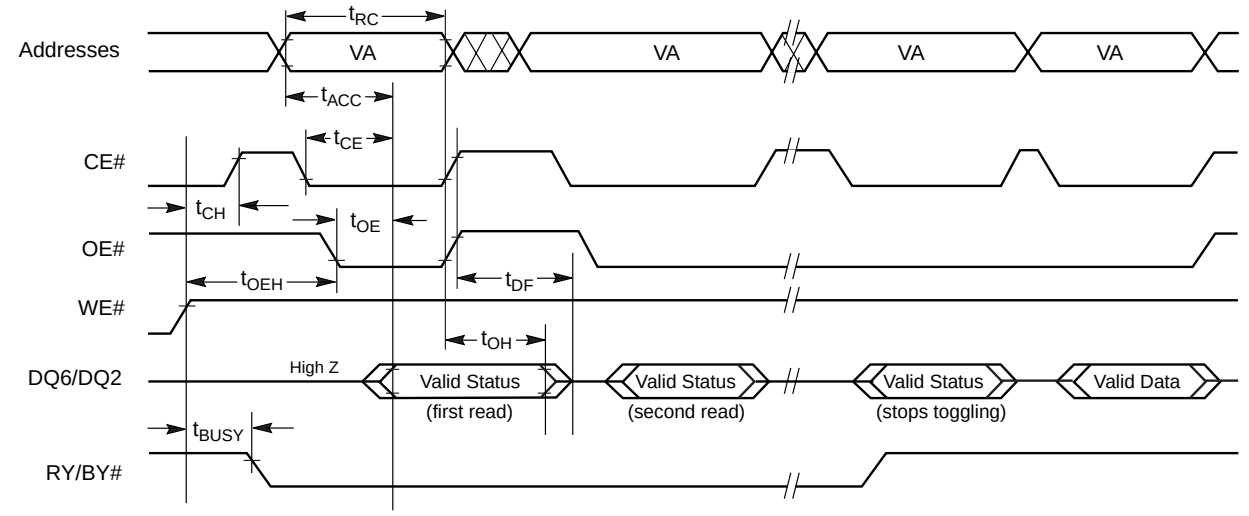
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

21503A-18

Figure 13. Data# Polling Timings (During Embedded Algorithms)

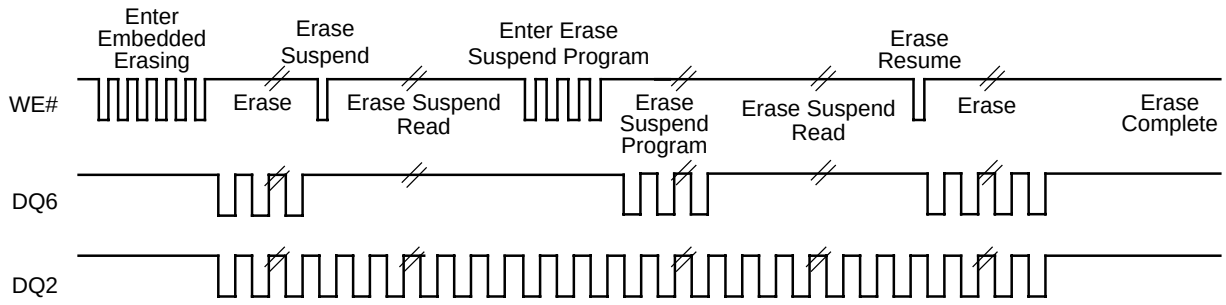


Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

21503A-19

Figure 14. Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS



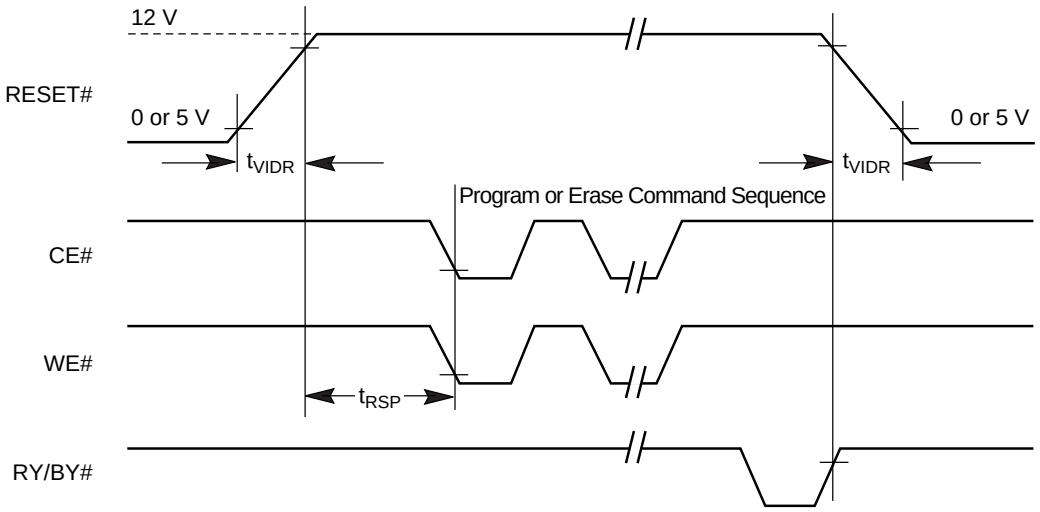
Note: *The system may use OE# or CE# to toggle DQ2 and DQ6. DQ2 must be read at an address within the erase-suspended sector.*

21503A-20

Figure 15. DQ2 vs. DQ6

Temporary Sector Unprotect

Parameter					
JEDEC	**Std.**	**Description**		**All Speed Options**	**Unit**
	t_{VIDR}	V_{ID} Rise and Fall Time	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs



21503A-21

Figure 16. Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS

Write (Erase/Program) Operations

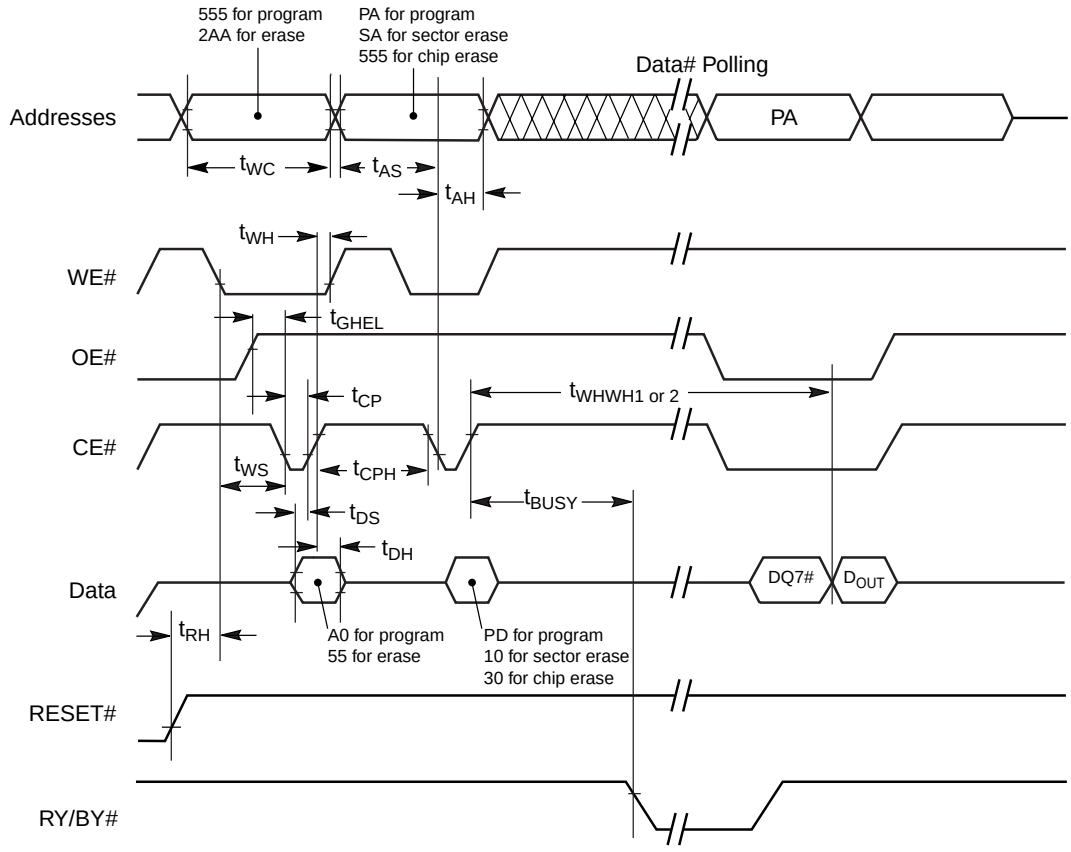
Alternate CE# Controlled Writes

Parameter Symbol		Parameter Description		Speed Options				Unit
JEDEC	Standard			-75	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	40	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	40	45	50	50	ns
t_{EHDX}	t_{DH}	Address Hold Time	Min	0	0	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	CE# Setup Time	Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	CE# Hold Time	Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min	40	45	50	50	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	7	7	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ	1	1	1	1	sec
			Max	8	8	8	8	sec

Notes:

1. *This does not include the preprogramming time.*
2. *Not 100% tested.*

AC CHARACTERISTICS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *DQ7# is the complement of the data written to the device.*
4. *D_{OUT} is the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

21503A-22

Figure 17. Alternate CE# Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	1	8	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	16	128	sec	
Byte Programming Time	7	300	µs	Excludes system-level overhead (Note 5)
Chip Programming Time (Note 3)	7.2	21.6	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 5.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 4.5 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed. If the maximum byte program time given is exceeded, only then does the device set DQ5 = 1. See the section on DQ5 for further information.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the four-bus-cycle sequence for programming. See Table 5 for further information on command definitions.*
6. *The device has a typical erase and program cycle endurance of 1,000,000 cycles. 100,000 cycles are guaranteed.*

LATCHUP CHARACTERISTIC

	Min	Max
Input Voltage with respect to V_{SS} on I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 Volt, one pin at a time.

TSOP AND SO PIN CAPACITANCE

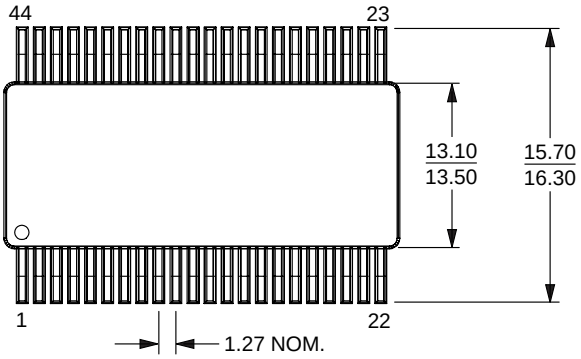
Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

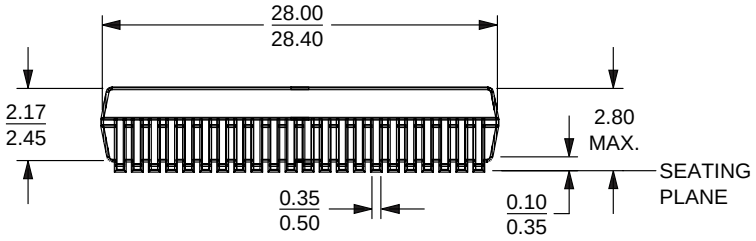
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PHYSICAL DIMENSIONS

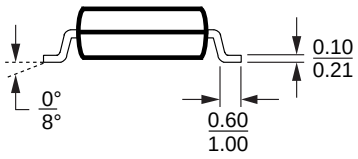
SO 044—44-Pin Small Outline Package (measured in millimeters)



TOP VIEW



SIDE VIEW

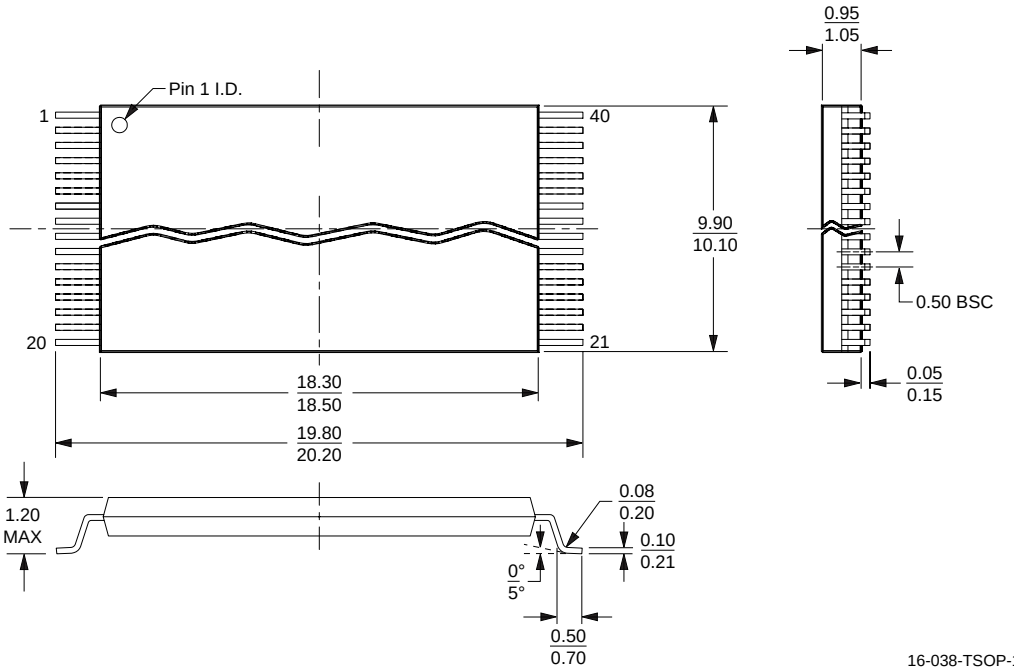


END VIEW

16-038-SO44-2
SO 044
DF83
8-8-96 lv

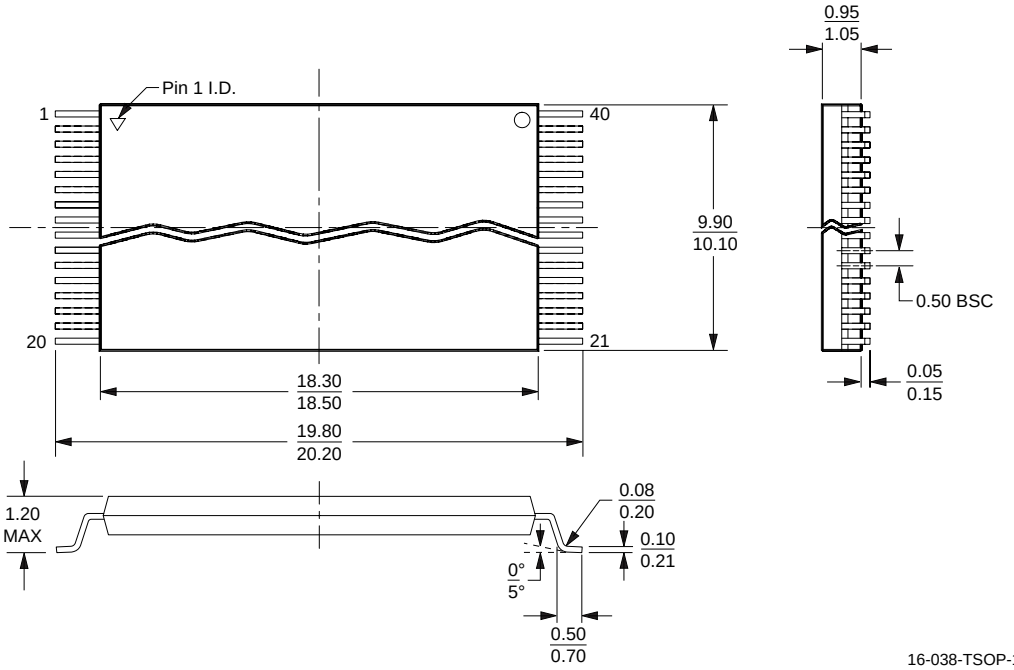
PHYSICAL DIMENSIONS

TS 040—40-Pin Standard Thin Small Outline Package



16-038-TSOP-1_AE
TS 040
2-27-97 lv

TSR040—40-Pin Reverse Thin Small Outline Package



16-038-TSOP-1_AE
TSR040
2-27-97 lv