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# HM628128A Series

131,072-word  $\times$  8-bit High Speed CMOS Static RAM

# HITACHI

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## Description

The Hitachi HM628128A is a CMOS static RAM organized 128-kword  $\times$  8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8  $\mu\text{m}$  Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8  $\times$  20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

## Features

- High speed
  - Fast access time: 55/70/85/100 ns (max)
- Low power
  - Active: 75 mW (typ)
  - Standby: 10  $\mu\text{W}$  (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery backup operation
  - 2 chip selection for battery backup

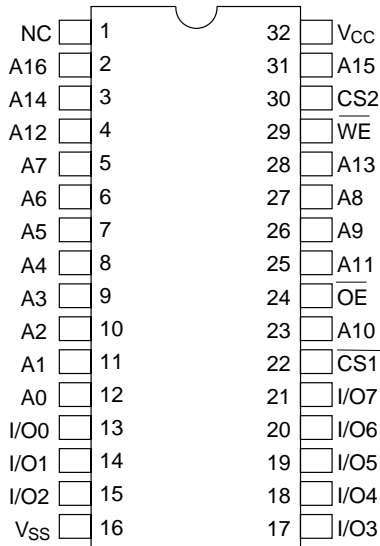
# HM628128A Series

## Ordering Information

| Type No.          | Access Time | Package  |
|-------------------|-------------|--|
| HM628128ALP-5     | 55 ns       | 600-mil 32-pin plastic DIP (DP-32)                 |
| HM628128ALP-7     | 70 ns       |  |
| HM628128ALP-8     | 85 ns       |  |
| HM628128ALP-10    | 100 ns      |  |
| HM628128ALP-5SL   | 55 ns       |  |
| HM628128ALP-7SL   | 70 ns       |  |
| HM628128ALP-8SL   | 85 ns       |  |
| HM628128ALP-10SL  | 100 ns      |  |
| HM628128ALFP-5    | 55 ns       | 525-mil 32-pin plastic SOP (FP-32D)                |
| HM628128ALFP-7    | 70 ns       |  |
| HM628128ALFP-8    | 85 ns       |  |
| HM628128ALFP-10   | 100 ns      |  |
| HM628128ALFP-5SL  | 55 ns       |  |
| HM628128ALFP-7SL  | 70 ns       |  |
| HM628128ALFP-8SL  | 85 ns       |  |
| HM628128ALFP-10SL | 100 ns      |  |
| HM628128ALT-5     | 55 ns       | 8 mm × 20 mm 32-pin TSOP (normal type) (TFP-32D)   |
| HM628128ALT-7     | 70 ns       |  |
| HM628128ALT-8     | 85 ns       |  |
| HM628128ALT-10    | 100 ns      |  |
| HM628128ALT-5SL   | 55 ns       |  |
| HM628128ALT-7SL   | 70 ns       |  |
| HM628128ALT-8SL   | 85 ns       |  |
| HM628128ALT-10SL  | 100 ns      |  |
| HM628128ALR-5     | 55 ns       | 8 mm × 20 mm 32-pin TSOP (reverse type) (TFP-32DR) |
| HM628128ALR-7     | 70 ns       |  |
| HM628128ALR-8     | 85 ns       |  |
| HM628128ALR-10    | 100 ns      |  |
| HM628128ALR-5SL   | 55 ns       |  |
| HM628128ALR-7SL   | 70 ns       |  |
| HM628128ALR-8SL   | 85 ns       |  |
| HM628128ALR-10SL  | 100 ns      |  |

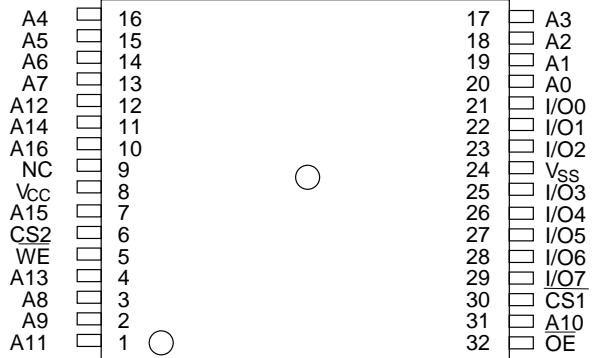
## Pin Arrangement

HM628128ALP/ALFP Series



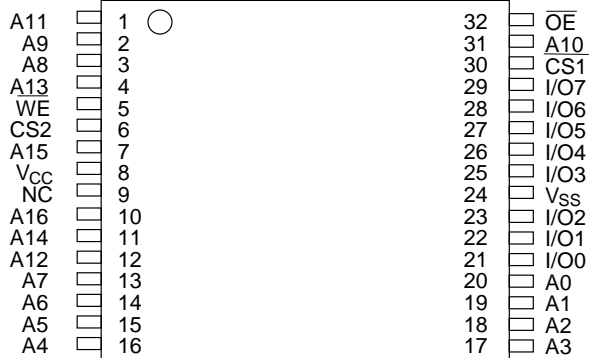
(Top View)

HM628128ALT Series



(Top View)

HM628128ALR Series

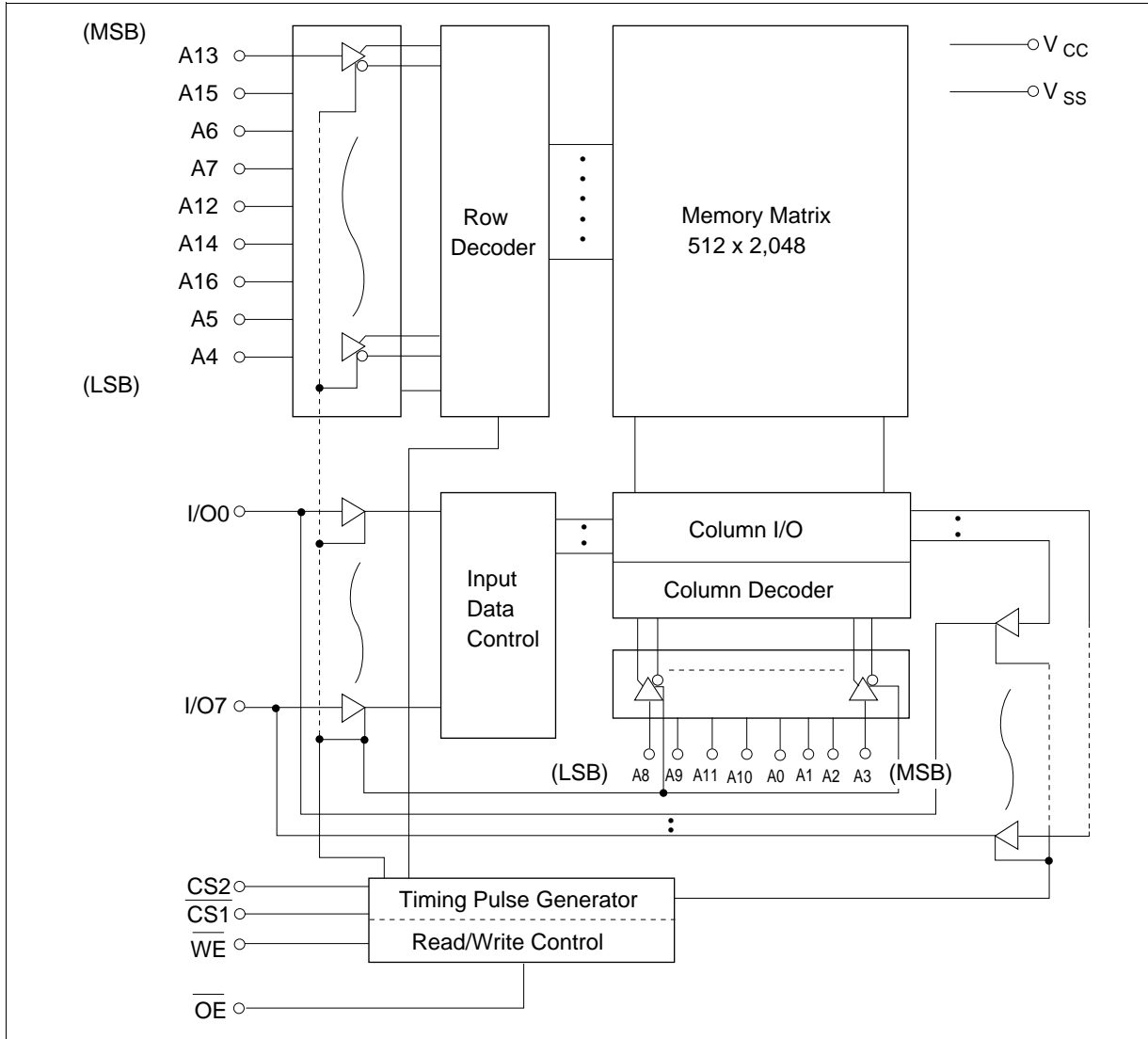


(Top View)

## Pin Description

| Pin Name         | Function      |
|------------------|---------------|
| A0 – A16         | Address       |
| I/O0 – I/O7      | Input/output  |
| $\overline{CS1}$ | Chip select 1 |
| CS2              | Chip select 2 |
| $\overline{WE}$  | Write enable  |
| $\overline{OE}$  | Output enable |
| NC               | No connection |
| $V_{CC}$         | Power supply  |
| $V_{SS}$         | Ground        |

## Block Diagram



**Function Table**

| CS1 | CS2 | OE | WE | Mode           | V <sub>CC</sub> Current            | I/O Pin | Ref. Cycle      |
|-----|-----|----|----|----------------|------------------------------------|---------|-----------------|
| H   | X   | X  | X  | Standby        | I <sub>SB</sub> , I <sub>SB1</sub> | High-Z  | —               |
| X   | L   | X  | X  | Standby        | I <sub>SB</sub> , I <sub>SB1</sub> | High-Z  | —               |
| L   | H   | H  | H  | Output disable | I <sub>CC</sub>                    | High-Z  | —               |
| L   | H   | L  | H  | Read           | I <sub>CC</sub>                    | Dout    | Read cycle      |
| L   | H   | H  | L  | Write          | I <sub>CC</sub>                    | Din     | Write cycle (1) |
| L   | H   | L  | L  | Write          | I <sub>CC</sub>                    | Din     | Write cycle (2) |

Note: X: H or L

**Absolute Maximum Ratings**

| Parameter  | Symbol            | Value   | Unit |
|--|-------------------|---|------|
| Supply voltage relative to V <sub>SS</sub>                   | V <sub>CC</sub>   | -0.5 to +7.0  | V    |
| Voltage on any pin relative to V <sub>SS</sub> <sup>*1</sup> | V <sub>T</sub>    | -0.5 <sup>*2</sup> to V <sub>CC</sub> + 0.3 <sup>*3</sup> | V    |
| Power dissipation  | P <sub>T</sub>    | 1.0   | W    |
| Operating temperature  | T <sub>opr</sub>  | 0 to +70  | °C   |
| Storage temperature  | T <sub>stg</sub>  | -55 to +125   | °C   |
| Storage temperature under bias                               | T <sub>bias</sub> | -10 to +85  | °C   |

- Notes: 1. With respect to V<sub>SS</sub>  
 2. -3.0 V for pulse half-width ≤ 30 ns  
 3. Maximum voltage is 7.0V.

**Recommended DC Operating Conditions (T<sub>a</sub> = 0 to +70°C)**

| Parameter                        | Symbol          | Min                | Typ | Max                   | Unit |
|----------------------------------|-----------------|--------------------|-----|-----------------------|------|
| Supply voltage                   | V <sub>CC</sub> | 4.5                | 5.0 | 5.5                   | V    |
|                                  | V <sub>SS</sub> | 0                  | 0   | 0                     | V    |
| Input voltage (HM628128A-7/8/10) | V <sub>IH</sub> | 2.2                | —   | V <sub>CC</sub> + 0.3 | V    |
|                                  | V <sub>IL</sub> | -0.3 <sup>*1</sup> | —   | 0.8                   | V    |
| Input voltage (HM628128A-5)      | V <sub>IH</sub> | 2.4                | —   | V <sub>CC</sub> + 0.3 | V    |
|                                  | V <sub>IL</sub> | -0.3 <sup>*1</sup> | —   | 0.8                   | V    |

- Note: 1. -3.0 V for pulse half-width ≤ 30 ns

# HM628128A Series

## DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

| Parameter                            | Symbol                              | Min | Typ <sup>*1</sup> | Max | Unit | Test Conditions   |
|--------------------------------------|-------------------------------------|-----|-------------------|-----|------|---|
| Input leakage current                | I <sub>LI</sub>                     | —   | —                 | 1.0 | μA   | V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>  |
| Output leakage current               | I <sub>LO</sub>                     | —   | —                 | 1.0 | μA   | $\overline{CS1} = V_{IH}$ or CS2 = V <sub>IL</sub> or<br>OE = V <sub>IH</sub> or WE = V <sub>IL</sub> ,<br>V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>                                |
| Operating power supply current: DC   | I <sub>CC</sub>                     | —   | 15                | 30  | mA   | $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> ,<br>Others = V <sub>IH</sub> /V <sub>IL</sub><br>I <sub>I/O</sub> = 0 mA   |
| Operating power supply current       | I <sub>CC1</sub> (HM628128A-7/8/10) | —   | 45                | 70  | mA   | Min cycle, duty = 100%,<br>$\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> ,<br>Others = V <sub>IH</sub> /V <sub>IL</sub><br>I <sub>I/O</sub> = 0 mA  |
|                                      | I <sub>CC1</sub> (HM628128A-5)      | —   | 50                | 80  | mA   |   |
|                                      | I <sub>CC2</sub>                    | —   | 15                | 25  | mA   | Cycle time = 1 μs, duty = 100%,<br>I <sub>I/O</sub> = 0 mA, $\overline{CS1} \leq 0.2$ V,<br>CS2 ≥ V <sub>CC</sub> - 0.2 V<br>V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IL</sub> ≤ 0.2 V |
| Standby power supply current: DC     | I <sub>SB</sub>                     | —   | 1                 | 2   | mA   | (1) $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IH</sub> or<br>(2) CS2 = V <sub>IL</sub>   |
| Standby power supply current (1): DC | I <sub>SB1</sub> (L-version)        | —   | 2                 | 100 | μA   | 0 V ≤ V <sub>in</sub> ≤ V <sub>CC</sub> ,<br>(1) $\overline{CS1} \geq V_{CC} - 0.2$ V,<br>(2) CS2 ≥ V <sub>CC</sub> - 0.2 V or ,<br>0 V ≤ CS2 ≤ 0.2 V   |
|                                      | I <sub>SB1</sub> (L-SL version)     | —   | 2                 | 50  | μA   |   |
| Output voltage                       | V <sub>OL</sub>                     | —   | —                 | 0.4 | V    | I <sub>OL</sub> = 2.1 mA  |
|                                      | V <sub>OH</sub>                     | 2.4 | —                 | —   | V    | I <sub>OH</sub> = -1.0 mA   |

Note: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.

## Capacitance (Ta = 25°C, f = 1.0 MHz)<sup>\*1</sup>

| Parameter                | Symbol           | Min | Typ | Max | Unit | Test Conditions        |
|--------------------------|------------------|-----|-----|-----|------|------------------------|
| Input capacitance        | C <sub>in</sub>  | —   | —   | 8   | pF   | V <sub>in</sub> = 0 V  |
| Input/output capacitance | C <sub>I/O</sub> | —   | —   | 10  | pF   | V <sub>I/O</sub> = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ , unless otherwise noted.)

**Test Conditions**

- Input pulse levels: 0.8 V to 2.4 V (HM628128A-7/8/10)  
0 V to 3 V (HM628128A-5)
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100 pF) (HM628128A-7/8/10)  
1 TTL Gate and CL (30 pF) (HM628128A-5) (Including scope & jig)

**Read Cycle**

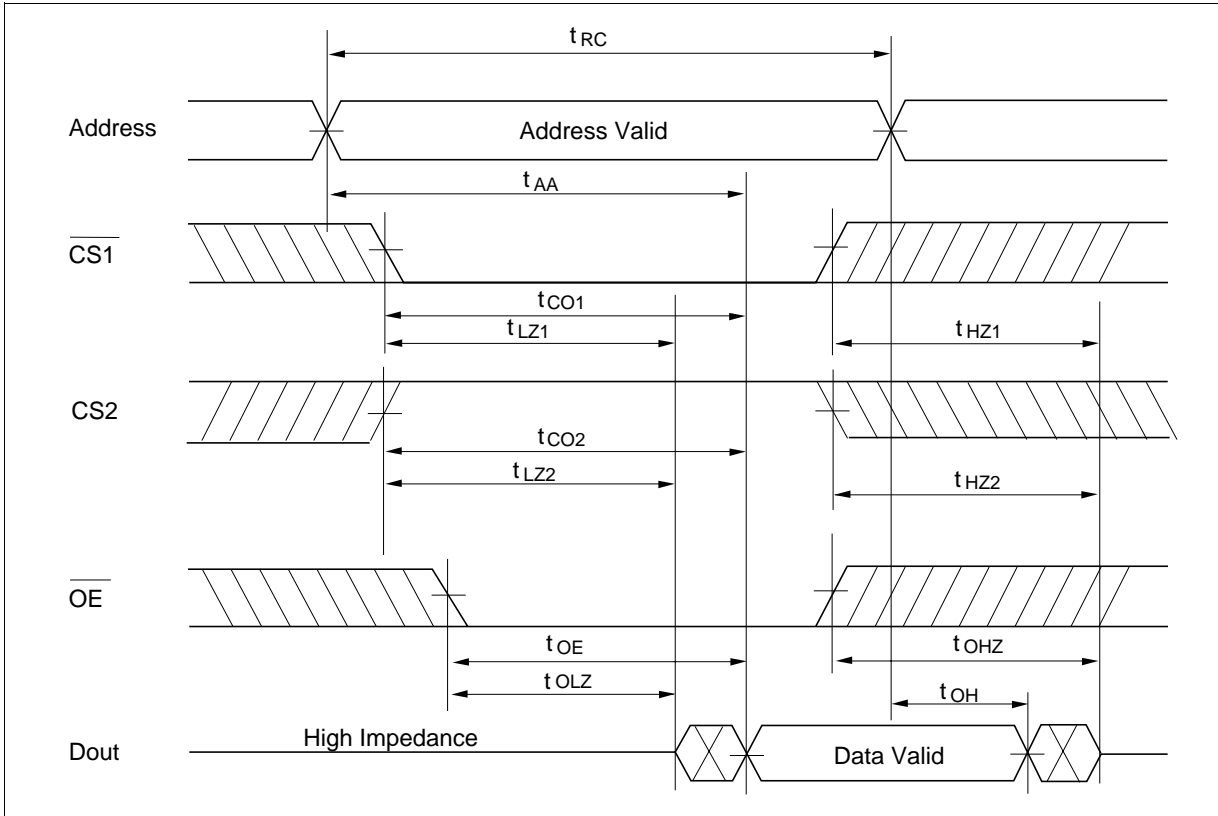
|                                      |           | HM628128A |     |     |     |     |     |     |     |      |         |
|--------------------------------------|-----------|-----------|-----|-----|-----|-----|-----|-----|-----|------|---------|
|                                      |           | -5        |     | -7  |     | -8  |     | -10 |     |      |         |
| Parameter                            | Symbol    | Min       | Max | Min | Max | Min | Max | Min | Max | Unit | Notes   |
| Read cycle time                      | $t_{RC}$  | 55        | —   | 70  | —   | 85  | —   | 100 | —   | ns   |         |
| Address access time                  | $t_{AA}$  | —         | 55  | —   | 70  | —   | 85  | —   | 100 | ns   |         |
| Chip selection to output valid       | $t_{CO1}$ | —         | 55  | —   | 70  | —   | 85  | —   | 100 | ns   |         |
|                                      | $t_{CO2}$ | —         | 55  | —   | 70  | —   | 85  | —   | 100 | ns   |         |
| Output enable to output valid        | $t_{OE}$  | —         | 30  | —   | 35  | —   | 45  | —   | 50  | ns   |         |
| Chip selection to output in low-Z    | $t_{LZ1}$ | 5         | —   | 10  | —   | 10  | —   | 10  | —   | ns   | 2, 3    |
|                                      | $t_{LZ2}$ | 5         | —   | 10  | —   | 10  | —   | 10  | —   | ns   | 2, 3    |
| Output enable to output in low-Z     | $t_{OLZ}$ | 5         | —   | 5   | —   | 5   | —   | 5   | —   | ns   | 2, 3    |
| Chip deselection to output in high-Z | $t_{HZ1}$ | 0         | 20  | 0   | 25  | 0   | 30  | 0   | 35  | ns   | 1, 2, 3 |
|                                      | $t_{HZ2}$ | 0         | 20  | 0   | 25  | 0   | 30  | 0   | 35  | ns   | 1, 2, 3 |
| Output disable to output in high-Z   | $t_{OHZ}$ | 0         | 20  | 0   | 25  | 0   | 30  | 0   | 35  | ns   | 1, 2, 3 |
| Output hold from address change      | $t_{OH}$  | 5         | —   | 10  | —   | 10  | —   | 10  | —   | ns   |         |

Notes: 1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.

3. This parameter is sampled and not 100% tested.

## Read Timing Waveform ( $\overline{WE} = V_{IH}$ )





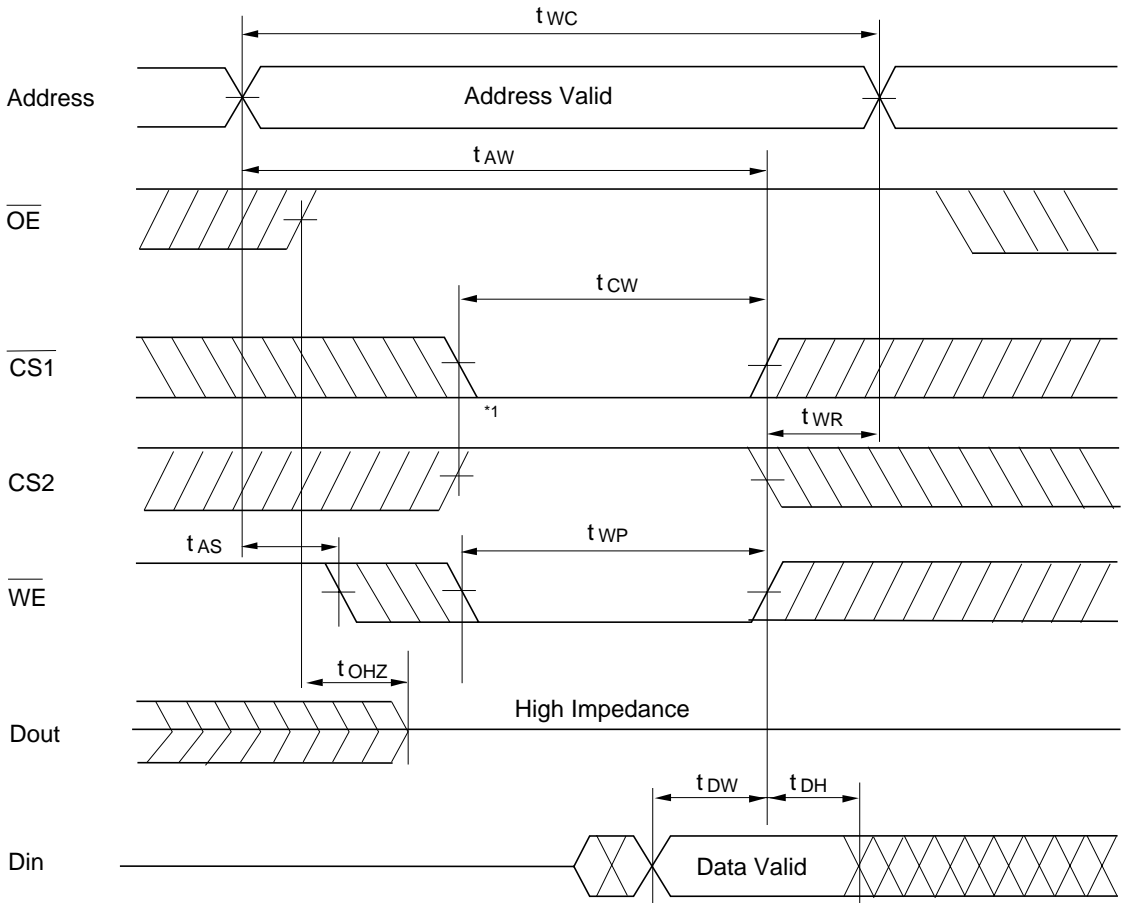
Write Cycle

|                                    |           | HM628128A |     |     |     |     |     |     |     |      |       |
|------------------------------------|-----------|-----------|-----|-----|-----|-----|-----|-----|-----|------|-------|
|                                    |           | -5        |     | -7  |     | -8  |     | -10 |     |      |       |
| Parameter                          | Symbol    | Min       | Max | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Write cycle time                   | $t_{WC}$  | 55        | —   | 70  | —   | 85  | —   | 100 | —   | ns   |       |
| Chip selection to end of write     | $t_{CW}$  | 50        | —   | 60  | —   | 75  | —   | 80  | —   | ns   | 2     |
| Address setup time                 | $t_{AS}$  | 0         | —   | 0   | —   | 0   | —   | 0   | —   | ns   | 3     |
| Address valid to end of write      | $t_{AW}$  | 50        | —   | 60  | —   | 75  | —   | 80  | —   | ns   |       |
| Write pulse width                  | $t_{WP}$  | 40        | —   | 50  | —   | 55  | —   | 60  | —   | ns   | 1, 7  |
| Write recovery time                | $t_{WR}$  | 0         | —   | 0   | —   | 0   | —   | 0   | —   | ns   | 4     |
| Write to output in high-Z          | $t_{WHZ}$ | 0         | 20  | 0   | 25  | 0   | 30  | 0   | 35  | ns   | 5, 6  |
| Data to write time overlap         | $t_{DW}$  | 25        | —   | 30  | —   | 35  | —   | 40  | —   | ns   |       |
| Data hold from write time          | $t_{DH}$  | 0         | —   | 0   | —   | 0   | —   | 0   | —   | ns   |       |
| Output active from end of write    | $t_{OW}$  | 5         | —   | 5   | —   | 5   | —   | 5   | —   | ns   | 6     |
| Output disable to output in High-Z | $t_{OHZ}$ | 0         | 20  | 0   | 25  | 0   | 30  | 0   | 35  | ns   | 5     |

- Notes:
1. A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2, and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high, and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low, and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  2.  $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
  3.  $t_{AS}$  is measured from the address valid to the beginning of write.
  4.  $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.
  5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
  6. This parameter is sampled and not 100% tested.
  7. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ mix}$

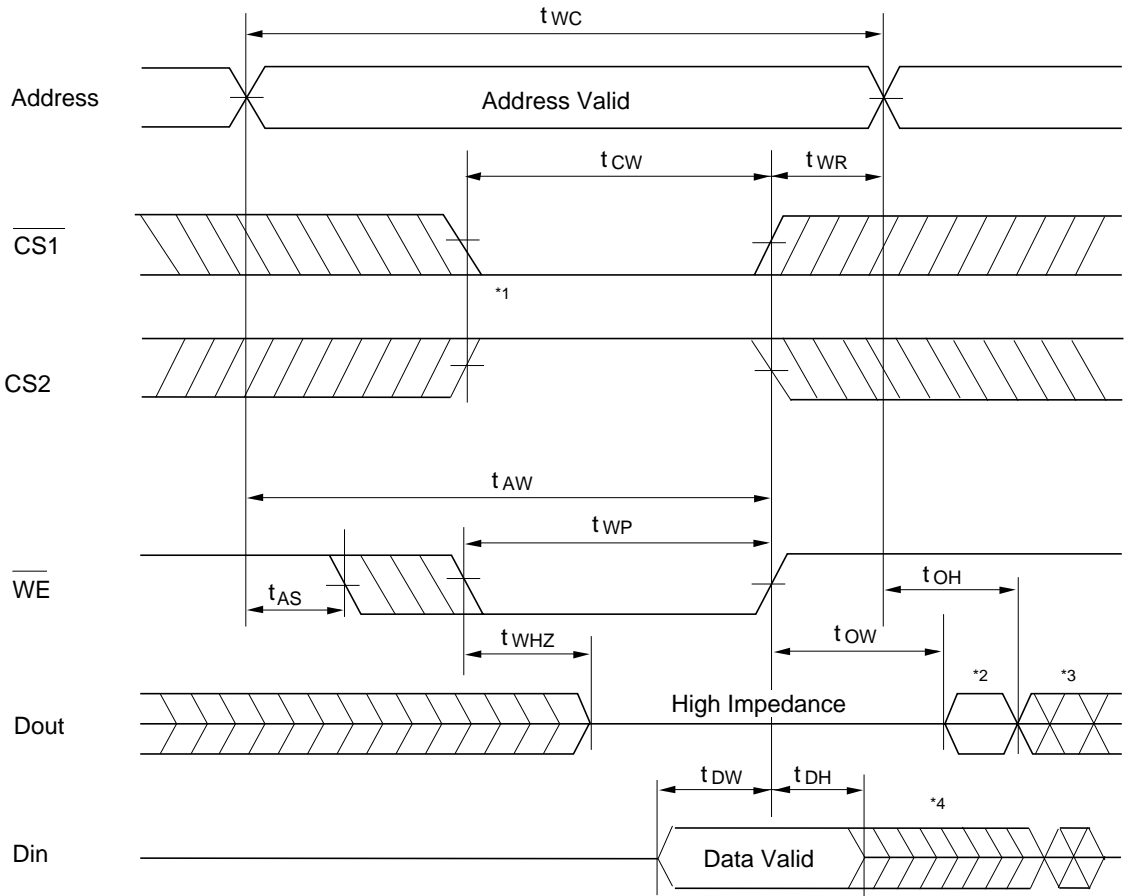
# HM628128A Series

## Write Timing Waveform (1) ( $\overline{OE}$ Clock)



Notes: 1. If the  $\overline{CS1}$  goes low simultaneously with  $\overline{WE}$  going low or after the  $\overline{WE}$  going low, the outputs remain in a high impedance state.

Write Timing Waveform (2) ( $\overline{OE}$  low Fixed)



## Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

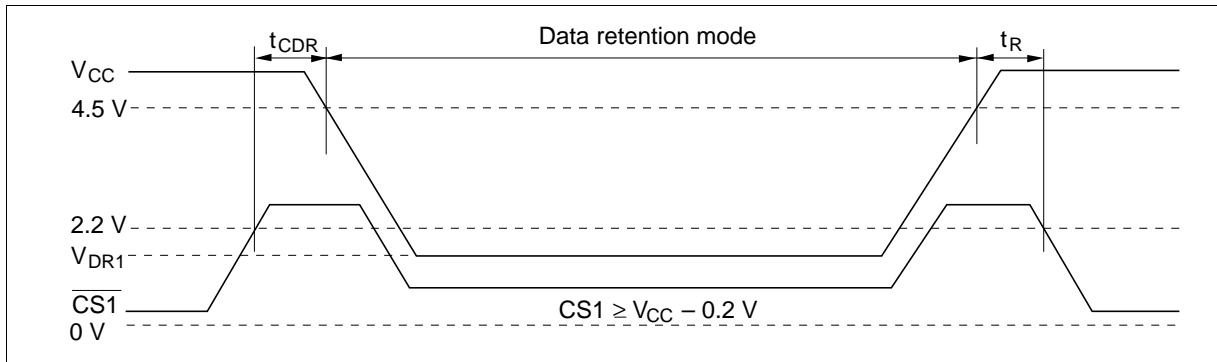
| Parameter                            | Symbol                    | Min | Typ | Max       | Unit          | Test Conditions <sup>3</sup>  |
|--------------------------------------|---------------------------|-----|-----|-----------|---------------|---|
| $V_{CC}$ for data retention          | $V_{DR}$                  | 2.0 | —   | —         | V             | $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$ , $CS2 \geq V_{CC} - 0.2\text{ V}$<br>or<br>$0\text{ V} \leq CS2 \leq 0.2\text{ V}$<br>$V_{in} > 0\text{ V}$                            |
| Data retention current               | $I_{CCDR}$ (L-version)    | —   | 1   | $50^{-1}$ | $\mu\text{A}$ | $V_{CC} = 3.0\text{ V}$ , $V_{in} \geq 0\text{ V}$<br>$\overline{CS1} \geq V_{CC} - 0.2\text{ V}$<br>$CS2 \geq V_{CC} - 0.2\text{ V}$ or<br>$0\text{ V} \leq CS2 \leq 0.2\text{ V}$ |
|                                      | $I_{CCDR}$ (L-SL version) | —   | 1   | $15^{-2}$ | $\mu\text{A}$ |   |
| Chip deselect to data retention time | $t_{CDR}$                 | 0   | —   | —         | ns            | See retention waveform  |
| Operation recovery time              | $t_R$                     | 5   | —   | —         | ms            |   |

Notes: 1.  $20\ \mu\text{A}$  max at  $T_a = 0$  to  $40^\circ\text{C}$  (L-version).

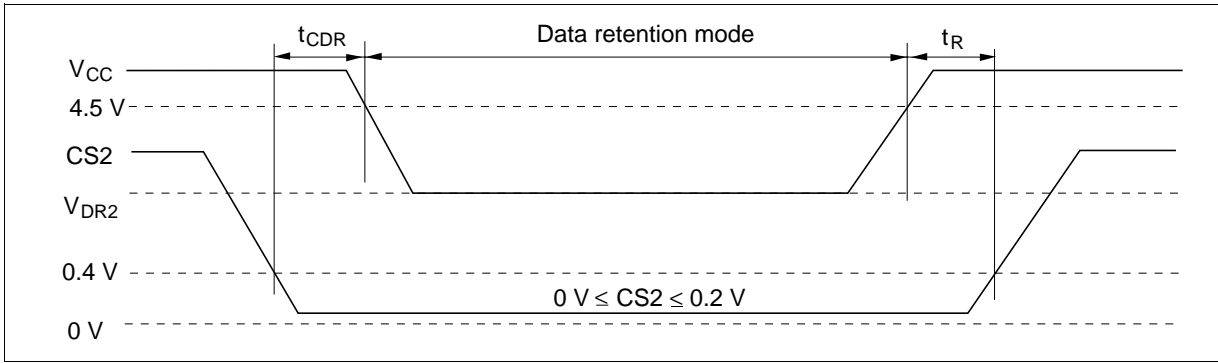
2.  $3\ \mu\text{A}$  max at  $T_a = 0$  to  $40^\circ\text{C}$  (L-SL-version).

3.  $\overline{CS2}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{CS1}$  buffer,  $\overline{OE}$  buffer, and  $D_{in}$  buffer. If  $\overline{CS2}$  controls data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CS1}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode,  $\overline{CS2}$  must be  $CS2 \geq V_{CC} - 0.2\text{ V}$  or  $0\text{ V} \leq CS2 \leq 0.2\text{ V}$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.

### Low $V_{CC}$ Data Retention Timing Waveform (1) ( $\overline{CS1}$ Controlled)



Low  $V_{CC}$  Data Retention Timing Waveform (2) (CS2 Controlled)

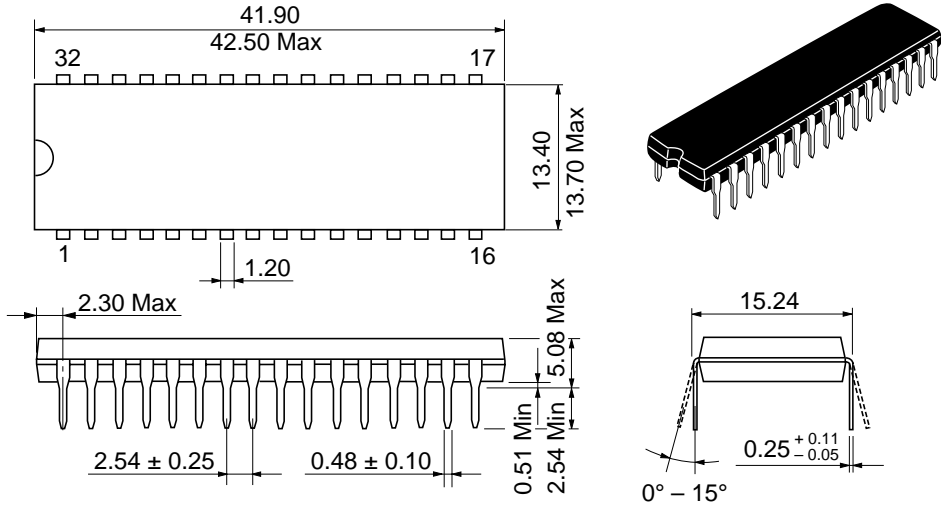


# HM628128A Series

## Package Dimensions

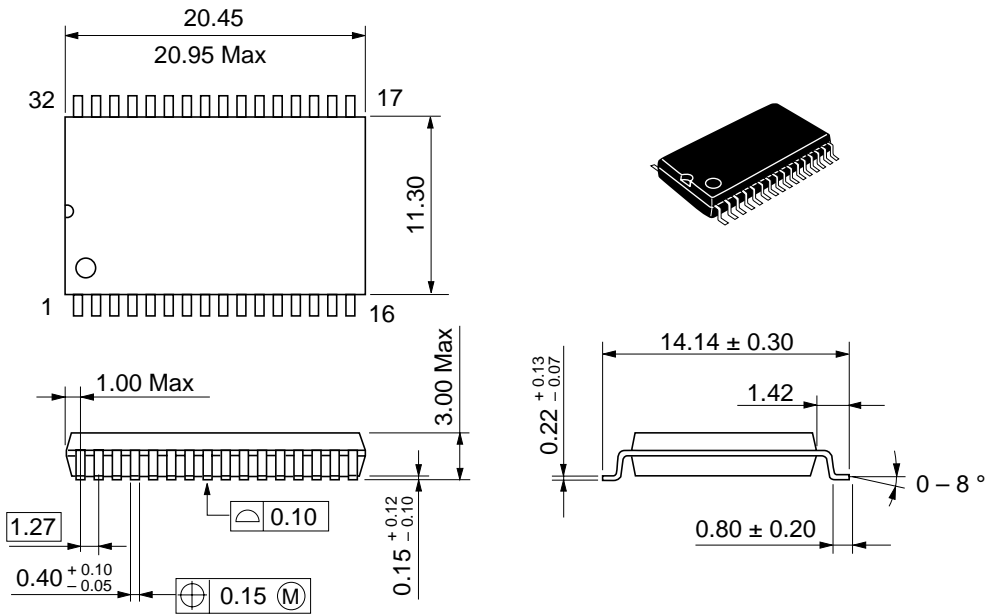
HM628128ALP Series (DP-32)

Unit: mm



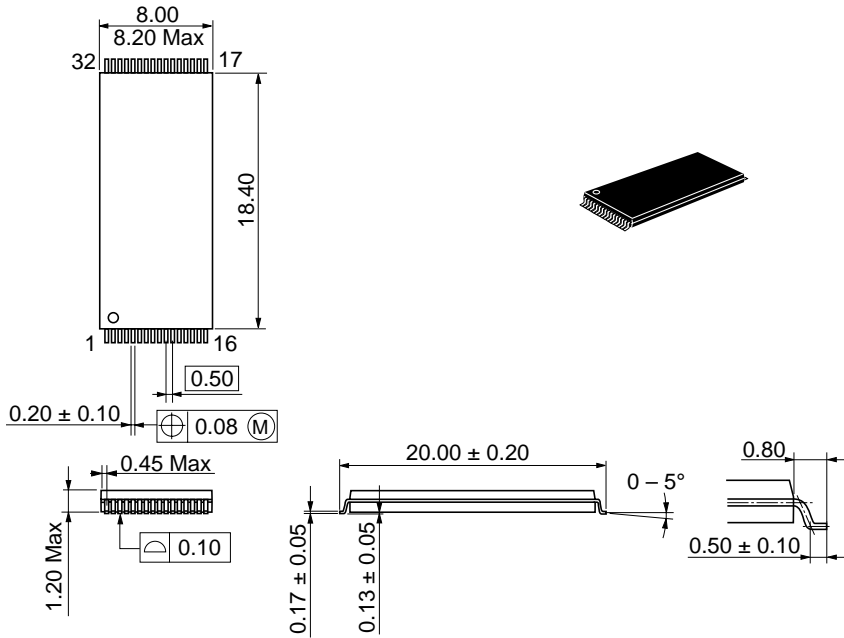
HM628128ALFP Series (FP-32D)

Unit: mm



HM628128ALT Series (TFP-32D)

Unit: mm



HM628128ALR Series (TFP-32DR)

Unit: mm

