

Document Title**32Kx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Design target	February 12, 1993	Advance
0.1	Initial draft	November 2, 1993	Preliminary
1.0	Finalize	September 24, 1994	Final
2.0	Revised	August 12, 1995	Final
3.0	Revised - One datasheet for commercial, extended, industrial product. - Increased KM62V256C Family's Icc2 30 to 35mA. - Increased tDW 50 to 60ns for KM62U256C Family. - Remove SOP package from KM62V256C Family.	April 1, 1997	Final
4.0	Revised - Change datasheets format. - Improved power dissipation : 0.7W→1W	February 12, 1998	Final

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32Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : Poly Load
- Organization : 32Kx8
- Power Supply Voltage
 - KM62V256C family : 2.7~3.3V
 - KM62U256C family : 3.0~3.6V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 28-SOP-450, 28-TSOP1-0813.4F/R

GENERAL DESCRIPTION

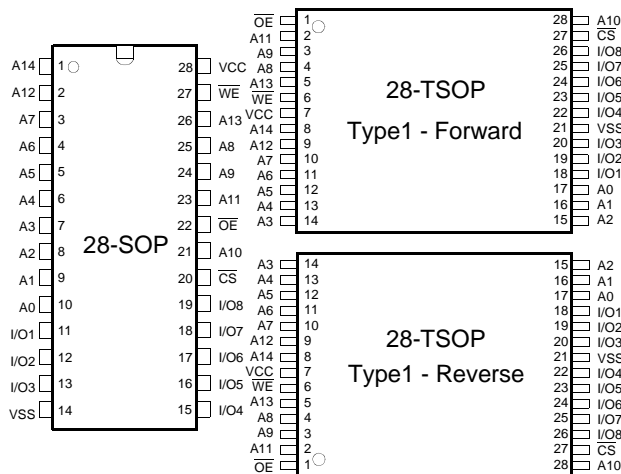
The KM62V256C and KM62U256C families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and has various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I _{sb1} , Max)	Operating (I _{cc2} , Max)	
KM62V256CL-L KM62U256CL-L	Commercial(0~70°C)	3.0 ~ 3.6V 2.7 ~ 3.3V	70 ¹⁾ /100 85 ¹⁾ /100	10μA 10μA	35mA	28-SOP ²⁾ 28-TSOP1-F/R
KM62V256CLE-L KM62U256CLE-L	Extended(-25~85°C)	3.0 ~ 3.6V 2.7 ~ 3.3V	70 ¹⁾ /100 85 ¹⁾ /100	20μA 15μA		
KM62V256CL-L KM62U256CLI-L	Industrial(-40~85°C)	3.0 ~ 3.6V 2.7 ~ 3.3V	70 ¹⁾ /100 85 ¹⁾ /100	20μA 15μA		

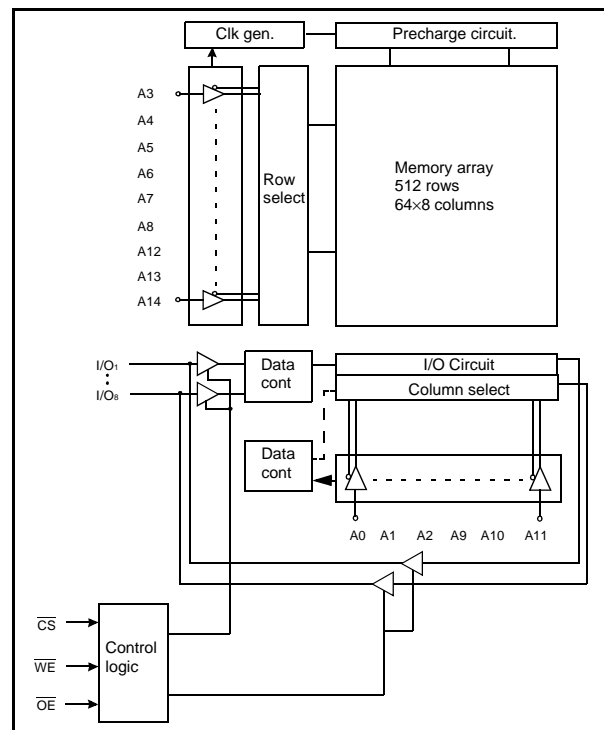
1. The parameter is measured with 30pF test load.
2. The device with 100ns SOP package in 3.0~3.6V Vcc range which is not produced.

PIN DESCRIPTION



Pin Name	Function
\overline{CS}	Chip Select Input
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
A0~A14	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products (0~70°C)		Extended Temperature Products (-25~85°C)		Industrial Temperature Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM62V256CLG-7L	28-SOP, 70ns, 3.3V	KM62V256CLGE-7L	28-SOP, 70ns, 3.3V	KM62V256CLGI-7L	28-SOP, 70ns, 3.3V
KM62V256CLG-10L	28-SOP, 100ns, 3.3V	KM62V256CLGE-10L	28-SOP, 100ns, 3.3V	KM62V256CLGI-10L	28-SOP, 100ns, 3.3V
KM62V256CLTG-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGE-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGI-7L	28-TSOP F, 70ns, 3.3V
KM62V256CLTG-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGE-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGI-10L	28-TSOP F, 100ns, 3.3V
KM62V256CLRG-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGE-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGI-7L	28-TSOP R, 70ns, 3.3V
KM62V256CLRG-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGE-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGI-10L	28-TSOP R, 100ns, 3.3V
KM62U256CLG-8L	28-SOP, 85ns, 3.0V	KM62U256CLGE-8L	28-SOP, 85ns, 3.0V	KM62U256CLGI-8L	28-SOP, 85ns, 3.0V
KM62U256CLG-10L	28-SOP, 100ns, 3.0V	KM62U256CLGE-10L	28-SOP, 100ns, 3.0V	KM62U256CLGI-10L	28-SOP, 100ns, 3.0V
KM62U256CLTG-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGE-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGI-8L	28-TSOP F, 85ns, 3.0V
KM62U256CLTG-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGE-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGI-10L	28-TSOP F, 100ns, 3.0V
KM62U256CLRG-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGE-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGI-8L	28-TSOP R, 85ns, 3.0V
KM62U256CLRG-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGE-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGI-10L	28-TSOP R, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be low or high state.)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM62V256CL-L, KM62U256CL-L
		-25 to 85	°C	KM62V256CLE-L, KM62U256CLE-L
		-40 to 85	°C	KM62V256CLI-L, KM62U256CLI-L
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	KM62V256C Family	3.0	3.3	3.6	V
		KM62U256C Family	2.7	3.0	3.3	
Ground	V _{SS}	All	0	0	0	V
Input high voltage	V _{IH}	KM62V256C, KM62U256C Family	2.2	-	V _{CC} +0.3V ²⁾	V
Input low voltage	V _{IL}	KM62V256C, KM62U256C Family	-0.3 ³⁾	-	0.4	V

Note:

- Commercial Product : T_A=0 to 70°C, otherwise specified
 Extended Product : T_A=-25 to 85°C, unless otherwise specified
 Industrial Product : T_A=-40 to 85°C, otherwise specified
- Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
- Undershoot : -3.0V in case of pulse width ≤ 30ns
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

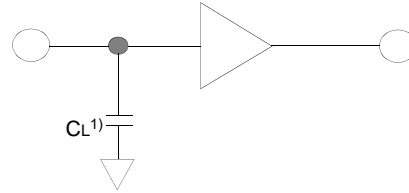
Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	1.0	2.0	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS} \leq 0.2V$, V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	-	2.5	5	mA	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	20	35	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0~V _{CC}	KM62V256CL-L	-	1.5	10	μA
			KM62V256CLE-L	-	1.5	20	
			KM62V256CLI-L	-	1.5	20	
			KM62U256CL-L	-	1.0	10	μA
			KM62U256CLE-L	-	1.0	15	
			KM62U256CLI-L	-	1.0	15	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

- Input pulse level : 0.4 to 2.2V
- Input rising and falling time : 5ns
- Input and output reference voltage : 1.5V
- Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$
- ¹⁾ $C_L=30\text{pF}+1\text{TTL}$

1. KM62V256CL-7L Family, KM62U256CL-8L Family



1. Including scope and jig capacitance

AC CHARACTERISTICS

(KM62V256C Family : $V_{CC}=3.0\text{--}3.6\text{V}$, KM62U256C Family : $V_{CC}=2.7\text{--}3.3\text{V}$)

Commercial product : $T_A=0\text{ to }70^\circ\text{C}$, Extended product : $T_A=-25\text{ to }85^\circ\text{C}$, Industrial product : $T_A=-40\text{ to }85^\circ\text{C}$)

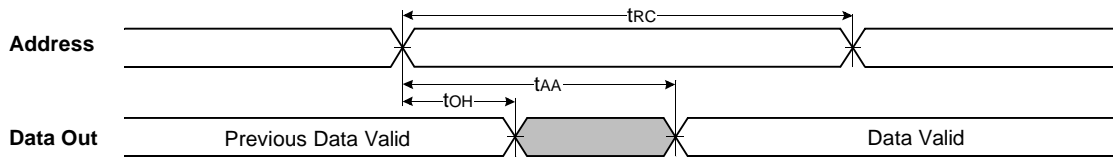
Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	85	-	100	-	ns
	Address access time	t _{AA}	-	70	-	85	-	100	ns
	Chip select to output	t _{CO}	-	70	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	40	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	30	0	30	0	35	ns
	Output disable to high-Z output	t _{OHZ}	0	30	0	30	0	35	ns
	Output hold from address change	t _{OH}	5	-	10	-	15	-	ns
Write	Write cycle time	t _{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	70	-	70	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	70	-	70	-	ns
	Write pulse width	t _{WP}	50	-	60	-	60	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	25	0	30	ns
	Data to write time overlap	t _{DW}	50	-	60	-	60	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	10	-	10	-	ns

DATA RETENTION CHARACTERISTICS

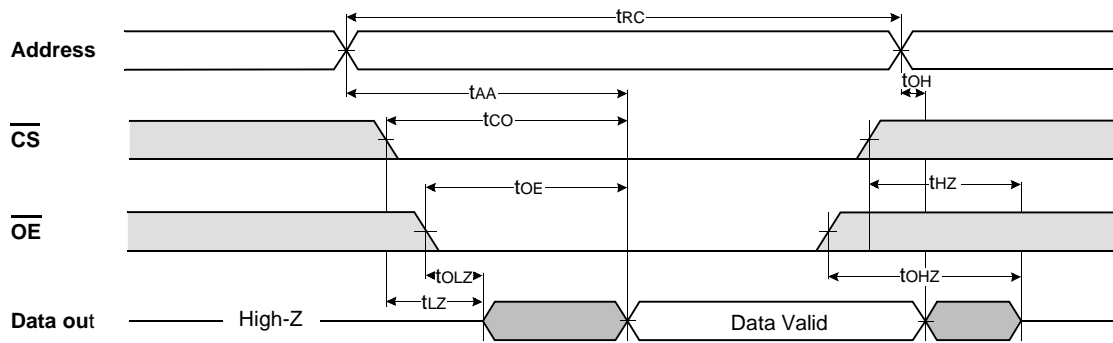
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS} \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	V _{CC} =3.0V $\overline{CS} \geq V_{CC}-0.2\text{V}$	-	1	8	μA
			-	0.6	8	
			-	1	10	
			-	0.6	10	
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



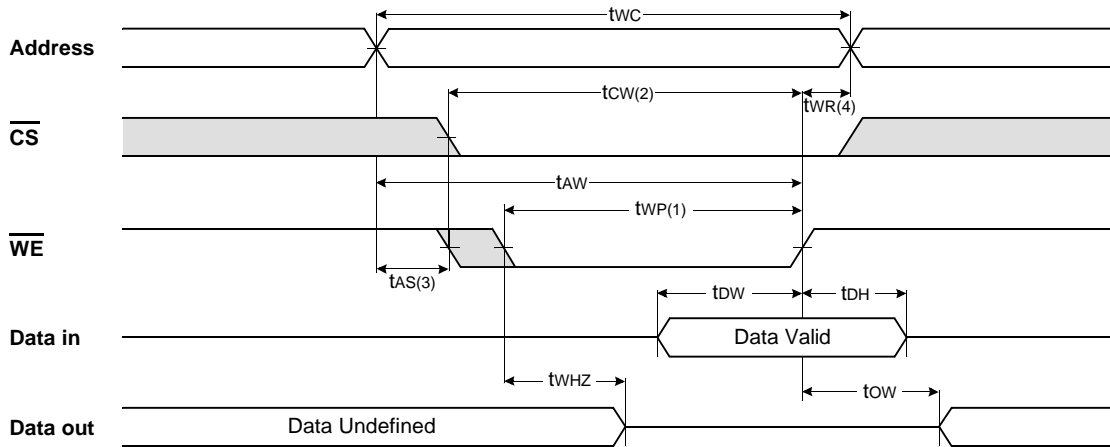
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



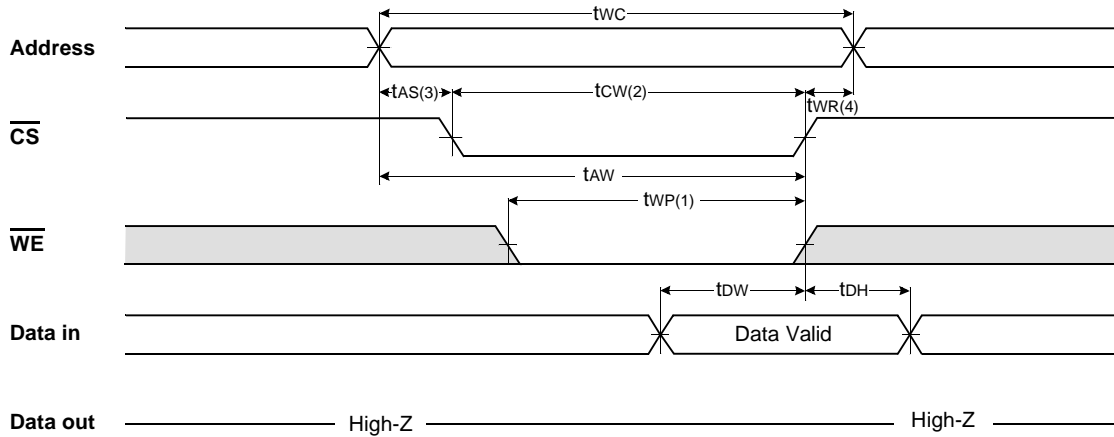
NOTES (READ CYCLE)

1. t_{HZ} and t_{OZH} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)

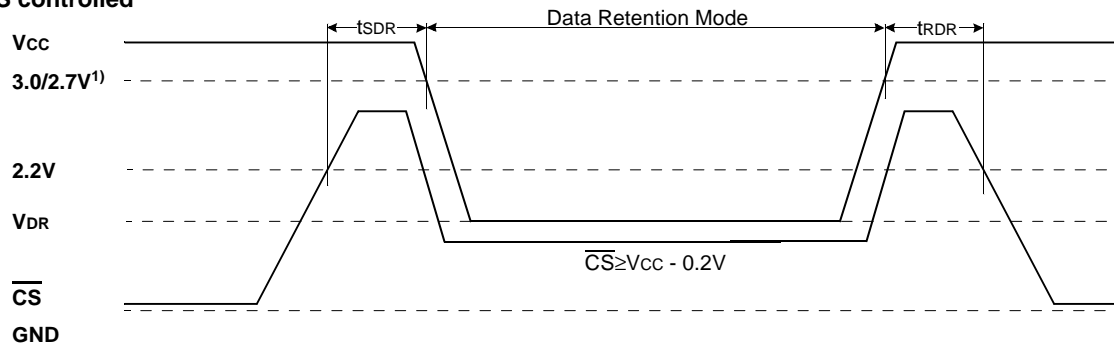


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going Low and \overline{WE} going low : A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM

\overline{CS} controlled

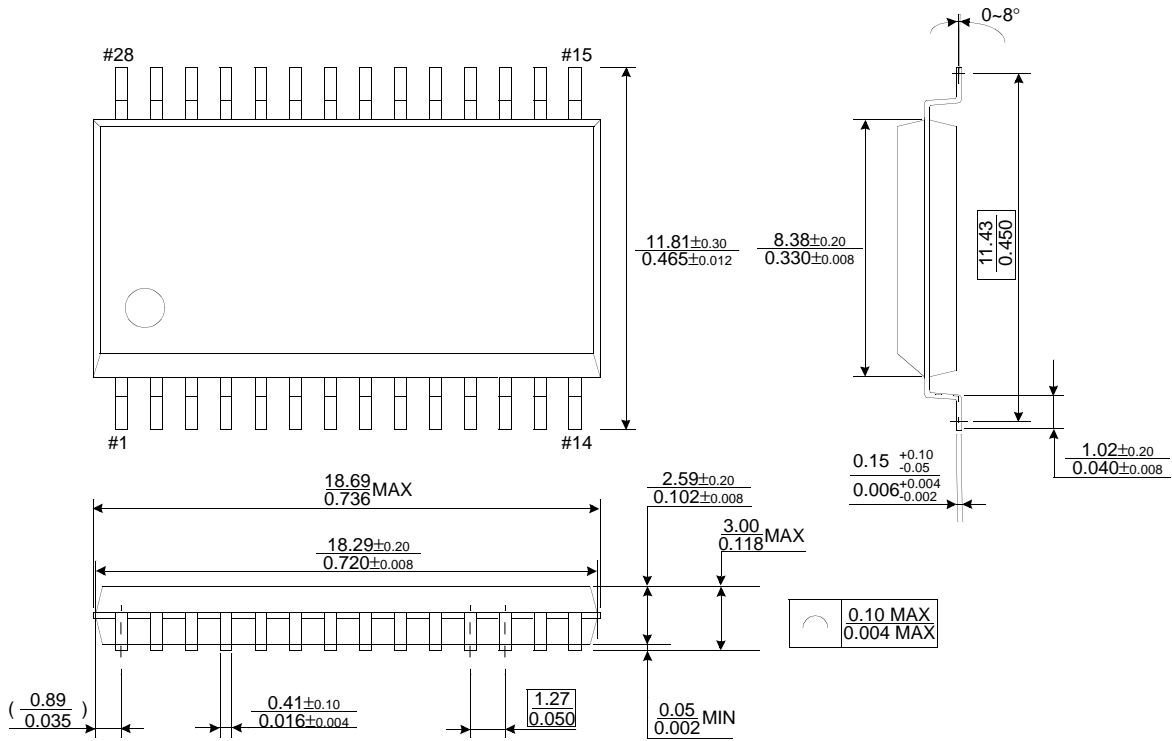


1. 3.0V for KM62V256C Family, 2.7V for KM62U256C Family.

PACKAGE DIMENSIONS

Units : millimeter(inch)

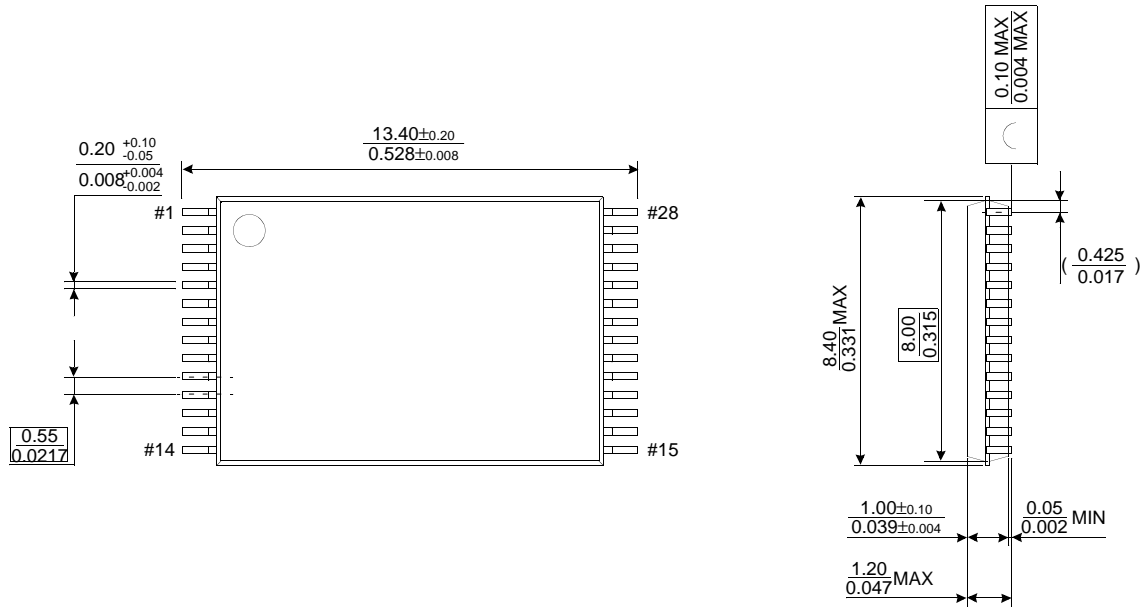
28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



PACKAGE DIMENSIONS

Units : millimeter(inch)

28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)

