Am27C1024

1 Megabit (65,536 x 16-Bit) CMOS EPROM

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 55 ns maximum access time
- **Low power consumption**
  - — 100 µA typical CMOS standby current
- **JEDEC-approved pinouts**
  - — 40-Pin DIP/PDIP
  - — 44-Pin PLCC
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite programming**
  - — Typical programming time of 8 seconds
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

GENERAL DESCRIPTION

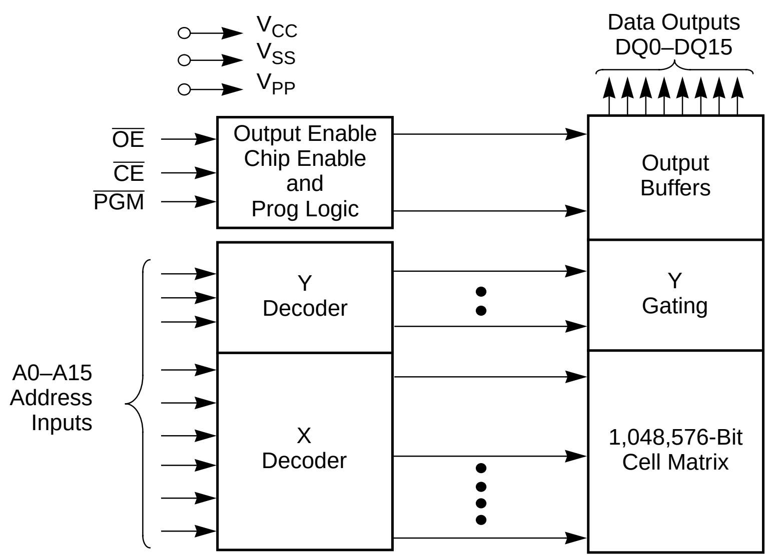
The Am27C1024 is a 1 Mbit ultraviolet erasable programmable read-only memory. It is organized as 64K words by 16 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 70 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C1024 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C1024 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in a typical programming time of 8 seconds.

BLOCK DIAGRAM



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Publication# **06780** Rev: **I** Amendment/**+2**
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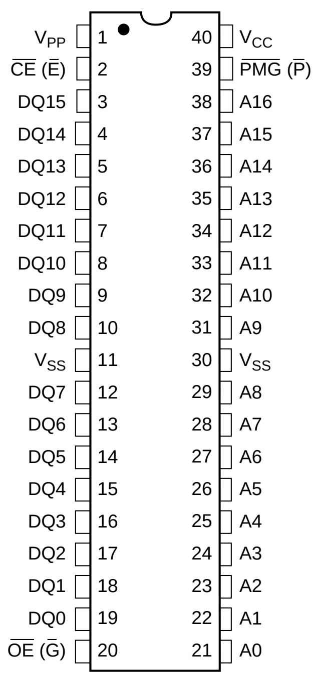
PRODUCT SELECTOR GUIDE

Family Part No:	Am27C1024						
Ordering Part No: V_{CC} = 5.0 V ± 5%	**-55**						**-255**
V_{CC} = 5.0 V ± 10%	**-55**	**-70**	**-90**	**-120**	**-150**	**-200**	
Max Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	40	40	50	65	75	75

CONNECTION DIAGRAMS

Top View

DIP



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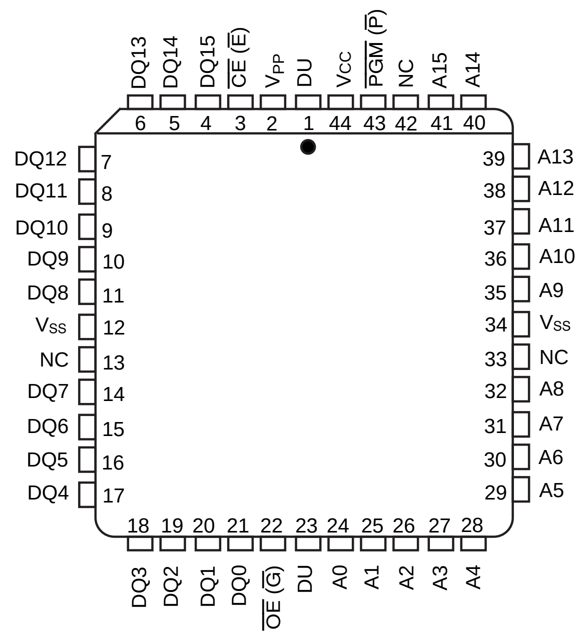
PLCC



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Note:

1. JEDEC nomenclature is in parenthesis.

PIN DESIGNATIONS

A0–A15 = Address Inputs

$\overline{CE}$ ($\overline{E}$) = Chip Enable

DQ0–DQ15 = Data Inputs/Outputs

$\overline{OE}$ ($\overline{G}$) = Output Enable Input

$\overline{PGM}$ ($\overline{P}$) = Program Enable Input

V_{CC} = V_{CC} Supply Voltage

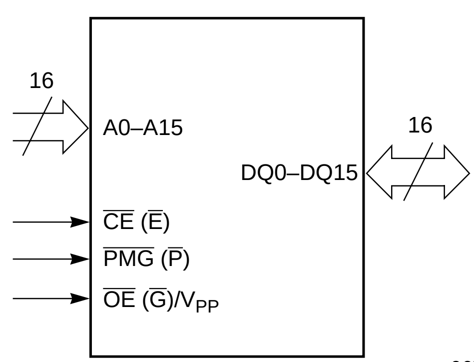
V_{PP} = Program Voltage Input

V_{SS} = Ground

NC = No Internal Connection

DU = No External Connection (Do Not Use)

LOGIC SYMBOL



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ORDERING INFORMATION

UV EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM27C1024 -55 D C 5 B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

VOLTAGE TOLERANCE
5 = V_{CC} ± 5%, 55 ns only
See Product Selector Guide and Valid Combinations

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
D = 40-Pin Ceramic DIP (CDV040)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27C1024
1 Megabit (65,536 x 16-Bit) CMOS UV EPROM

Valid Combinations	
AM27C1024-55 V_{CC} = 5.0 V ± 5%	DC5, DC5B, DI5, DI5B
AM27C1024-55 V_{CC} = 5.0 V ± 10%	DC, DCB, DI, DIB
AM27C1024-70	
AM27C1024-90	
AM27C1024-120	DC, DCB, DE, DEB, DI, DIB
AM27C1024-150	
AM27C1024-200	
AM27C1024-255 V_{CC} = 5.0 V ± 5%	DC, DCB, DI, DIB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM27C1024 -55 J C 5

OPTIONAL PROCESSING
Blank = Standard Processing

VOLTAGE TOLERANCE
5 = V_{CC} ± 5%, -55 ns only
See Product Selector Guide and Valid Combinations

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)

PACKAGE TYPE
P = 40-Pin Plastic DIP (PD 040)
J = 44-Pin Square Plastic Leaded Chip Carrier (PL 044)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27C1024
2 Megabit (131,072 x 16-Bit) CMOS OTP EPROM

Valid Combinations	
AM27C1024-55 V_{CC} = 5.0 V ± 5%	PC5, PI5, JC5, JI5
AM27C1024-55 V_{CC} = 5.0 V ± 10%	PC, PI, JC, JI
AM27C1024-70	
AM27C1024-90	
AM27C1024-120	
AM27C1024-150	
AM27C1024-200	
AM27C1024-255 V_{CC} = 5.0 V ± 5%	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Erasing the Am27C1024

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C1024 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C1024. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 (Å)—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C1024 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C1024 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C1024 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C1024

Upon delivery or after each erasure the Am27C1024 has all 1,048,576 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C1024 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C1024. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP}$ = 5.25 V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C1024 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C1024 may be common. A TTL low-level program pulse applied to an Am27C1024 $\overline{CE}$ input with V_{PP} = 12.75 V ± 0.25 V, and $\overline{PGM}$ Low will program that Am27C1024. A high-level $\overline{CE}$ input inhibits the other Am27C1024 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} between 12.75 V ± 0.25 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C1024.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V open address the A9 of the Am27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device code. For the Am27C1024, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The Am27C1024 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C1024 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	Hi-Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Autoselect (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H	X	8CH

Notes:

1. *$V_H = 12.0\ V \pm 0.5\ V$*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A15 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products. . . . . –65°C to +125°C
All Other Products . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Voltage with Respect to V_{SS}
All pins except A9, V_{PP}, V_{CC} . . . . –0.6 V to V_{CC} + 0.6 V

A9 and V_{PP} (Note 2). . . . . –0.6 V to +13.5 V

V_{CC} (Note 1). –0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, the inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20ns.*
2. *Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. A9 and V_{CC} must not exceed +13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A). . . . . .0°C to +70°C

Industrial (I) Devices
Ambient Temperature (T_A). . . . .–40°C to +85°C

Extended (E) Devices
Ambient Temperature (T_A). . . . .–55°C to +125°C

Supply Read Voltages

V_{CC} for Am27C1024-55, 255 . . . . +4.75 V to +5.25 V

V_{CC} for Am27C1024 (All Others) . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, and 4)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}			5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 10 MHz I_{OUT} = 0 mA	C/I Devices		50	mA
			E Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During (Read)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution**: The Am27C1024 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

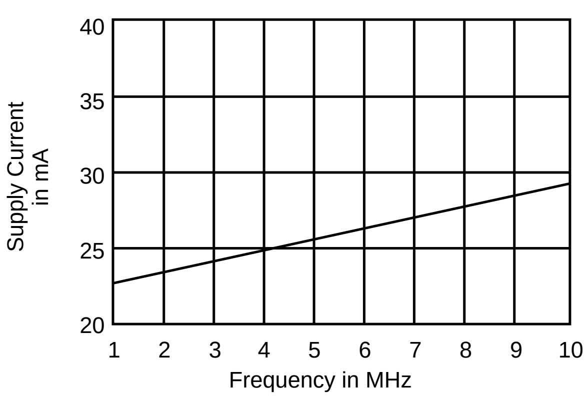

Figure 1. Typical Supply Current vs. Frequency V_{CC} = 5.5 V, T = 25°C

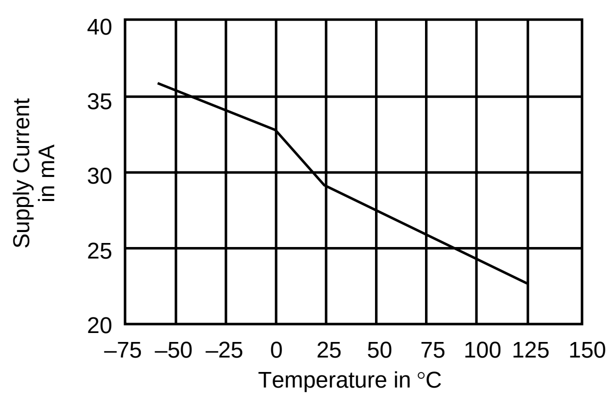

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Figure 2. Typical Supply Current vs. Frequency V_{CC} = 5.5 V, T = 25°C

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV040		PD 040		PL 044		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	$V_{IN} = 0$	9	12	7	12	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	12	14	11	14	11	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *$T_A = +25°C$, f = 1 MHz.*

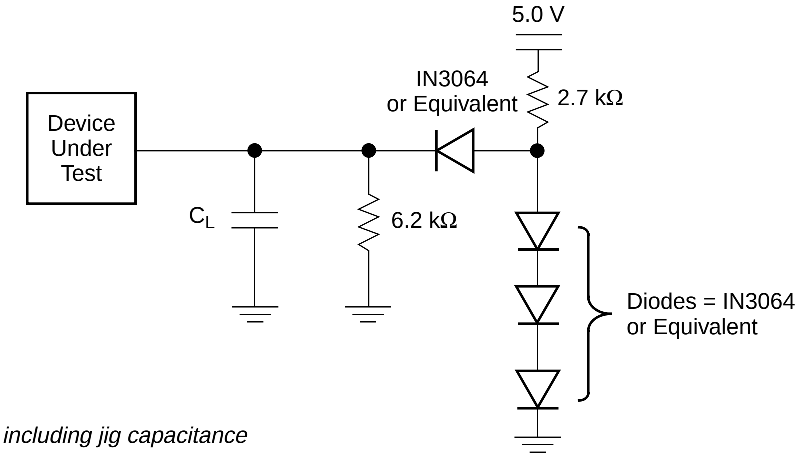
AC CHARACTERISTICS

Parameter Symbols		Description	Test Setup		Am27C1024							Unit
JEDEC	Standard				-55	-70	-90	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$, $\overline{OE} = V_{IL}$	Max	55	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max	55	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Max	40	40	45	50	65	75	75	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 3)	Chip Enable to Output High Z or Output Enable to Output High Z to Output Float, whichever occurs first		Max	30	30	40	50	50	50	50	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurs first		Min	0	0	0	0	0	0	0	ns

Notes:

1. ***Caution:*** *Do not remove the Am27C1024 from (or insert it into) a socket or board that has V_{PP} or V_{CC} applied.*
2. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
3. *This parameter is sampled and not 100% tested.*
4. *Switching characteristics are over operating range, unless otherwise specified.*
5. *Test Conditions for Am27C1024-55:*
   Output Load: 1 TTL gate and $C_L = 30$ pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level Inputs and Outputs: 1.5 V
   Test Conditions for all others:
   Output Load: 1 TTL gate and $C_L = 100$ pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level Inputs and Outputs: 0.8 and 2.0 V

SWITCHING TEST CIRCUIT



Notes:
For -55: C_L = 30 pF including jig capacitance
For all others: C_L = 100 pF including jig capacitance

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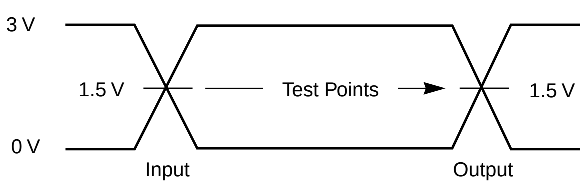
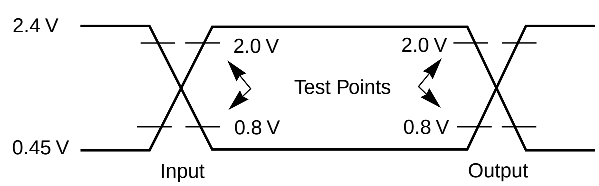
Test Conditions

SWITCHING TEST WAVEFORM





AC Testing for -55 devices: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤20 ns.

AC Testing (except for -55 devices): Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤20 ns.

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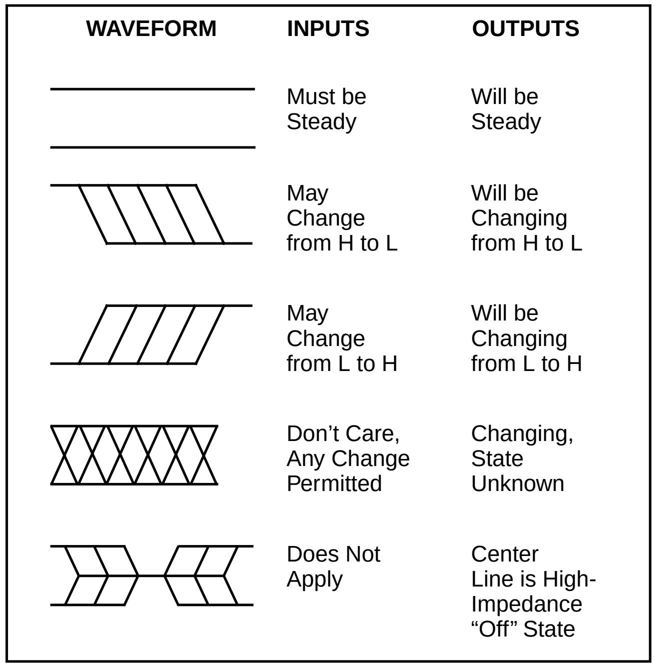
KEY TO SWITCHING WAVEFORMS



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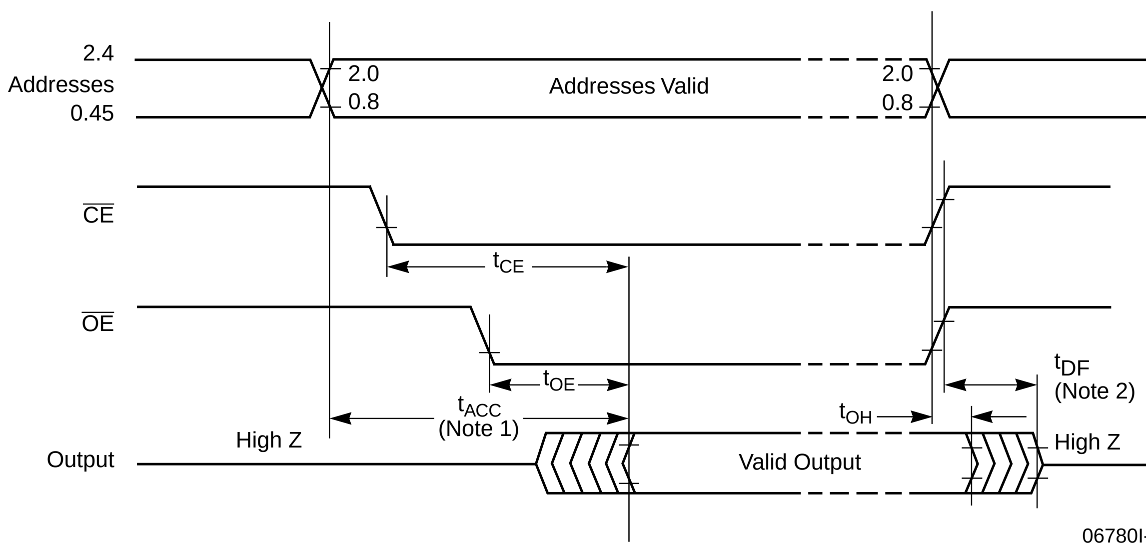
SWITCHING WAVEFORMS



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Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} – t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *DF is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

REVISION SUMMARY FOR AM27C1024

Distinctive Characteristics:

The fastest speed grade available is now 55 ns.

Product Selector Guide:

Added 55 ns column.

Ordering Information, UV EPROM Products:

The 55 ns part number is now listed in the example. The nomenclature now has a method of clearly designating the voltage operating range and speed grade.

Ordering Information, OTP EPROM Products:

Changed the part number example from -70 to -55. The nomenclature now has a method of clearly designating the voltage operating range and speed grade.

Operating Ranges:

Changed Supply Read Voltages listings to match those in the Product Selector Guide.

AC Characteristics:

Added column for 55 ns speed grade, rearranged notes, moved text from table title to Note 4, renamed table.

Switching Test Circuit:

Added 55 ns to the C_L note on 30 pF test condition.

Switching Test Waveform:

Added the 3 V test waveform.