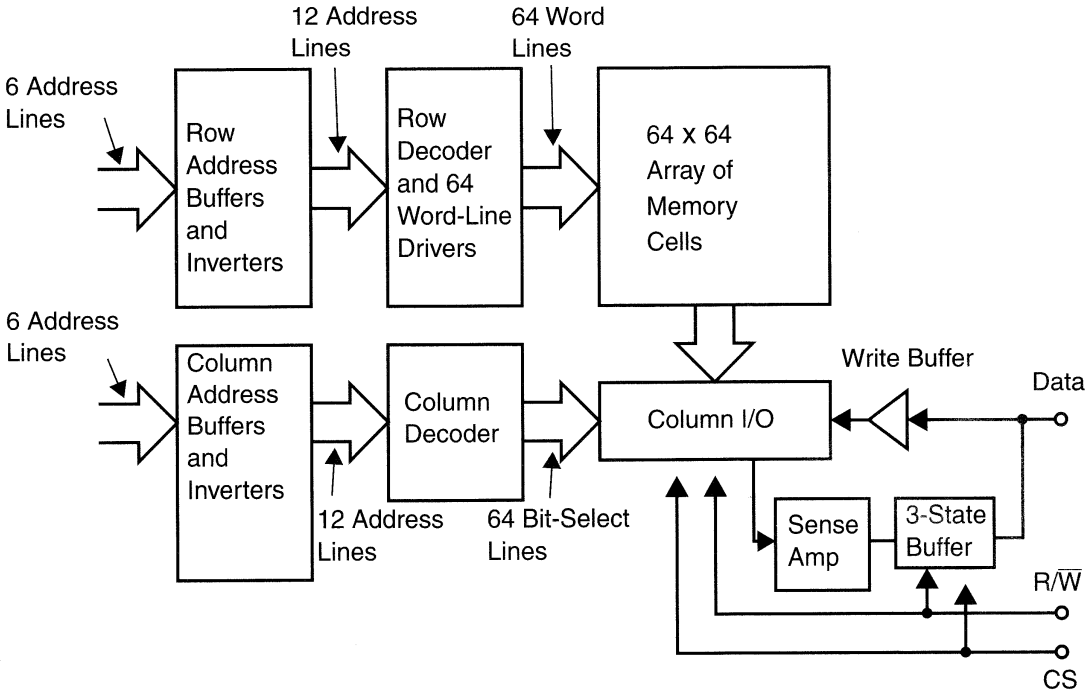

Figure 11.1 A simplified block diagram of a 4096 by 1 RAM.

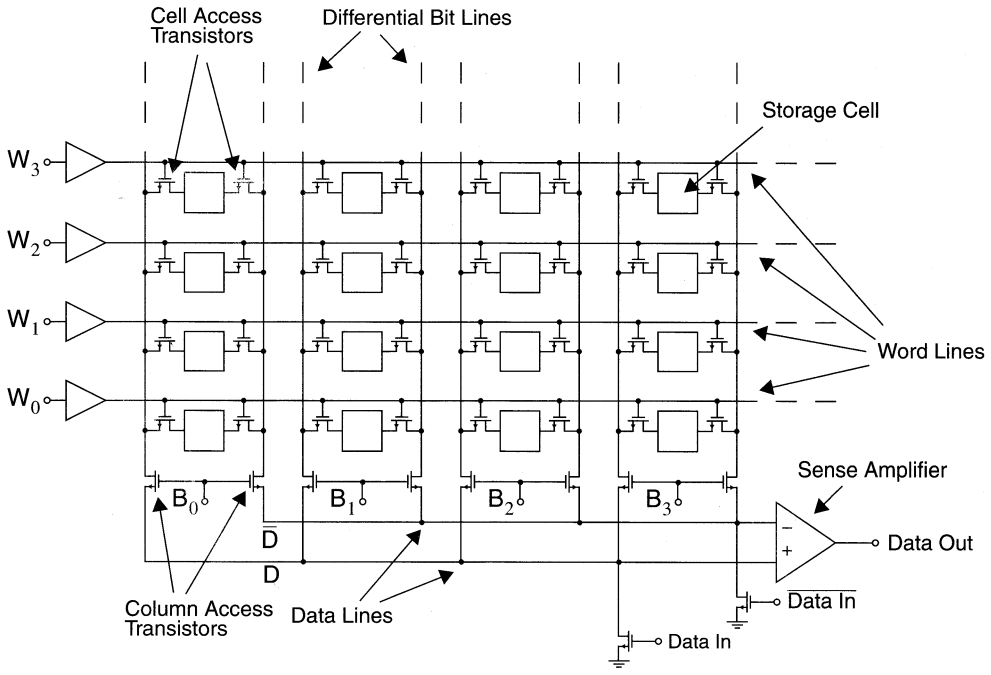

Figure 11.2 A simplified portion of an SRAM array.

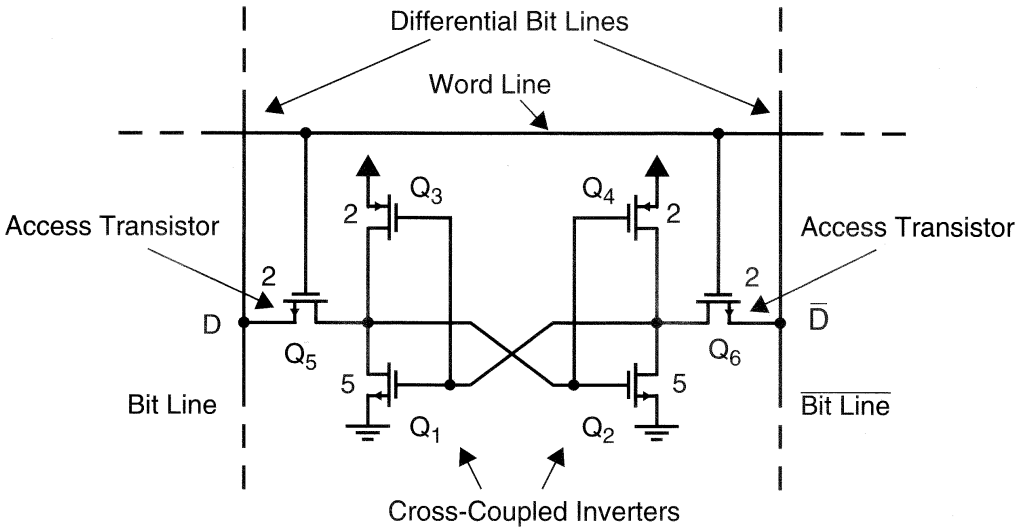

Figure 11.3 A CMOS static RAM storage cell.

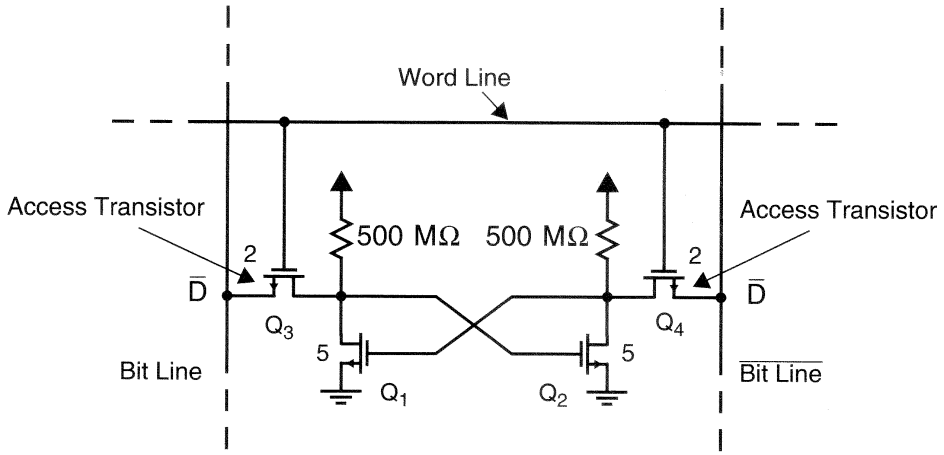

Figure 11.4 A CMOS static RAM storage cell using high-resistivity polysilicon loads.

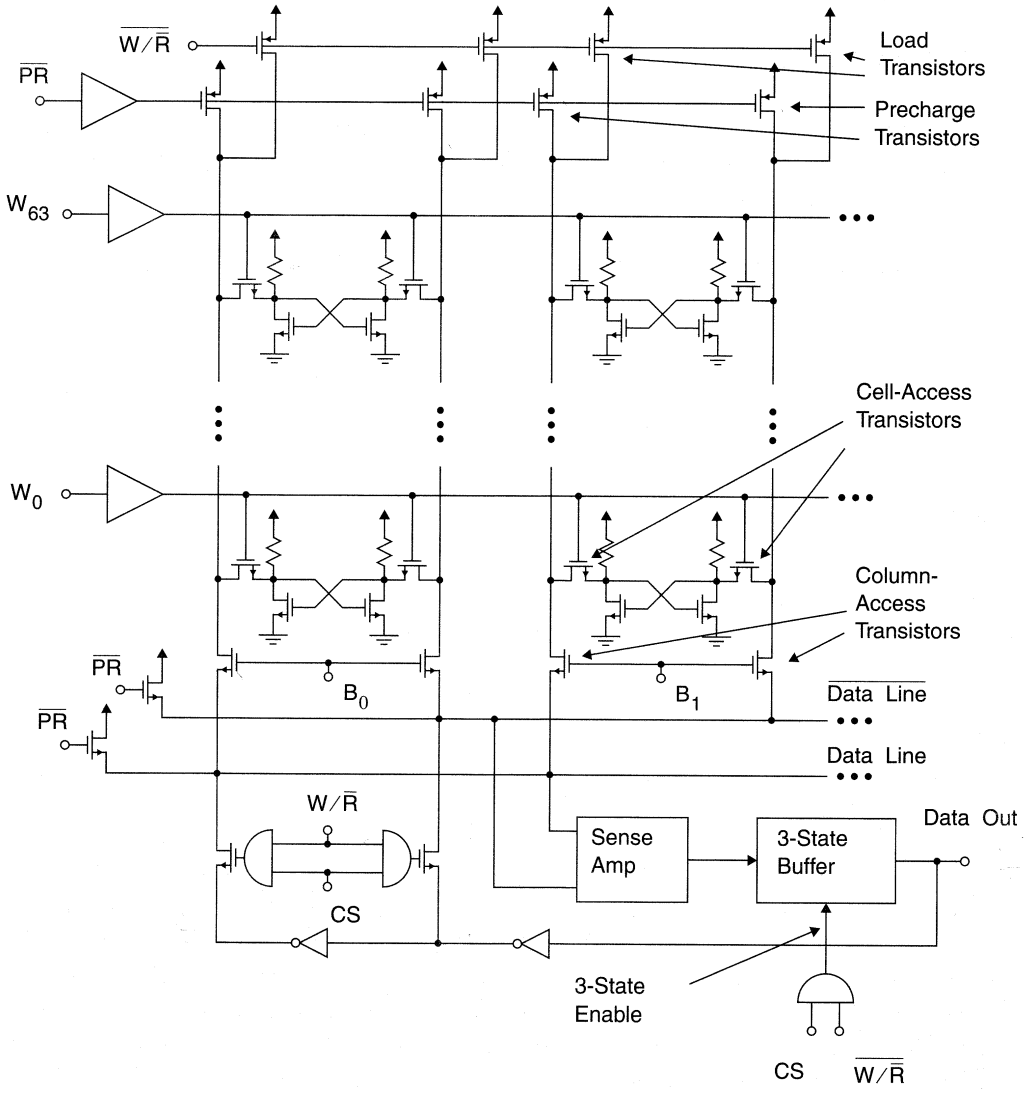

Figure 11.5 An SRAM array with some of the peripheral circuitry shown.

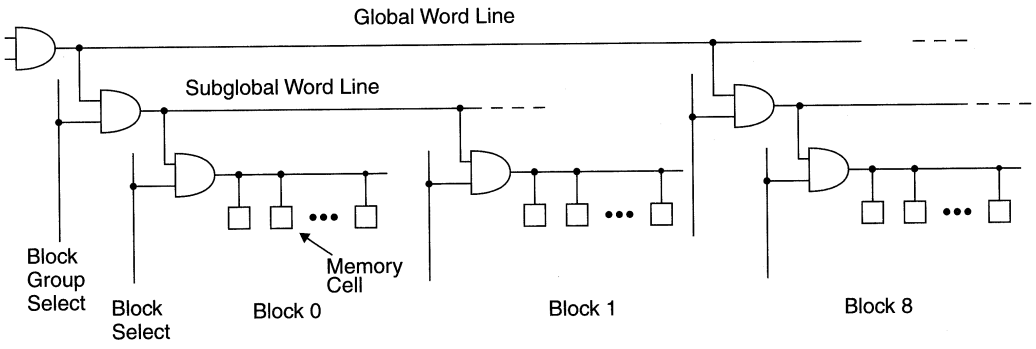

Figure 11.19 The hierarchical word decoding of Hirose et al. (1990).