

## Features

- Compatible with MCS-51™ Products
- 4 Kbytes of In-System Reprogrammable Flash Memory  
Endurance: 1,000 Write/Erase Cycles
- 2.7 V to 6 V Operating Range
- Fully Static Operation: 0 Hz to 12 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

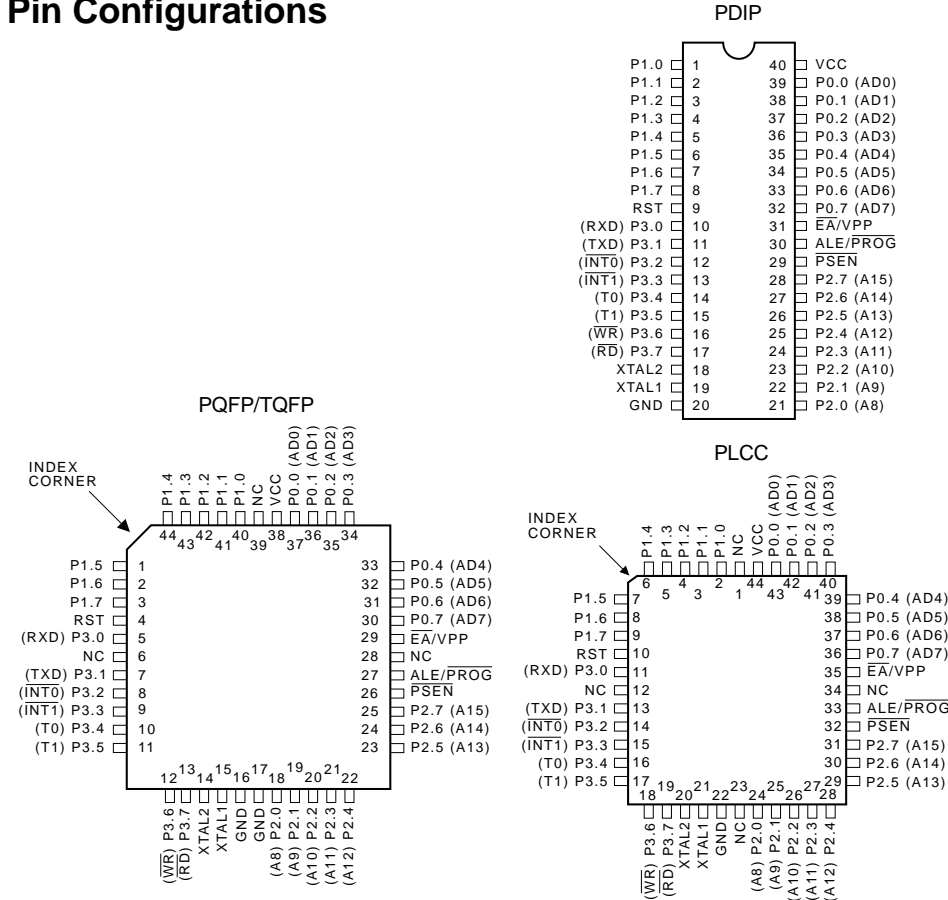
## Description

The AT89LV51 is a low-voltage, high-performance CMOS 8-bit microcomputer with 4 Kbytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89LV51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

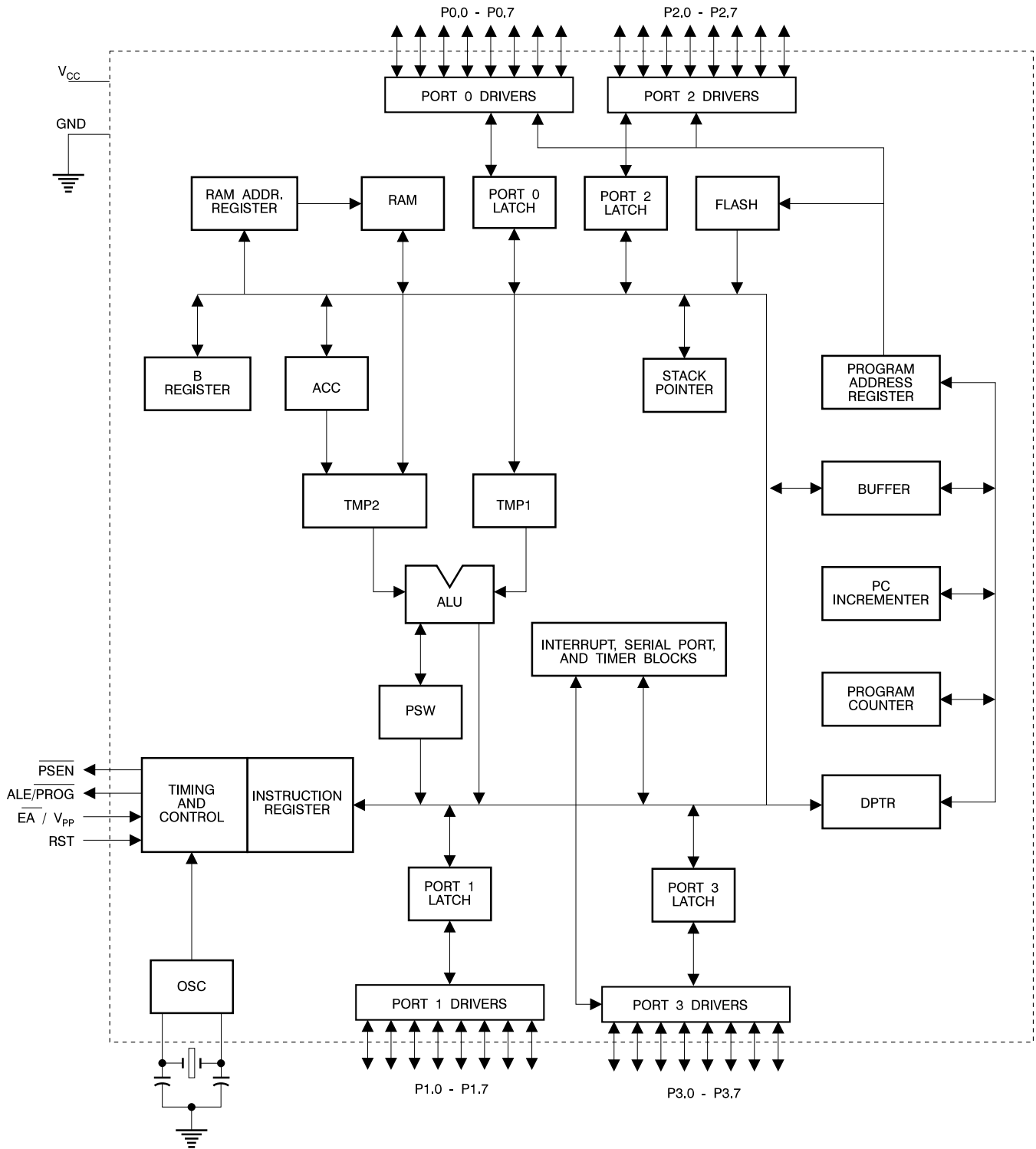
The AT89LV51 provides the following standard features: 4 Kbytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89LV51 is

*(continued)*

## Pin Configurations



# Block Diagram



## Description (Continued)

designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

## Pin Description

V<sub>CC</sub>

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I<sub>IL</sub>) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and program verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I<sub>IL</sub>) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s

are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I<sub>IL</sub>) because of the pullups.

Port 3 also serves the functions of various special features of the AT89LV51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ( $\overline{\text{PROG}}$ ) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{\text{PSEN}}$

Program Store Enable is the read strobe to external program memory.

When the AT89LV51 is executing code from external program memory,  $\overline{\text{PSEN}}$  is activated twice each machine cycle, except that two  $\overline{\text{PSEN}}$  activations are skipped during each access to external data memory.

$\overline{\text{EA}}/\text{VPP}$

External Access Enable.  $\overline{\text{EA}}$  must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed,  $\overline{\text{EA}}$  will be internally latched on reset.

$\overline{\text{EA}}$  should be strapped to V<sub>CC</sub> for internal program executions.

This pin also receives the 12-volt programming enable voltage (V<sub>PP</sub>) during Flash programming, when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

## Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

## Idle Mode

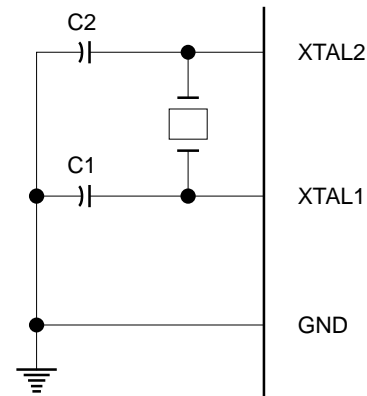
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

## Power Down Mode

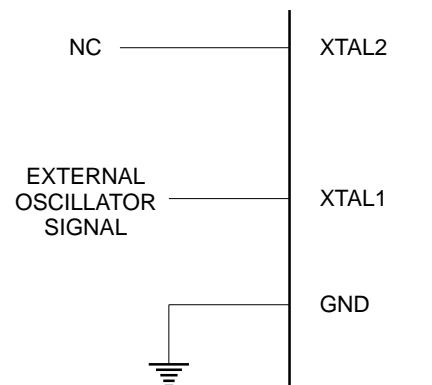
In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before  $V_{CC}$  is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 1. Oscillator Connections



Notes: C1, C2 = 30 pF ± 10 pF for Crystals  
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



## Status of External Pins During Idle and Power Down

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

## Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the  $\overline{EA}$  pin is sampled and latched during reset. If the device is powered up

without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of  $\overline{EA}$  be in agreement with the current logic level at that pin in order for the device to function properly.

## Lock Bit Protection Modes<sup>(1)</sup>

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Note: 1. The lock bits can only be erased with the chip erase operation.

## Programming the Flash

The AT89LV51 is normally shipped with the on-chip Flash memory array in the erased state (i.e. contents=FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (5-volt) program enable signal. The low voltage programming mode provides a convenient way to program the AT89LV51 inside the user's system while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89LV51 is shipped with either the High-Voltage or Low-Voltage programming mode enabled. The respective top-side marking and device signature codes are listed below:

	VPP = 12 V	VPP = 5 V
Top-Side Mark	AT89LV51 xxxx yyww	AT89LV51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=61H (032H)=FFH	(030H)=1EH (031H)=61H (032H)=05H

The AT89LV51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip PEROM Code Memory, the entire memory must be erased using the Chip Erase Mode.*

**Programming Algorithm:** Before programming the AT89LV51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89LV51, the following sequence should be followed:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise  $\overline{EA}/V_{PP}$  to 12-V if in the high-voltage programming mode.
5. Pulse  $\overline{ALE}/\overline{PROG}$  once to program a byte in the Flash

array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

**Data Polling:** The AT89LV51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on PO.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

**Ready/Busy:** The progress of byte programming can also be monitored by the  $\overline{RDY}/\overline{BSY}$  output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

**Program Verify:** If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase:** The entire Flash array and the lock bits are erased electrically by using the proper combination of control signals and by holding  $\overline{ALE}/\overline{PROG}$  low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

**Reading the Signature Bytes:** The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values returned are:

- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 61H indicates 89LV51
- (032H) = FFH (High-Voltage) or 05H (Low-Voltage) programming mode



## Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

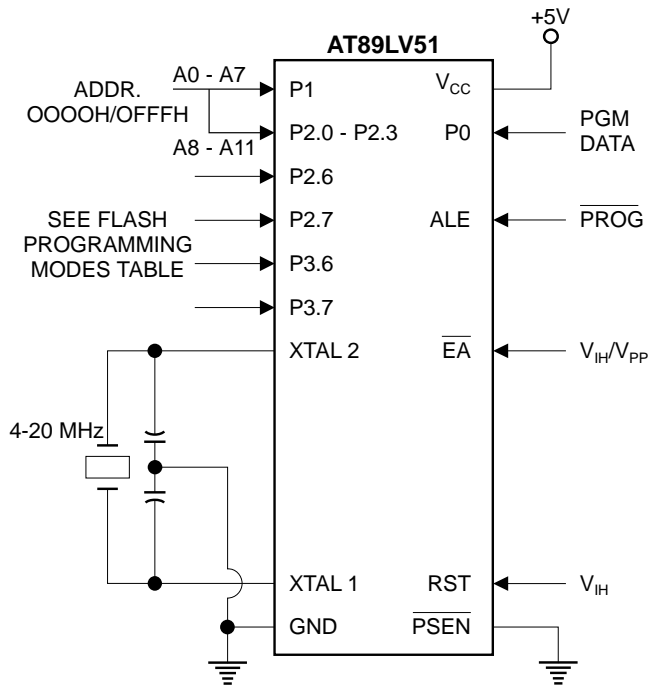
All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

## Flash Programming Modes

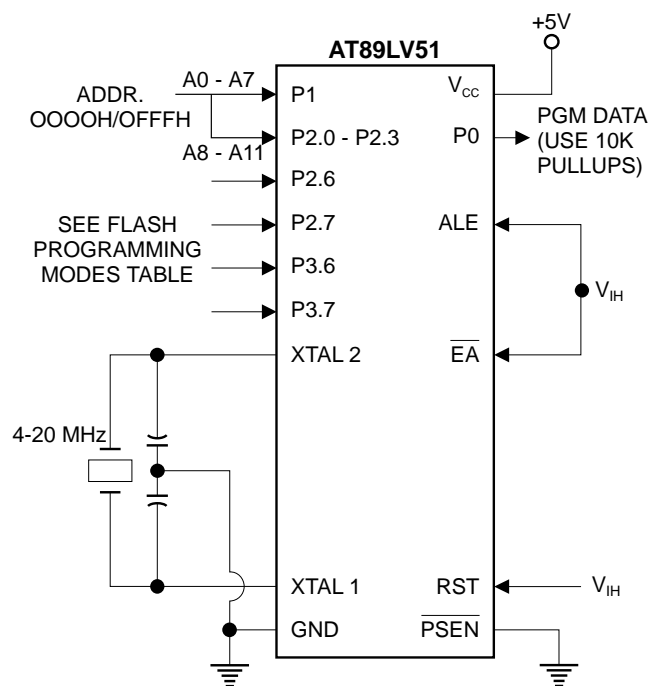
Mode	RST	$\overline{\text{PSEN}}$	ALE/ PROG	EA/ V <sub>PP</sub>	P2.6	P2.7	P3.6	P3.7								
Write Code Data	H	L		H/12V <sup>(1)</sup>	L	H	H	H								
Read Code Data	H	L	H	H	L	L	H	H								
Write Lock	Bit - 1	L		H/12V	H	H	H	H								
									Bit - 2	L		H/12V <sup>(2)</sup>	H	H	L	L
									Bit - 3							
Chip Erase	H	L		H/12V	H	L	L	L								
Read Signature Byte	H	L	H	H	L	L	L	L								

Notes: 1. The signature byte at location 032H designates whether V<sub>pp</sub> = 12 V or V<sub>pp</sub> = 5 V should be used to enable programming. 2. Chip Erase requires a 10 ms  $\overline{\text{PROG}}$  pulse.

**Figure 3. Programming the Flash**



**Figure 4. Verifying the Flash**



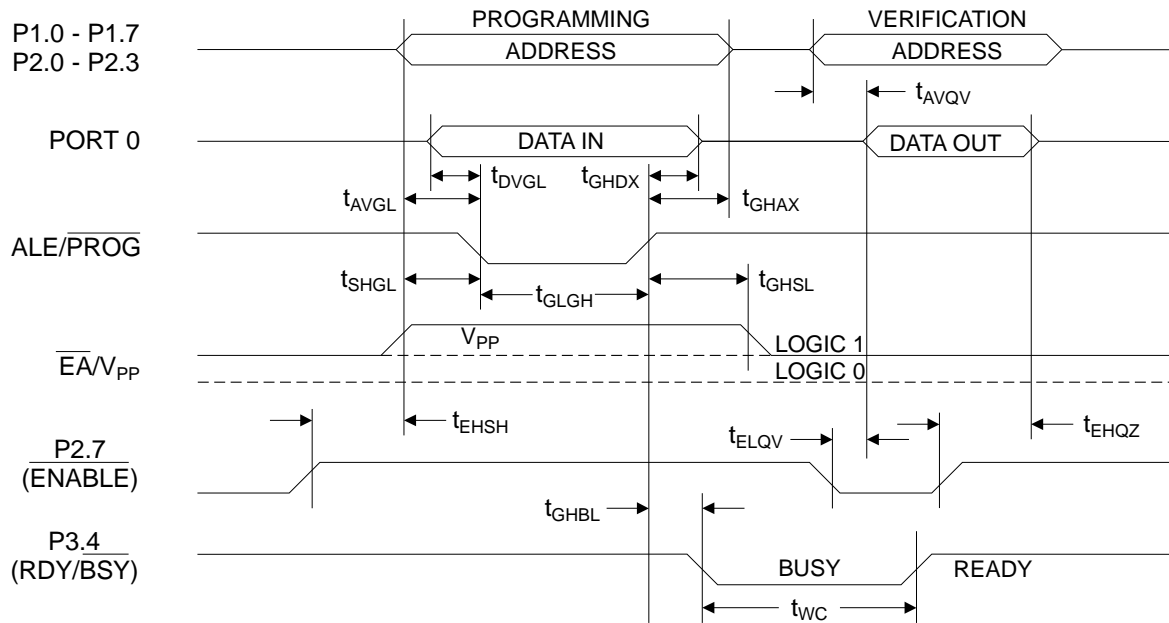
## Flash Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$  to  $27^\circ\text{C}$ ,  $V_{CC} = 5.0 \pm 10\%$

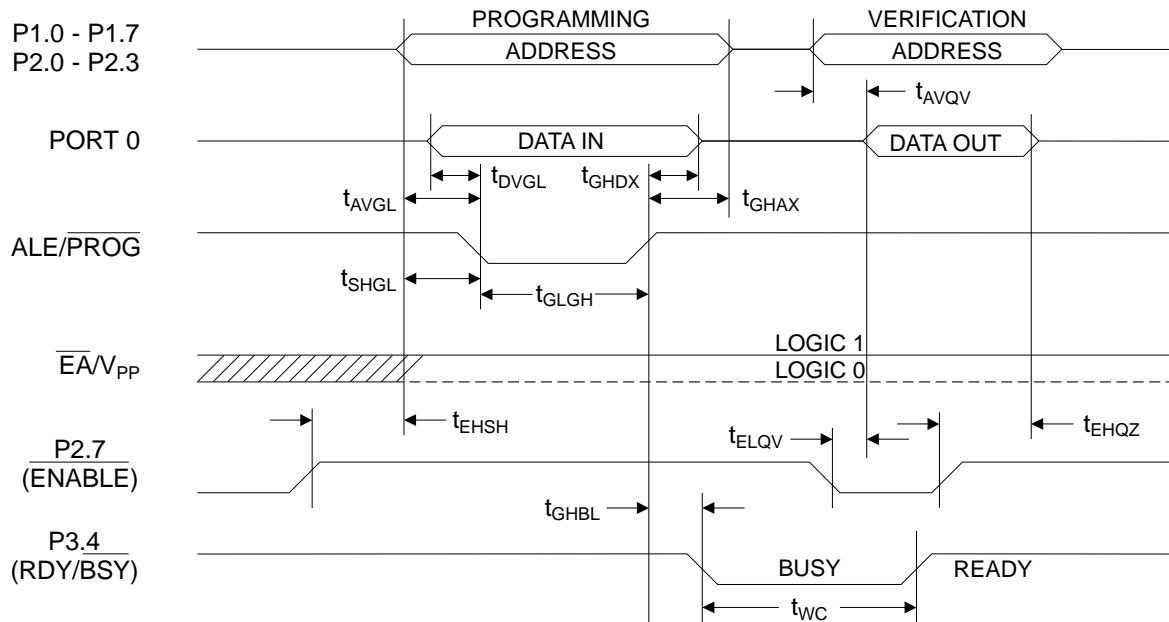
Symbol	Parameter	Min	Max	Units
$V_{PP}^{(1)}$	Programming Enable Voltage	11.5	12.5	V
$I_{PP}^{(1)}$	Programming Enable Current		25	$\mu\text{A}$
$1/t_{CLCL}$	Oscillator Frequency	4	12	MHz
$t_{AVGL}$	Address Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
$t_{GHAX}$	Address Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
$t_{DVGL}$	Data Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
$t_{GHDX}$	Data Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
$t_{EHS}$	P2.7 ( $\overline{\text{ENABLE}}$ ) High to $V_{PP}$	$48t_{CLCL}$		
$t_{SHGL}$	$V_{PP}$ Setup to $\overline{\text{PROG}}$ Low	10		$\mu\text{s}$
$t_{GHSL}^{(1)}$	$V_{PP}$ Hold After $\overline{\text{PROG}}$	10		$\mu\text{s}$
$t_{GLGH}$	$\overline{\text{PROG}}$ Width	1	110	$\mu\text{s}$
$t_{AVQV}$	Address to Data Valid		$48t_{CLCL}$	
$t_{ELQV}$	$\overline{\text{ENABLE}}$ Low to Data Valid		$48t_{CLCL}$	
$t_{EHQV}$	Data Float After $\overline{\text{ENABLE}}$	0	$48t_{CLCL}$	
$t_{GHBL}$	$\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low		1.0	$\mu\text{s}$
$t_{WC}$	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

## Flash Programming and Verification Waveforms - High Voltage Mode



## Flash Programming and Verification Waveforms - Low Voltage Mode





## Absolute Maximum Ratings\*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-1.0 V to +7.0 V
Maximum Operating Voltage .....	6.6 V
DC Output Current.....	15.0 mA

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. Characteristics

T<sub>A</sub> = -40°C to 85°C, V<sub>CC</sub> = 2.7 V to 6.0 V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V <sub>IL</sub>	Input Low Voltage	(Except $\overline{EA}$ )	-0.5	0.2 V <sub>CC</sub> -0.1	V
V <sub>IL1</sub>	Input Low Voltage ( $\overline{EA}$ )		-0.5	0.2 V <sub>CC</sub> -0.3	V
V <sub>IH</sub>	Input High Voltage	(Except XTAL1, RST)	0.2 V <sub>CC</sub> +0.9	V <sub>CC</sub> +0.5	V
V <sub>IH1</sub>	Input High Voltage	(XTAL1, RST)	0.7 V <sub>CC</sub>	V <sub>CC</sub> +0.5	V
V <sub>OL</sub>	Output Low Voltage <sup>(1)</sup> (Ports 1,2,3)	I <sub>OL</sub> = 1.6 mA		0.45	V
V <sub>OL1</sub>	Output Low Voltage <sup>(1)</sup> (Port 0, ALE, PSEN)	I <sub>OL</sub> = 3.2 mA		0.45	V
V <sub>OH</sub>	Output High Voltage (Ports 1,2,3, ALE, PSEN)	I <sub>OH</sub> = -60 μA, V <sub>CC</sub> = 5 V ± 10%	2.4		V
		I <sub>OH</sub> = -20 μA	0.75 V <sub>CC</sub>		V
		I <sub>OH</sub> = -10 μA	0.9 V <sub>CC</sub>		V
V <sub>OH1</sub>	Output High Voltage (Port 0 in External Bus Mode)	I <sub>OH</sub> = -800 μA, V <sub>CC</sub> = 5 V ± 10%	2.4		V
		I <sub>OH</sub> = -300 μA	0.75 V <sub>CC</sub>		V
		I <sub>OH</sub> = -80 μA	0.9 V <sub>CC</sub>		V
I <sub>IL</sub>	Logical 0 Input Current (Ports 1,2,3)	V <sub>IN</sub> = 0.45 V		-50	μA
I <sub>TL</sub>	Logical 1 to 0 Transition Current (Ports 1,2,3)	V <sub>IN</sub> = 2 V		-650	μA
I <sub>LI</sub>	Input Leakage Current (Port 0, EA)	0.45 < V <sub>IN</sub> < V <sub>CC</sub>		±10	μA
RRST	Reset Pulldown Resistor		50	300	KΩ
C <sub>IO</sub>	Pin Capacitance	Test Freq. = 1 MHz, T <sub>A</sub> = 25°C		10	pF
I <sub>CC</sub>	Power Supply Current	Active Mode, 12 MHz, V <sub>CC</sub> = 6 V/3 V		20/5.5	mA
		Idle Mode, 12 MHz, V <sub>CC</sub> = 6 V/3 V		5/1	mA
	Power Down Mode <sup>(2)</sup>	V <sub>CC</sub> = 6 V		100	μA
		V <sub>CC</sub> = 3 V		20	μA

Notes: 1. Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows:  
 Maximum I<sub>OL</sub> per port pin: 10 mA  
 Maximum I<sub>OL</sub> per 8-bit port:  
 Port 0: 26 mA  
 Ports 1, 2, 3: 15 mA  
 Maximum total I<sub>OL</sub> for all output pins: 71 mA

If I<sub>OL</sub> exceeds the test condition, V<sub>OL</sub> may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V<sub>CC</sub> for Power Down is 2 V.

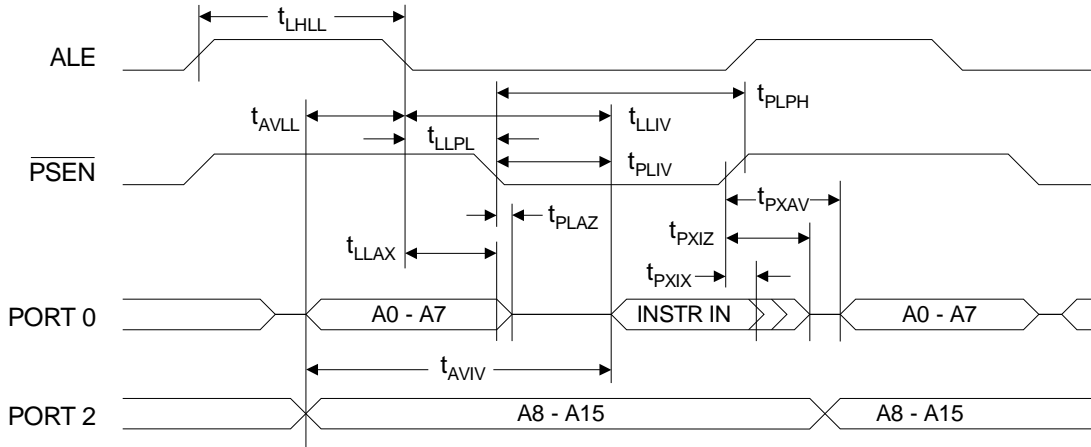
## A.C. Characteristics

Under operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other outputs = 80 pF.

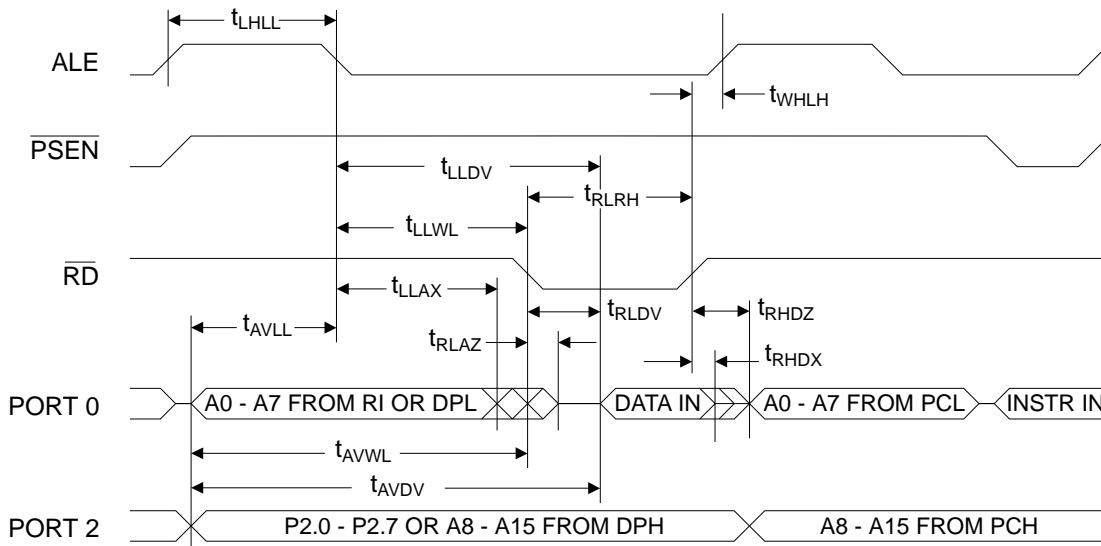
### External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/tCLCL	Oscillator Frequency			0	12	MHz
tLHLL	ALE Pulse Width	127		2tCLCL-40		ns
tAVLL	Address Valid to ALE Low	28		tCLCL-25		ns
tLLAX	Address Hold After ALE Low	48		tCLCL-25		ns
tLLIV	ALE Low to Valid Instruction In		233		4tCLCL-65	ns
tLLPL	ALE Low to PSEN Low	43		tCLCL-25		ns
tPLPH	PSEN Pulse Width	205		3tCLCL-45		ns
tPLIV	PSEN Low to Valid Instruction In		145		3tCLCL-60	ns
tPXIX	Input Instruction Hold After PSEN	0		0		ns
tPXIZ	Input Instruction Float After PSEN		59		tCLCL-25	ns
tPXAV	PSEN to Address Valid	75		tCLCL-8		ns
tAVIV	Address to Valid Instruction In		312		5tCLCL-80	ns
tPLAZ	PSEN Low to Address Float		10		10	ns
tRLRH	RD Pulse Width	400		6tCLCL-100		ns
tWLWH	WR Pulse Width	400		6tCLCL-100		ns
tRLDV	RD Low to Valid Data In		252		5tCLCL-90	ns
tRHDX	Data Hold After RD	0		0		ns
tRHDZ	Data Float After RD		97		2tCLCL-28	ns
tLLDV	ALE Low to Valid Data In		517		8tCLCL-150	ns
tAVDV	Address to Valid Data In		585		9tCLCL-165	ns
tLLWL	ALE Low to RD or WR Low	200	300	3tCLCL-50	3tCLCL+50	ns
tAVWL	Address to RD or WR Low	203		4tCLCL-75		ns
tQVWX	Data Valid to WR Transition	23		tCLCL-30		ns
tQVWH	Data Valid to WR High	433		7tCLCL-120		ns
tWHQX	Data Hold After WR	33		tCLCL-25		ns
tRLAZ	RD Low to Address Float		0		0	ns
tWHLH	RD or WR High to ALE High	43	123	tCLCL-25	tCLCL+25	ns

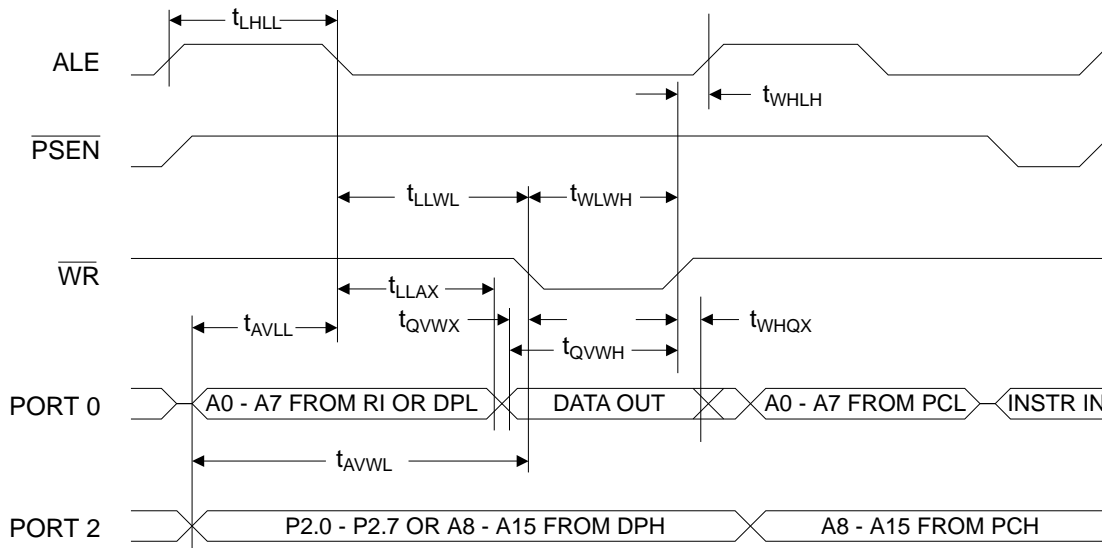
### External Program Memory Read Cycle



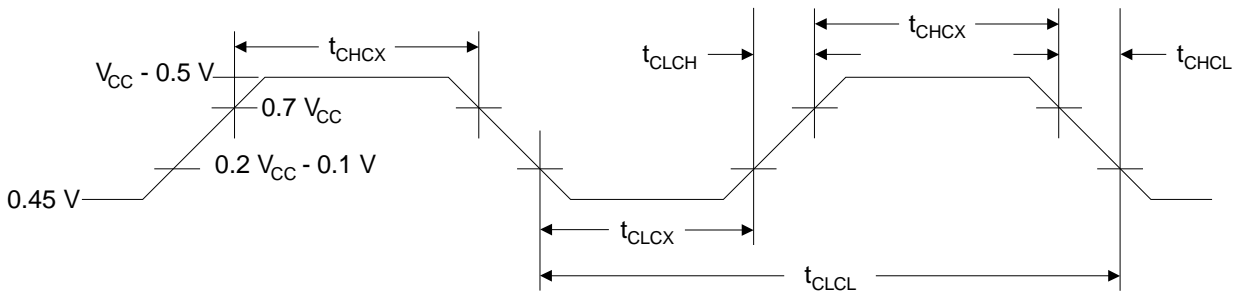
### External Data Memory Read Cycle



## External Data Memory Cycle



## External Clock Drive Waveforms



## External Clock Drive

$T_A = -40^{\circ}C$  to  $85^{\circ}C$

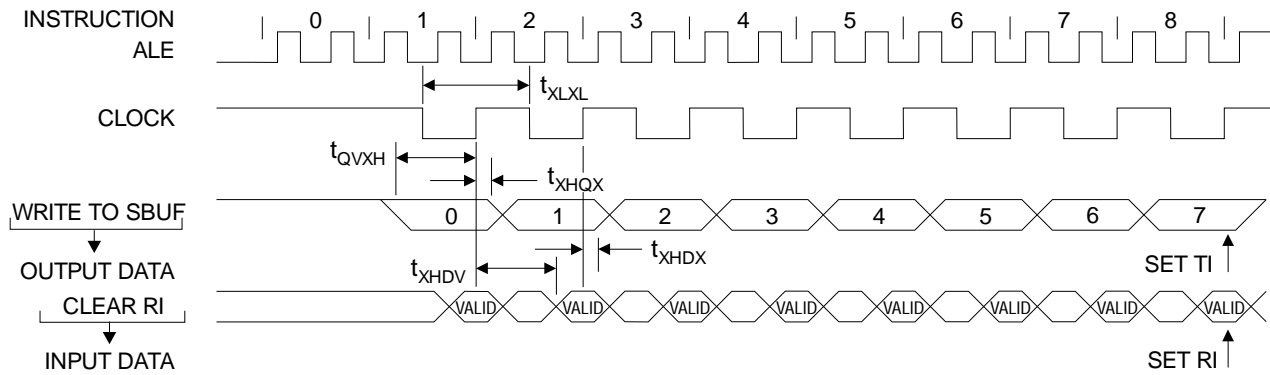
Symbol	Parameter	Min			Max			Units
		$V_{CC} = 2.7 V$	$V_{CC} = 3.0 V$	$V_{CC} = 3.3 V$	$V_{CC} = 2.7 V$	$V_{CC} = 3.0 V$	$V_{CC} = 3.3 V$	
$1/t_{CLCL}$	Oscillator Frequency	0	0	0	12	16	20	MHz
$t_{CLCL}$	Clock Period	83.3	62.5	50				ns
$t_{CHCX}$	High Time	20	15	10				ns
$t_{CLCX}$	Low Time	20	15	10				ns
$t_{CLCH}$	Rise Time				20	15	10	ns
$t_{CHCL}$	Fall Time				20	15	10	ns

## Serial Port Timing: Shift Register Mode Test Conditions

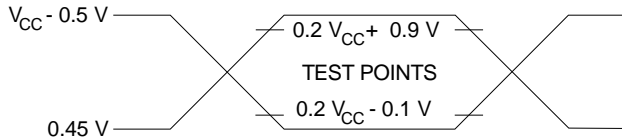
(V<sub>CC</sub> = 2.7 V to 6 V; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t <sub>XLXL</sub>	Serial Port Clock Cycle Time	1.0		12t <sub>CLCL</sub>		μs
t <sub>QVXH</sub>	Output Data Setup to Clock Rising Edge	700		10t <sub>CLCL</sub> -133		ns
t <sub>XHQX</sub>	Output Data Hold After Clock Rising Edge	50		2t <sub>CLCL</sub> -117		ns
t <sub>XHDX</sub>	Input Data Hold After Clock Rising Edge	0		0		ns
t <sub>XHDV</sub>	Clock Rising Edge to Input Data Valid		700		10t <sub>CLCL</sub> -133	ns

## Shift Register Mode Timing Waveforms

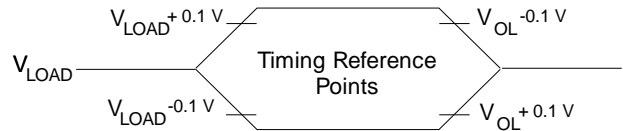


## AC Testing Input/Output Waveforms <sup>(1)</sup>



Note: 1. AC Inputs during testing are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

## Float Waveforms <sup>(1)</sup>

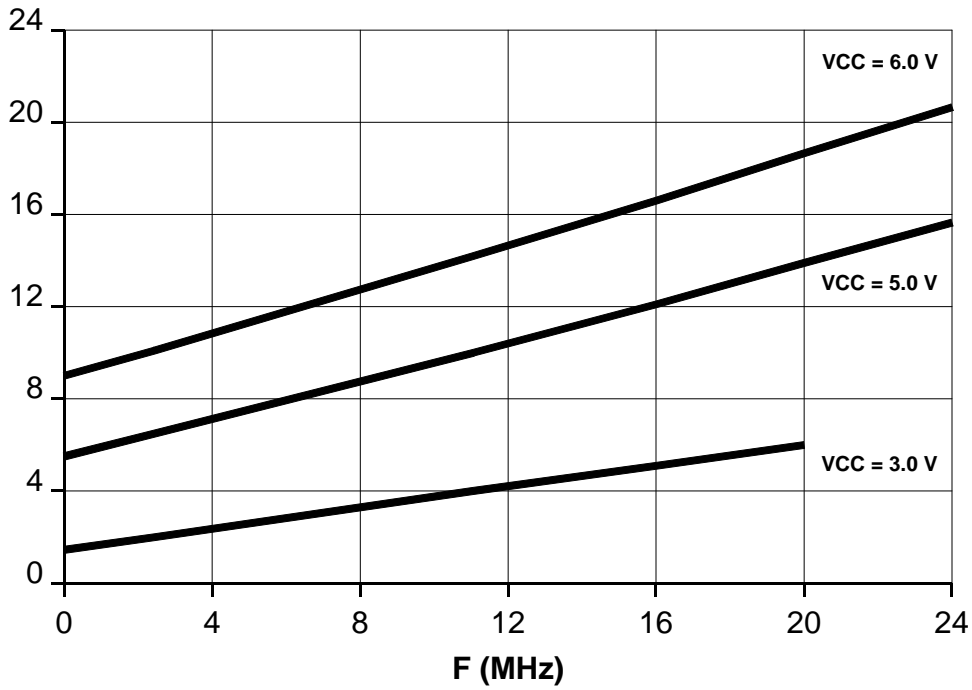


Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V<sub>OH</sub>/V<sub>OL</sub> level occurs.



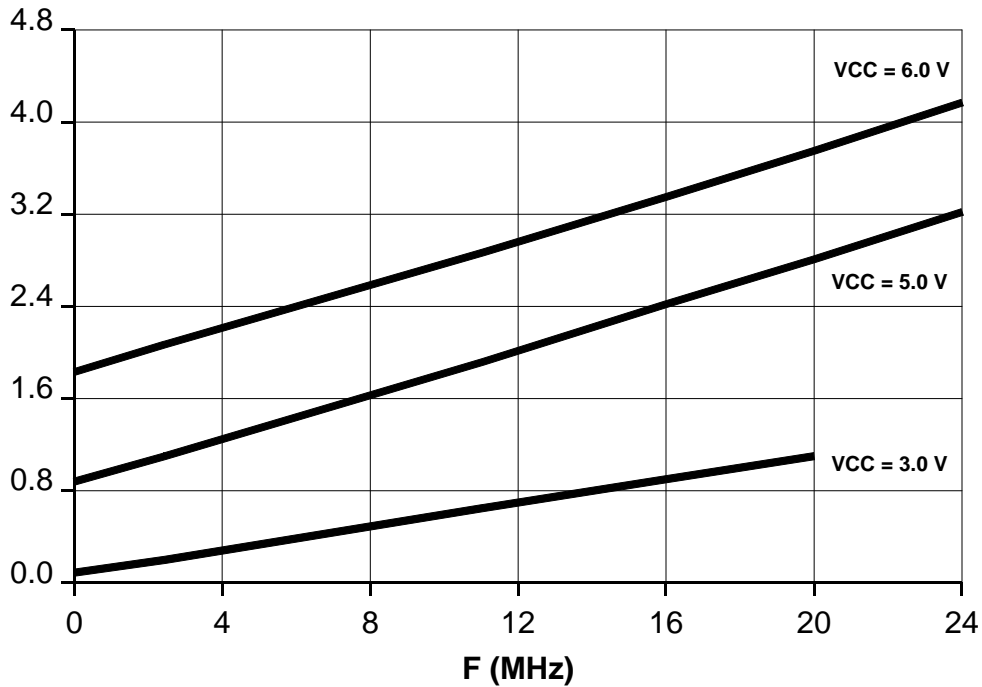
# AT89LV51

ICC (mA) TYPICAL ICC (ACTIVE) at 25° C

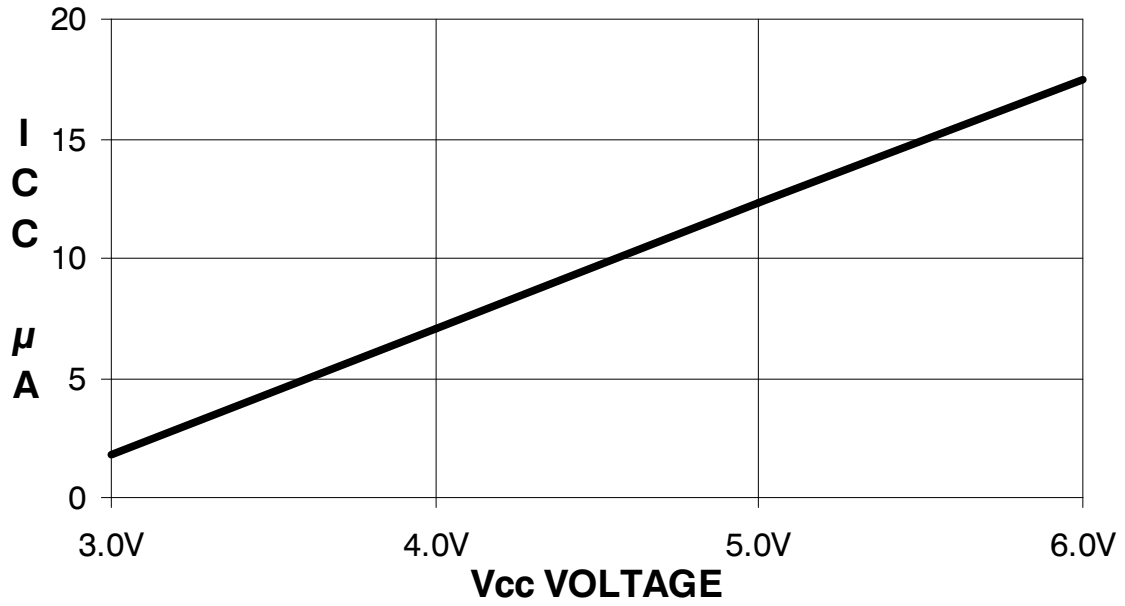


# AT89LV51

ICC (mA) TYPICAL ICC (IDLE) at 25° C



### AT89LV51 TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)





## Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	2.7 V to 6 V	AT89LV51-12AC AT89LV51-12JC AT89LV51-12PC AT89LV51-12QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

## Ordering Information

Package Type	
<b>44A</b>	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
<b>44J</b>	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
<b>40P6</b>	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
<b>44Q</b>	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)