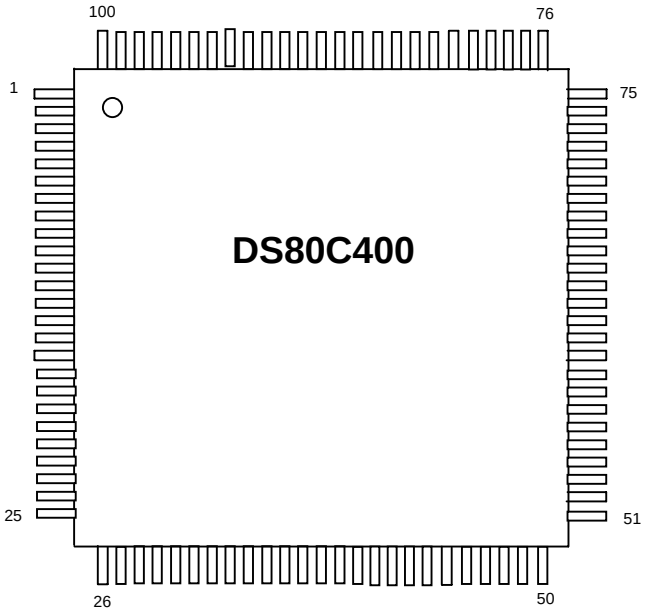
DALLAS SEMICONDUCTOR

DS80C400
Network Microcontroller

FEATURES

- **High-Performance Architecture**
  - Single 8051 instruction cycle in 54 ns
  - DC to 75 MHz clock rate
  - Flat 16 MB address space
  - Four data pointers with auto-inc/dec and select accelerate data movement
  - 16/32-bit math accelerator
- **Multitiered Networking and I/O**
  - 10/100 Ethernet Media Access Controller (MAC)
  - CAN 2.0B controller
  - 1-Wire™ net controller
  - Three full-duplex hardware serial ports
  - Up to eight bi-directional 8-bit ports (64 digital I/O pins)
- **Robust ROM Firmware**
  - Supports network boot over Ethernet using DHCP and TFTP
  - Full, application-accessible TCP/IP network stack
  - Supports IPv4 and IPv6
  - Implements UDP, TCP, DHCP, ICMP, and IGMP
  - Preemptive, priority based task scheduler
  - MAC address can optionally be acquired from IEEE-registered DS2502-E48
- **10/100 Ethernet MAC**
  - Flexible IEEE 802.3 MII (10/100 Mbps) and ENDEC (10 Mbps) interfaces allow selection of PHY
  - Low-power operation
  - Ultra low-power sleep mode with Magic Packet and wake-up frame detection
  - 8kB on-chip TX/RX packet data memory with Buffer Control Unit reduces load on CPU
  - Half- or full-duplex operation with flow control
  - Multicast/Broadcast address filtering with VLAN support

PIN ASSIGNMENT



100-PIN LQFP
(TOP VIEW)

- **Full-Function CAN 2.0B Controller**
  - 15 message centers
  - Supports standard (11-bit) and extended (29-bit) identifiers and global masks
  - Media byte filtering to support DeviceNet™, SDS, and higher layer CAN protocols
  - Auto-baud mode and SIESTA low power mode
- **Integrated Primary System Logic**
  - 16 total interrupt sources with 6 external
  - Four 16-bit timer/counters
  - 2X/4X Clock Multiplier reduces EMI
  - Programmable watchdog timer

- Oscillator fail detection
- Programmable IrDA clock

- **Advanced Power Management**
  - Energy saving 1.8V Core
  - 3.3V I/O Operation, 5V tolerant
  - Power Management, idle and stop mode operation with switchback feature
  - Ethernet and CAN shutdown control for power conservation
  - Early warning power-fail interrupt
  - Power-fail reset
- **Enhanced Memory Architecture**
  - Selectable 8/10-bit stack pointer for high-level language support
  - 1kB additional on-chip SRAM usable as stack/data memory
  - 16-bit / 24-bit paged / 24-bit contiguous modes
  - Selectable multiplexed / non-multiplexed external memory interface
  - Merged program/data memory space allows in-system programming
  - Defaults to true 8051 memory compatibility

DESCRIPTION

The DS80C400 is a fast 8051-compatible microcontroller that executes instructions up to 3 times faster than an original 8051 at the same crystal speed. A maximum system clock frequency of 75 MHz, results in a minimum instruction cycle time of 54 ns. Access to large program or data memory areas is simplified with a 24-bit addressing scheme that supports up to 16MB of flat memory. To accelerate data transfers between the microcontroller and the 16MB memory map, the DS80C400 provides four data pointers, each of which can be configured to automatically increment or decrement upon execution of certain data pointer related instructions. The mircocontroller's hardware math accelerator further increases the speed of 32 and 16 bit multiply and divide operations, as well as high-speed shift, normalization and accumulate functions.

With extensive networking and I/O capabilities, the DS80C400 is equipped to serve as a central controller in a multitiered network. The 10/100 Ethernet Media Access Controller (MAC) enables the DS80C400 to access and communicate over the Internet. While maintaining a presence on the Internet, the microcontroller can actively control lower tier networks with dedicated on-chip hardware. These hardware resources include a full CAN 2.0B controller, a 1-Wire net controller, three full-duplex serial ports, and eight 8-bit ports (up to 64 digital I/O pins).

Instant connectivity and networking support are provided via an embedded 64kB ROM. This ROM contains firmware to perform a network boot over an Ethernet connection using DHCP in conjunction with TFTP. The ROM firmware realizes a full, application accessible, TCP/IP stack, supporting both IPv4 and IPv6, and implements UDP, TCP, DHCP, ICMP, and IGMP. In addition, a priority based, preemptive task scheduler is also included. The firmware has been structured so that a MAC address can optionally be acquired from an IEEE registered DS2502-E48.

The 10/100 Ethernet MAC featured on the DS80C400 complies with both the IEEE 802.3 MII and ENDEC PHY interface standards. The MII interface supports 10/100 Mbps bus operation, while the ENDEC interface supports 10Mbps operation. The MAC has been designed for low power standard operation and can optionally be placed into an ultra low-power sleep mode, to be awakened manually or by detection of a Magic Packet or wake-up frame. Incorporating a Buffer Control Unit reduces the burden of Ethernet traffic on the CPU. This Unit, after initial configuration through an SFR interface, manages all TX/RX packet activity and status reporting through an on-chip 8kB SRAM. To further reduce host (DS80C400) software intervention, the MAC can be setup to generate a hardware interrupt following each transmit or receive status report. The DS80C400 MAC can be operated in half-duplex or full-duplex mode with flow control and provides Multicast/Broadcast address filtering modes as well as VLAN tag recognition capability.

The DS80C400 features a full-function Controller Area Network (CAN) 2.0B controller. This controller provides 15 total message centers, 14 of which can be configured as either transmit or receive buffers and 1 which can serve as a receive double buffer. The device supports standard 11-bit or 29-extended message identifiers, and offers two separate 8-bit media masks and media arbitration fields to support the use of higher-level CAN protocols such as DeviceNet™ and SDS. A special auto-baud mode allows the CAN controller to quickly determine required bus timing when inserted into a new network. A SIESTA sleep mode has been made available for times when the CAN controller can be placed into a power saving mode.

The DS80C400 has resources that far exceed those normally provided on a standard 8-bit microcontroller. Many functions, which might exist as peripheral circuits to a microcontroller, have been integrated into the DS80C400. Some of the integrated functions of the DS80C400 include: 16 interrupt sources (6

oscillator fail detection circuit, and an internal 2X/4X clock multiplier. This frequency multiplier allows the microcontroller to operate at full speed with a reduced crystal frequency, reducing EMI.

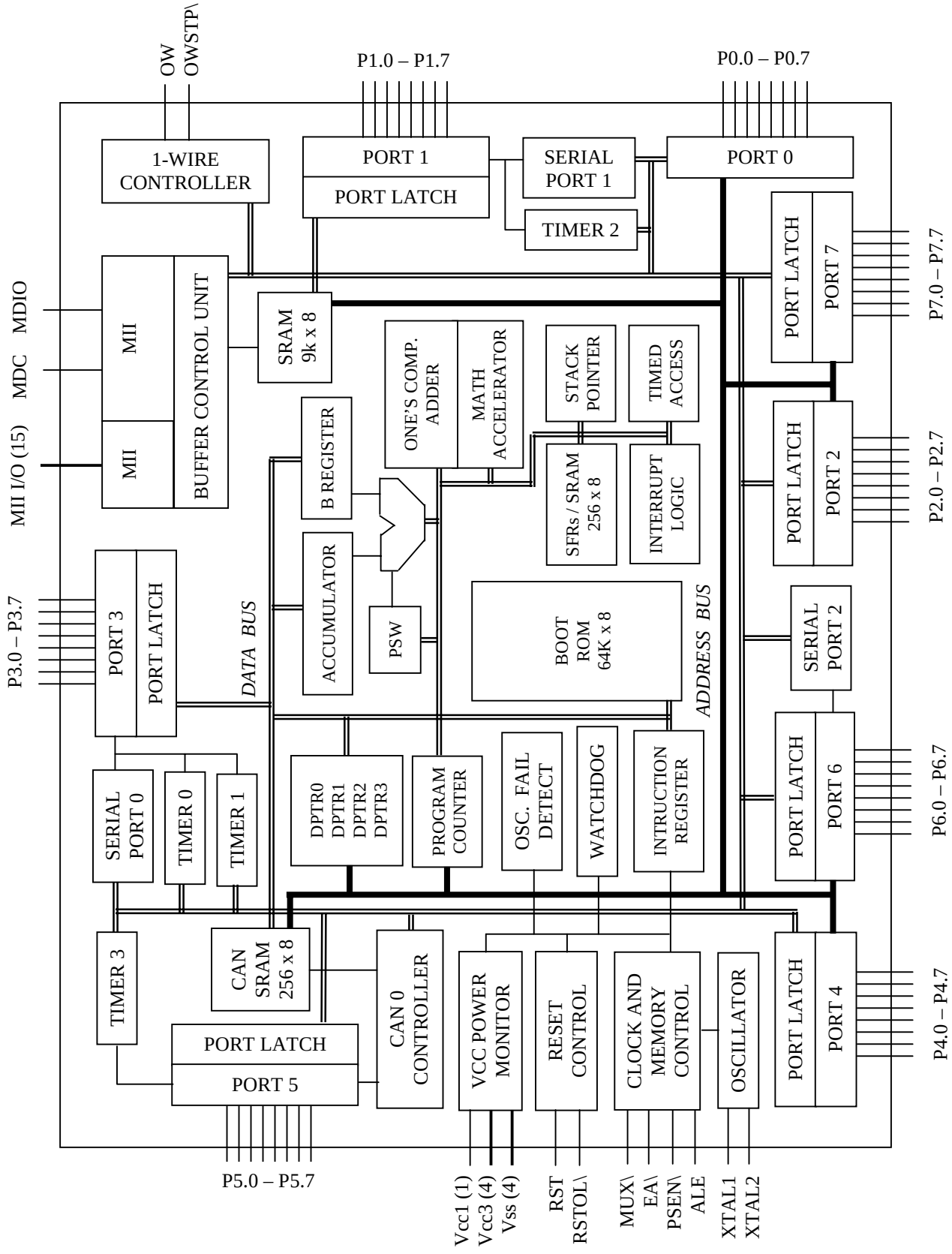
An advanced power management support positions the DS80C400 for portable and power conscious applications. The low voltage microcontroller core runs from a 1.8V supply while the I/O remains 5V tolerant, operating from a 3.3V supply. A Power Management Mode (PMM) allows software to switch from the standard machine cycle rate of 4 clocks per cycle to 1024 clocks per cycle. For example, 40 MHz standard operation has a machine cycle rate of 10 MHz. In Power Management Mode, at the same external clock speed, software can select a 39 kHz machine cycle rate, considerably reducing power consumption. The microcontroller can be configured to automatically switch back from PMM to the faster mode in response to external interrupts or serial port activity. The DS80C400 provides the ability to place the CPU into an idle state or an ultra low power stop mode state. As protection against brown-out and power-fail conditions, the microcontroller is capable of issuing an early warning power-fail interrupt and can generate a power-fail reset.

Defaulting to true 8051 memory compatibility, the microcontroller is most powerful when taking advantage of its enhanced memory architecture. The DS80C400 has a selectable 10-bit stack pointer that can address up to 1kB of on-chip SRAM stack space for increased code efficiency. The DS80C400 can be operated in a 24-bit paged or 24-bit contiguous address mode, giving access to a much larger address range than the standard 16-bit address mode. Support for merged program and data memory access allows in-system programming and can be configured to internally demultiplex data and the lowest address byte, thereby eliminating the need for an external latch and potentially allowing the use of slower memory devices.

ORDERING INFORMATION

Part Number	Package	Max. Clock Speed	Operating Temperature Range
DS80C400-FNY	100-pin LQFP	75 MHz	-40°C to +85°C

DS80C400 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

LQFP	SIGNAL NAME	DESCRIPTION
70	V_{CC1}	**+1.8V Core Supply Voltage**
12, 36, 62, 87	V_{CC3}	**+3.3V I/O Supply Voltage**
13, 39, 63, 88	V_{SS}	**Digital Circuit Ground**
68	ALE	**Address Latch Enable** - Output. When the $\overline{MUX}$ pin is low, this pin outputs a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. When the $\overline{MUX}$ pin is high, the pin will toggle continuously if the ALEOFF bit is cleared. ALE is forced high when the device is in a Reset condition or if the ALEOFF bit is set while the $\overline{MUX}$ pin is high.
67	$\overline{PSEN}$	**Program Store Enable** – Output. This signal is the chip enable for external ROM memory. $\overline{PSEN}$ provides an active low pulse and is driven high when external ROM is not being accessed.
69	$\overline{EA}$	**External Access Enable** - Input. Connect to GND to use external program memory. Connect to Vcc to use internal ROM.
40	$\overline{MUX}$	**Multiplex/Demultiplex Select** - Input. This pin selects if the address/data bus operates in multiplexed ($\overline{MUX}$ =0) or demultiplexed ($\overline{MUX}$ =1) mode.
97	RST	**Reset** - Input. The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pull-down resistor to allow for a combination of wired OR external Reset sources. An RC circuit is not required for power-up, as the device provides this function internally.
98	$\overline{RSTOL}$	**Reset Output Low** - Output. This active low signal will be asserted: When the microcontroller has entered reset via the RST pin, During crystal warm-up period following power-on or Stop mode, During a watchdog timer reset (2 cycles duration), During an oscillator failure (if OFDE=1), Whenever $V_{CC1} \le V_{RST1}$ or $V_{CC3} \le V_{RST3}$
37, 38	XTAL2, XTAL1	**XTAL1, XTAL2** - Crystal oscillator pins support fundamental mode, parallel resonant, AT cut crystals. XTAL1 is the input if an external clock source is used in place of a crystal. XTAL2 is the output of the crystal amplifier.

		AD0-7 (Port 0) - I/O. When the $\overline{\text{MUX}}$ pin is tied low, Port 0 is the multiplexed address/data bus. While ALE is high, the LSB of a memory address is presented. While ALE falls, the port transitions to a bi-directional data bus. When the $\overline{\text{MUX}}$ pin is tied high, Port 0 functions as the bi-directional data bus. Port 0 cannot be modified by software. The reset condition of Port 0 pins is high. No pull-up resistors are needed. **Port Alternate Function**
86	AD0 / D0	P0.0 AD0 / D0 (Address)/Data 0
85	AD1 / D1	P0.1 AD1 / D1 (Address)/Data 1
84	AD2 / D2	P0.2 AD2 / D2 (Address)/Data 2
83	AD3 / D3	P0.3 AD3 / D3 (Address)/Data 3
82	AD4 / D4	P0.4 AD4 / D4 (Address)/Data 4
81	AD5 / D5	P0.5 AD5 / D5 (Address)/Data 5
80	AD6 / D6	P0.6 AD6 / D6 (Address)/Data 6
79	AD7 / D7	P0.7 AD7 / D7 (Address)/Data 7
	P1.0-P1.7	**Port 1** – I/O. Port 1 can function as either an 8-bit bi-directional I/O port or as an alternate interface for internal resources. The reset condition of Port 1 is all bits at logic 1 via a weak pull-up. The logic 1 state also serves as an input mode, since external circuits writing to the port can overdrive the weak pull-up. When software clears any port pin to 0, a strong pull-down is activated that remains on until either a 1 is written to the port pin or a reset occurs. Writing a 1 after the port has been at 0 will activate a strong transition driver, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port once again becomes the output (and input) high state. **Port Alternate Function**
89		P1.0 T2 External I/O for Timer/Counter 2
90		P1.1 T2EX Timer/Counter 2 Capture/Reload Trigger
91		P1.2 RXD1 Serial Port 1 Receive
92		P1.3 TXD1 Serial Port 1 Transmit
93		P1.4 INT2 External Interrupt 2 (Pos. Edge Detect)
94		P1.5 $\overline{\text{INT3}}$ External Interrupt 3 (Neg. Edge Detect)
95		P1.6 INT4 External Interrupt 4 (Pos. Edge Detect)
96		P1.7 $\overline{\text{INT5}}$ External Interrupt 5 (Neg. Edge Detect)

		A15-A8 (Port 2) - Output. Port 2 serves as the MSB for external addressing. The port automatically asserts the address MSB during external ROM and RAM access. Although the Port 2 SFR exists, the SFR value will never appear on the pins (due to memory access). Therefore accessing the Port 2 SFR is only useful for MOVX A, @Ri or MOVX @Ri, A instructions, which use the Port 2 SFR as the external address MSB. **Port Alternate Function** P2.0 A8 Program/Data Memory Address 8 P2.1 A9 Program/Data Memory Address 9 P2.2 A10 Program/Data Memory Address 10 P2.3 A11 Program/Data Memory Address 11 P2.4 A12 Program/Data Memory Address 12 P2.5 A13 Program/Data Memory Address 13 P2.6 A14 Program/Data Memory Address 14 P2.7 A15 Program/Data Memory Address 15
66 65 64 61 60 59 58 57	A8 A9 A10 A11 A12 A13 A14 A15	
	P3.0-P3.7	**Port 3** - I/O. Port 3 functions as an 8-bit bi-directional I/O port, and as an alternate interface for several resources found on the traditional 8051. The reset condition of Port 3 is all bits at logic 1 via a weak pull-up. The logic 1 state also serves as an input mode, since external circuits writing to the port can overdrive the weak pull-up. When software clears any port pin to 0, the device activates a strong pull-down that remains on until either a 1 is written to the port pin or a reset occurs. Writing a 1 after the port has been at 0 will activate a strong transition driver, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port once again becomes the output (and input) high state. **Port Alternate Function** P3.0 RXD0 Serial Port 0 Receive P3.1 TXD0 Serial Port 0 Transmit P3.2 $\overline{\text{INT0}}$ External Interrupt 0 P3.3 $\overline{\text{INT1}}$ External Interrupt 1 P3.4 T0 Timer 0 External Input P3.5 T1/CLKO Timer 1 External Input/External Clock Output P3.6 $\overline{\text{WR}}$ External Data Memory Write Strobe P3.7 $\overline{\text{RD}}$ External Data Memory Read Strobe
20 21 22 23 24 25 26 27		

	P4.0-P4.7	**Port 4** - I/O. Port 4 can function as an 8-bit bi-directional I/O port, and as the source for external address and chip enable signals for program and data memory. Port pins are configured as I/O or memory signals via the P4CNT register. The reset condition of Port 4 is all bits at logic 1 via a weak pull-up. The logic 1 state also serves as an input mode, since external circuits writing to the port can overdrive the weak pull-up. When software clears any port pin to 0, the device activates a strong pull-down that remains on until either a 1 is written to the port pin or a reset occurs. Writing a 1 after the port has been at 0 will activate a strong transition driver, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port once again becomes the output (and input) high state.
48		P4.0 $\overline{CE0}$ Program Memory Chip Enable 0
47		P4.1 $\overline{CE1}$ Program Memory Chip Enable 1
46		P4.2 $\overline{CE2}$ Program Memory Chip Enable 2
45		P4.3 $\overline{CE3}$ Program Memory Chip Enable 3
44		P4.4 A16 Program/Data Memory Address 16
43		P4.5 A17 Program/Data Memory Address 17
42		P4.6 A18 Program/Data Memory Address 18
41		P4.7 A19 Program/Data Memory Address 19
	P5.0-P5.7	**Port 5** - I/O. Port 5 can function as an 8-bit bi-directional I/O port, the CAN interface, Timer 3 input and/or as peripheral enable signals. The reset condition of Port 5 is all bits at logic 1 via a weak pull-up. The logic 1 state also serves as an input mode, since external circuits writing to the port can overdrive the weak pull-up. When software clears any port pin to 0, the device activates a strong pull-down that remains on until either a 1 is written to the port pin or a reset occurs. Writing a 1 after the port has been at 0 will activate a strong transition driver, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port once again becomes the output (and input) high state.
		Port Alternate Function
35		P5.0 C0TX CAN0 Transmit Output
34		P5.1 C0RX CAN0 Receive Input
33		P5.2 T3 Timer 3 External Input
32		P5.3 none
31		P5.4 $\overline{PCE0}$ Peripheral Chip Enable 0
30		P5.5 $\overline{PCE1}$ Peripheral Chip Enable 1
29		P5.6 $\overline{PCE2}$ Peripheral Chip Enable 2
28		P5.7 $\overline{PCE3}$ Peripheral Chip Enable 3

	P6.0-P6.7	**Port 6 –** I/O. Port 6 can function as an 8-bit bi-directional I/O port, as program and data memory address / chip enable signals and/or a third serial port. The reset condition of Port 6 is all bits at logic 1 via a weak pull-up. The logic 1 state also serves as an input mode, since external circuits writing to the port can overdrive the weak pull-up. When software clears any port pin to 0, the device activates a strong pull-down that remains on until either a 1 is written to the port pin or a reset occurs. Writing a 1 after the port has been at 0 will activate a strong transition driver, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port once again becomes the output (and input) high state. **Port Alternate Function**
56		P6.0 $\overline{\text{CE4}}$ Program Memory Chip Enable 4
55		P6.1 $\overline{\text{CE5}}$ Program Memory Chip Enable 5
54		P6.2 $\overline{\text{CE6}}$ Program Memory Chip Enable 6
53		P6.3 $\overline{\text{CE7}}$ Program Memory Chip Enable 7
52		P6.4 A20 Program/Data Memory Address 20
51		P6.5 A21 Program/Data Memory Address 21
50		P6.6 RXD2 Serial Port 2 Receive
49		P6.7 TXD2 Serial Port 2 Transmit
		Port 7 - I/O. Port 7 can function as either an 8-bit bi-directional I/O port or the non-multiplexed A0 - A7 signals (when the $\overline{\text{MUX}}$ pin =1). The reset condition of Port 7 is all bits at logic 1 via a weak pull-up. The logic 1 state also serves as an input mode, since external circuits writing to the port can overdrive the weak pull-up. When software clears any port pin to 0, a strong pull-down is activated that remains on until either a 1 is written to the port pin or a reset occurs. Writing a 1 after the port has been at 0 will activate a strong transition driver, followed by a weaker sustaining pull-up. Once the momentary strong driver turns off, the port once again becomes the output (and input) high state. **Port Alternate Function**
78	A0	P7.0 A0 Program/Data Memory Address 0
77	A1	P7.1 A1 Program/Data Memory Address 1
76	A2	P7.2 A2 Program/Data Memory Address 2
75	A3	P7.3 A3 Program/Data Memory Address 3
74	A4	P7.4 A4 Program/Data Memory Address 4
73	A5	P7.5 A5 Program/Data Memory Address 5
72	A6	P7.6 A6 Program/Data Memory Address 6
71	A7	P7.7 A7 Program/Data Memory Address 7

8	TXClk	**Transmit Clock** – Input. The transmit clock is a continuous clock sourced from the Ethernet PHY controller. It is used to provide timing reference for transferring of TX_EN and TXD[3:0] signals from the MAC to the external Ethernet PHY controller. The input clock frequency of TXClk should be 25Mhz for 100Mbps operation and 2.5Mhz for 10Mbps operation. For ENDEC operation, TXClk serves the same function, but the input clock frequency should be 10Mhz.
7	TX_EN	**Transmit Enable** – Output. The transmit enable is an active high output and is synchronous with respect to the TXClk signal. TX_EN is used to indicate valid nibbles of data for transmission on the MII pins TXD.3 – TXD.0. TX_EN is asserted with the first nibble of the preamble and will remain asserted while all nibbles to be transmitted are presented on the TXD.3 – TXD.0 pins. TX_EN will be negated prior to the first TXClk following the final nibble of the frame. TX_EN serves the same function for ENDEC operation.
3 4 5 6	TXD.3 TXD.2 TXD.1 TXD.0	**Transmit Data** – Output. The transmit data outputs provide 4-bit nibbles of data for transmission over the MII. The transmit data is synchronous with respect to the TXClk signal. For each TXClk period when TX_EN is asserted, TXD.3 – TXD.0 will provide the data for transmission to the Ethernet PHY controller. When TX_EN is deasserted, the TXD data should be ignored. For ENDEC operation, only TXD.0 is used for transmission of frames.
10	RXClk	**Receive Clock** – Input. The receive clock is a continuous clock sourced from the Ethernet PHY controller. It is used to provide timing reference for transferring of RX_DV, RX_ER, and RXD[3:0] signals from the external Ethernet PHY controller to the MAC. The input clock frequency of RXClk should be 25Mhz for 100Mbps operation and 2.5Mhz for 10Mbps operation. For ENDEC operation, RXClk serves the same function, but the input clock frequency should be 10Mhz.
11	RX_DV	**Receive Data Valid** – Input. The receive data valid is an active high input from the external Ethernet PHY controller and is synchronous with respect to the RXClk signal. RX_DV is used to indicate valid nibbles of data for reception on the MII pins RXD.3 – RXD.0. RX_DV is asserted continuously from the first nibble of the frame through the final nibble. RX_DV will be negated prior to the first RXClk following the final nibble. RX_DV serves the same function for ENDEC operation.
9	RX_ER	**Receive Error** – Input. The receive error is an active high input from the external Ethernet PHY controller and is synchronous with respect to the RXClk signal. RX_ER is used to indicate to the MAC that an error (e.g., a coding error, or any error detectable by the PHY) was detected somewhere in the frame presently being transmitted by the PHY. RX_ER will have no effect on the MAC while RX_DV is deasserted. RX_ER should be low for ENDEC operation.

17 16 15 14	RXD.3 RXD.2 RXD.1 RXD.0	**Receive Data** – Input. The receive data inputs provide 4-bit nibbles of data for reception over the MII. The receive data is synchronous with respect to the RXClk signal. For each RXClk period when RX_DV is asserted, RXD.3 – RXD.0 will have the data to be received by the MAC. When RX_DV is deasserted, the RXD data should be ignored. For ENDEC operation, only RXD.0 is used for reception of frames.
1	CRS	**Carrier Sense** – Input. The carrier sense signal is an active high input and should be asserted by the external Ethernet PHY controller when either transmit or receive medium is not idle. CRS should be deasserted by the PHY when both transmit and receive medium are idle. The PHY should ensure that the CRS signal remains asserted throughout the duration of a collision condition. The transitions on the CRS signal need not be synchronous to TXClk or RXClk. CRS serves the same function for ENDEC operation.
2	COL	**Collision Detect** – Input. The collision detect signal is an active high input and should be asserted by the external Ethernet PHY controller upon detection of a collision on the medium. The PHY should ensure that COL remains asserted while the collision condition persists. The transitions on the COL signal need not be synchronous to TXClk or RXClk. The COL signal is ignored by the MAC when operating in full-duplex mode. COL serves the same function for ENDEC operation.
18	MDC	**MII Management Clock** – Output. The MII Management Clock is generated by the MAC for use by the external Ethernet PHY controller as a timing referenced for transferring information on the MDIO pin. MDC is a periodic signal that has no maximum high or low times. The minimum high and low times will be 160ns each. The minimum period for MDC will be 400ns independent of the period of TXClk and RXClk.
19	MDIO	**MII Management Input/Output** – I/O. The MII Management I/O is the data pin for serial communication with the external Ethernet PHY controller. In a read cycle, data is driven by the PHY to the MAC synchronously with respect to the MDC clock. In a write cycle, data from the MAC is output to the external PHY synchronously with respect to the MDC clock.
99	OW	**1-Wire Data** – I/O. The 1-Wire data pin is an open-drain, bi-directional data bus for the 1-Wire Bus Master. External 1-Wire slave devices are connected to this pin. This pin must be pulled high by an external resistor, normally 2.2K ohms.
100	$\overline{\text{OWSTP}}$	**Strong Pull-up Enable** – Output. This 1-Wire pin is an open-drain active low output used to enable an external strong pull-up for the 1-Wire bus. This pin must be pulled high by an external resistor, normally 10K ohms. This functionality will help recovery times when the 1-Wire bus is operated in overdrive and long-line standard communication modes. It can optionally be enabled while the bus master is in the idle state for slave devices requiring sustained high current operation.