Intel® StrongARM* SA-1110 Microprocessor

Specification Update

December 2000

Notice: The SA-1110 may contain design defects or errors known as errata. Characterized errata that may cause the SA-1110's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278259-020

Contents

Revision History

Date	Version	Description
12/08/00	020	New Errata item 28, “Incorrect Address Decode in USB Controller” (page 26) has been added. Under Documentation Changes, added item 19, “Real-Time Clock: Section 9.3” (page 36), item 20, “RTC Status Register (RTSR): Section 9.3.3” (page 36), item 22, “DRAM Refresh Control Register (MDREFR): Section 10.2.2” (page 37), item 23, “SMROM Configuration Register (SMCNFG): Section 10.3” (page 37), item 25, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 37), item 26, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 38), item 27, “DMA Control/Status Register (DCSRn): Section 11.6.1.2” (page 38), item 28, “DMA Control/Status Register (DCSRn): Section 11.6.1.2” (page 38), item 29, “DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4” (page 38), item 30, “DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6” (page 39), item 35, “Palette DMA Request Delay (PDD): Section 11.7.3.10” (page 41), item 43, “LCD Controller Register Locations: Section 11.7.12” (page 43), item 44, “UDC Endpoint Data Register: Section 11.8.10” (page 44), item 45, “UDC Data Register: Section 11.8.12” (page 44), item 48, “UART Data Register: Section 11.11.6” (page 45), item 49, “SSP Transmit and Receive FIFOs: Section 11.12.7.3” (page 45), item 50, “SSP Data Register: Section 11.12.11” (page 45), item 51, “PPC Pin Direction Register: Section 11.13.3” (page 46), item 52, “PPC Pin State Register: Section 11.13.4” (page 46), and item 53, “PPC Pin Assignment Register: Section 11.13.5.2” (page 46).
10/20/00	019	New Errata item 27, “Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written” (page 25) has been added. New Specification Change item 3, “Modifications in SDRAM/SMROM Data Input Hold Time” (page 30) has been added. Under Documentation Changes, added item 17, “Read Buffer: Section 6.4” (page 35), item 22, “DRAM Refresh Control Register (MDREFR): Section 10.2.2” (page 37), item 23, “SMROM Configuration Register (SMCNFG): Section 10.3” (page 37), item 31, “Frame Buffer: Section 11.7.1.2” (page 39), item 38, “Output Enable Polarity (OEP): Section 11.7.6.7” (page 42), item 41, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 43), item 43, “LCD Controller Register Locations: Section 11.7.12” (page 43), item 47, “Sample Clock GPIO: Section 11.11.3.5” (page 44), item 54, “DC Operating Conditions: Section 12.2” (page 47), item 56, “Timing Parameters: Section 13.6” (page 49), and item 60, “Boundary Scan Interface Signals: Section 16.7” (page 51).

Date	Version	Description
9/12/00	018	Under Errata item 21, “Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request” (page 24) -- the workaround instructions have been modified. In Item 24, “Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup” (page 25) the “affected steppings” have been modified (affects all steppings). New items 25, “Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count)” (page 25) and 26, “Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller” (page 25) have been added. Under Documentation Changes, removed documentation changes 1-6, 8-11, 13-20, 23-28, 30, 32, 34-36, 39-97 (having been incorporated into revision -003 of the developer’s manual) respective to Specification Update Revision 017. Under Documentation Changes, modified documentation change 21 (respective to revision 017) by removing the description for changing ‘9 bits’ to ‘9 bytes’ as this part of the modification was already implemented in revision -003 of the developer’s manual. Modified documentation change 22 (respective to revision 017) by removing the description for changing bits 24 and 25 as this part of the modification is no longer required. The new descriptions of these changes are now documentation changes 3 and 4. Under Documentation Changes, added item 10, “Register 14 – Debug Support (Breakpoints): Section 5.2.13” (page 34) item 11, “Data Caches (Dcaches): Section 6.2” (page 34), item 12, “Writes to a Bufferable and Noncacheable Location (B=1,C=0): Section 6.3.2.2” (page 35), item 13, “Unbufferable and Noncacheable Writes (B=0, C=0): Section 6.3.2.3” (page 35), item 14, “Writes to a Non-Bufferable and Cacheable Location (B=0, C=1): Section 6.3.2.4” (page 35), item 15, “Read Buffer (RB): Section 6.4” (page 35), item 16, “Read Buffer: Section 6.4” (page 35), item 21, “Sleep Mode: Section 9.5.3” (page 37), item 24, “8-, 16-, and 32-Bit Data Bus Operation: Section 10.6.1” (page 37), item 26, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 38), item 31, “Frame Buffer: Section 11.7.1.2” (page 39), item 32, “Passive/Active Display Select (PAS): Section 11.7.3.7” (page 40), item 33, “Passive/Active Display Select (PAS): Section 11.7.3.7” (page 41), item 34, “Palette DMA Request Delay (PDD): Section 11.7.3.10” (page 41)item 36, “Beginning-of-Frame Line Clock Wait Count (BFW): Section 11.7.5.4” (page 42), item 39, “DMA Channel 1 Current Address Register: Section 11.7.9” (page 43), item 40, “Output FIFO Underrun Lower Panel Status (OUL) (read only, maskable interrupt): Section 11.7.10” (page 43), item 41, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 43), item 41, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 43), item 43, “LCD Controller Register Locations: Section 11.7.12” (page 43), item 54, “DC Operating Conditions: Section 12.2” (page 47), item 55, “Power Supply Voltages and Currents: Section 12.3” (page 47), item 56, “Timing Parameters: Section 13.6” (page 49), item 57, “Timing Parameters: Section 13.6” (page 50), item 58, “Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2” (page 50), and item 59, “Boundary-Scan Interface Signals: Section 16.7” (page 50).
6/22/00	017	Under Documentation Changes, added to documentation change 2 two tables to Section 13.1 describing output derating parameters for slow and fast output buffers, removed documentation changes 3—63 (having been incorporated into the revision 003 developer’s manual) respective to Specification Update Revision 016. Also added updated information for the Reset Interrupt Mask, Receive Packet Error bit, Force Stall bit, and the UDC Control Register. Added information describing: Software Control of the UDC; a new section entitled “GPCLK Control Register 1”; changed section formally named “GPCLK Control Registers 1 and 2”; updated the table in the “GPCLK Register Locations” section. Made sentence corrections to the following sections: Serial Port 3 – UART; Baud Rate Divisor (BRD); Baud Rate Generation. Made general format corrections. Corrected bit assignment values to registers in Chapter 11. Rewrote sections 11.8.3, 11.8.3.4, 11.8.3.5, 11.8.3.6, 11.8.3.7, 11.8.3.3, 11.8.13.2, 11.8.13.13, 11.8.13.4, 11.8.13.5, 11.9, 9.3.4. Restructured Section 10.4.1. Added a note as appropriate in Chapters 9 and 11 to identify the use of a question mark as a value designator in register Reset fields. Added new section for GPCLK Register 1. Added new section describing software control of the UDC register. Rewrote Section 9.5.2.2, “exit Idle Mode.” Added new data for the Force Stall bit.Added new output derating tables to Chapter 13. Updated GPCLK register locations table. Changed “899.78 MHz” to “900 Hz” as needed in Section 11.9. Updated section for GPCLK registers 1 and 2. Corrected baud rate divisor descriptions. Restructured Section 13.6. Corrected Figure 10-1. See Documentation Changes 41 through 97 for details.

Date	Version	Description
		Under Errata, changed the No Fix setting to Fix in the Status fields of Errata 13 — 16 and 18, established errata 17 as a No Fix, as well as adding the B4 step designator to the Affected Steppings fields for all forementioned. Also added two new errata (19 and 20) describing a failure to Reset UDC IN/OUT Data Packet Toggle Generation to DATA0/1 on Endpoints 1/2. And added errata describing the failure of the SSP bit to generate an interrupt request (21), describing the failure of the LCD Controller to operate correctly following reconfiguration events (22), and describing how a misaligned word access with a 16-bit data bus can generate incorrect data (23).
4/6/00	016	Under Documentation Changes, added notes describing use definition of register reset value, listed in documentation changes 66–95. Corrected Transaction Formats figure (30) and corrected text and figure for Packet Formats (31). Added table footnote for GPIO functions and corrected USB web site listing. Corrected Figure 11-17 figure title and text located in paragraph above Figure 11-17. Corrected bit definitions for the MCCR0 register table. Corrected text in sections 11.8.3.8 and 11.8.12. Updated Table 12-3. Under Errata, added 5 errata documenting register reads/writes following SDRAM/SDROM reads and sleep requests and SDRAM refresh issues.
1/25/00	015	Under Documentation Changes, removed documentation changes #63 — #99 (referencing the 014 specification update) from the specification update and applied them to the developer's manual; added two changes documenting a change in the exit idle mode process (Chapter 9) and a change in the register summary table (Appendix A). Under Specification Changes, added one line to Specification Changes table.
1/11/00	014	Under Documentation Changes, added 38 documentation changes removing all references to SDLC, substituting SDLC information with GPCLK information. Made four changes substituting RDN+1 with RDF+1. Changed one line in the parameters definition list in section 10.5.8 and added one footnote for Figure 10-18. Also added GPCLKR0 register to Section 11.9.3.6. Under Errata, added one errata documenting UDC work-around procedure.
12/07/99	013	Under Errata, added nine errata; under Documentation Changes, changed output signals listed in Table 13-2; changes made to Section 10.1.7, Section 10.2.1, Section 10.2.2, Section 10.2.3, Section 10.2.4, Section 10.2.5, Section 10.3, Section 10.4.6, Section 10.5.1, Section 10.5.11, Section 10.7, Section 10.7.1, and Section 10.7.2; changed Section 13.6.SDLC feature changed from an errata to a specification change.
11/18/99	012	Under Documentation Changes, changed ID code and added stepping information in section 5.2.1.
11/15/99	011	Under Errata, added two errata; under Documentation Changes, changed title of section 13.2.
11/05/99	010	Under Documentation Changes, added sentence to end of first paragraph in section 9.5.2.2.
11/03/99	009	Under Documentation Changes, changed signal description of GPIO pin 25 in table in section 9.1.2; added note to end of section 11.11.6; deleted note to bit 3 of the RCSR register in section 9.6.1.2; revised bit 0 description of USB Device Controller (UDC) CR register in section 11.8.3.8; replaced section 11.10.2.3; corrected typo in table 9-3 title; changed sentence in section 10.8.
10/08/99	008	Under Errata, added one errata; under Documentation Changes, added paragraph to section 16.6.3; added boundary-scan signals and pins table 16-2.
09/15/99	007	Under Documentation Changes, added footnote to GPIO Alternate Functions Table in Section 9.1.2.
08/19/99	006	Under Documentation Changes, changed settings for serial port 2 and serial port 4 in Table 11-6.
07/22/99	005	Under Documentation Changes, changed code example for section 6.2.3; changed last sentence of section 9.5.3; added output signals to table 13-2.
06/28/99	004	Under Documentation Changes, removed section 16.8; changed Test Unit Control Register's description of bit 10; added change to Section 9.5.7.7; changed Figure 10-6; added change to section 10.5.1; added change to section 10.1; added change to section 10.2.2.and description of MDREFR:EAPD and MDREFR:KAPD bits; added step #8 to section 10.7.1; removed the SA-1110 Tool Chains and Operating Systems Table from the brief datasheet and the developer's manual; added change to section 9.5.6; added change to section 11.13.1; added change to section 11.13.6; added change to section 10.5.5.

Date	Version	Description
05/18/99	003	Under Documentation Changes, added changes to the PPSR and PSDR register drawing graphics; added changes to the OS Timer Interrupt Enable register; added change to the Big and Little Endian DMA Transfers graphic; corrected peripheral pin assignments; changed 15 timing diagrams; changed bit 31 description in the DRAM Refresh Control Register; added changes to section 10.4.7; added changes to section 10.7.1; added changes to section 10.8.
04/19/99	002	Under Document Changes, added changes to section 1.1; section 9.1.2.1; section 3.1; section 10.2.4; and section 10.6.
03/26/99	001	This is the new specification update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® StrongARM* SA-1110 Microprocessor Developer's Manual	278240-003

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the SA-1110 microprocessor. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum s intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

No.	Steppings					Page	Status	ERRATA
	A0	B0	B1	B2	B4			
1	X	X	X	X	X	17	No Fix	Incorrect Sign-Extended Value in Register After a Read Buffer Allocate
2	X	X	X	X	X	17	No Fix	LCD Ghost Lines
3	X					17	Fixed	High Current on VDDX During Reset
4	X					17	Fixed	High Current on VDDX During Sleep
5	X					17	Fixed	LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency
6	X					18	Fixed	USB Stalls When More Than One USB Client Is Present
7	X					18	Fixed	SDRAM Auto-Power-Up Failure
8	X					18	Fixed	SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM
9	X	X				18	Fixed	DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing
10	X	X	X			19	Fixed	Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads
11	X	X	X			20	Fixed	Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset
12	X	X	X			20	Fixed	UDC Not Responding to IN Packet After Receiving an SOF Packet
13	X	X	X			20	Fixed	Corruption of Internal Register Reads/Writes Following SDRAM/SDROM Reads
14	X	X	X	X		21	Fixed	Failure on Sleep Request During Variable Latency I/O to Perform SDRAM Self-Refresh and Enter Sleep
15	X	X	X	X		21	Fixed	Failure on Sleep Request During CBR Refreshes to Perform SDRAM Self-Refresh Prior to Entering Sleep
16				X		22	Fixed	Erroneous SDRAM Power-Down-Exit and Power-Down Following Self-Refresh and Sleep Entry
17	X	X	X	X	X	23	No Fix	Corruption of Internal Register Reads/Writes Following Reads from SDRAM on 16-bit Data Busses at Full Memory Clock Frequency
18	X	X	X	X		23	Fixed	Failure on Sleep Request During SDRAM Read/Write Bursts to Precharge SDRAM Row Prior to Performing SDRAM Self-Refresh and Entering Sleep
19	X	X	X	X		23	Fixed	Failure to Reset UDC OUT Data Packet Toggle Checking to DATA0 on Endpoint 1 After a Sequence of Setting/ Clearing Force Stall Bit (UDCCS1:FST) and Clearing Sent Stall Bit (UDCCS1:SST)
20	X	X	X	X		24	Fixed	Failure to Reset UDC IN Data Packet Toggle Generation to DATA0 on Endpoint 2 After a Sequence of Setting/ Clearing Force Stall Bit (UDCCS2:FST) and Clearing Sent Stall Bit (UDCCS2:SST)
21	X	X	X	X	X	24	Eval	Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request
22	X	X	X	X	X	24	No Fix	LCD Controller Fails to Operate Correctly Following Reconfiguration

Errata (Sheet 2 of 2)

No.	Steppings					Page	Status	ERRATA
	A0	B0	B1	B2	B4			
23	X	X	X	X	X	24	No Fix	Misaligned Word Accesses with 16-Bit Data Bus May Produce Incorrect Data
24	X	X	X	X	X	25	No Fix	Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup
25	X	X	X	X	X	25	No Fix	Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count)
26	X	X	X	X	X	25	No Fix	Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller
27	X	X	X	X	X	25	No Fix	Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written
28	X	X	X	X	X	26	No Fix	Incorrect Address Decode in USB Controller

Specification Changes

No.	Steppings					Page	Status	Specification Changes
	A0	B0	B1	B2	B4			
1	X	X	X	X		30	Eval	SDLC Feature
2	X	X	X	X		30	No Fix	SDLC Feature Not Supported
3	X	X	X	X	X	30	No Fix	Modifications in SDRAM/ SMROM Data Input Hold Time

Specification Clarifications

No.	Steppings					Page	Status	Specification Clarifications
	A0	B0	B1	B2	B4			
								None for this revision of this specification update.

Documentation Changes (Sheet 1 of 3)

No.	Document Revision	Page	Status	Documentation Changes
1	278240-002	32	Doc	GPCLK Control Register 1: Section 11.9.3
2	278240-002	32	Doc	HSSP Data Register: Section 11.10.9
3	278240-002	32	Doc	Receiver Overrun Flag (ROR) (read-only, noninterruptible): Section 11.11.8.6
4	278240-002	32	Doc	External Clock Prescaler (ECP): Section 11.12.3.11
5	278240-002	32	Doc	USB Operation: Section 11.8.1

Documentation Changes (Sheet 2 of 3)

No.	Document Revision	Page	Status	Documentation Changes
6	278240-002	32	Doc	Packet Formats: Section 11.8.1.5
7	278240-002	33	Doc	UDC Data Register: Section 11.8.12
8	278240-002	34	Doc	Bit 2 Reserved: Section 11.8.3.3
9	278240-002	34	Doc	Suspend/Resume Interrupt Mask (SRM): Section 11.8.3.7
10	278240-003	19	Doc	Register 14 – Debug Support (Breakpoints): Section 5.2.13
11	278240-003	34	Doc	Data Caches (Dcaches): Section 6.2
12	278240-003	35	Doc	Writes to a Bufferable and Noncacheable Location (B=1,C=0): Section 6.3.2.2
13	278240-003	35	Doc	Unbufferable and Noncacheable Writes (B=0, C=0): Section 6.3.2.3
14	278240-003	35	Doc	Writes to a Non-Bufferable and Cacheable Location (B=0, C=1): Section 6.3.2.4
15	278240-003	35	Doc	Read Buffer (RB): Section 6.4
16	278240-003	35	Doc	Read Buffer: Section 6.4
17	278240-003	35	Doc	Read Buffer: Section 6.4
18	278240-003	36	Doc	GPIO Alternate Functions: Section 9.1.2
19	278240-003	36	Doc	Real-Time Clock: Section 9.3
20	278240-003	36	Doc	RTC Status Register (RTSR): Section 9.3.3
21	278240-003	37	Doc	Sleep Mode: Section 9.5.3
22	278240-003	37	Doc	DRAM Refresh Control Register (MDREFR): Section 10.2.2
23	278240-003	37	Doc	SMROM Configuration Register (SMCNFG): Section 10.3
24	278240-003	37	Doc	8-, 16-, and 32-Bit Data Bus Operation: Section 10.6.1
25	278240-003	37	Doc	DMA Device Address Register (DDARn): Section 11.6.1.1
26	278240-003	38	Doc	DMA Device Address Register (DDARn): Section 11.6.1.1
27	278240-003	38	Doc	DMA Control/Status Register (DCSRn): Section 11.6.1.2
28	278240-003	38	Doc	DMA Control/Status Register (DCSRn): Section 11.6.1.2
29	278240-003	38	Doc	DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4
30	278240-003	39	Doc	DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6
31	278240-003	39	Doc	Frame Buffer: Section 11.7.1.2
32	278240-003	40	Doc	Passive/Active Display Select (PAS): Section 11.7.3.7
33	278240-003	41	Doc	Passive/Active Display Select (PAS): Section 11.7.3.7
34	278240-003	41	Doc	Palette DMA Request Delay (PDD): Section 11.7.3.10

Documentation Changes (Sheet 3 of 3)

No.	Document Revision	Page	Status	Documentation Changes
35	278240-003	41	Doc	Palette DMA Request Delay (PDD): Section 11.7.3.10
36	278240-003	42	Doc	Beginning-of-Frame Line Clock Wait Count (BFW): Section 11.7.5.4
37	278240-003	42	Doc	Pixel Clock Divider: Section 11.7.6.1
38	278240-003	42	Doc	Output Enable Polarity (OEP): Section 11.7.6.7
39	278240-003	43	Doc	DMA Channel 1 Current Address Register: Section 11.7.9
40	278240-003	43	Doc	Output FIFO Underrun Lower Panel Status (OUL) (read only, maskable interrupt): Section 11.7.10
41	278240-003	43	Doc	Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12
42	278240-003	43	Doc	LCD Disable Done Flag (LDD): Section 11.7.11.12
43	278240-003	43	Doc	LCD Controller Register Locations: Section 11.7.12
44	278240-003	44	Doc	UDC Endpoint Data Register: Section 11.8.10
45	278240-003	44	Doc	UDC Data Register: Section 11.8.12
46	278240-003	44	Doc	HP-SIR * Enable (HSE): Section 11.10.4.1
47	278240-003	44	Doc	Sample Clock GPIO: Section 11.11.3.5
48	278240-003	45	Doc	UART Data Register: Section 11.11.6
49	278240-003	45	Doc	SSP Transmit and Receive FIFOs: Section 11.12.7.3
50	278240-003	45	Doc	SSP Data Register: Section 11.12.11
51	278240-003	46	Doc	PPC Pin Direction Register: Section 11.13.3
52	278240-003	46	Doc	PPC Pin State Register: Section 11.13.4
53	278240-003	46	Doc	PPC Pin Assignment Register: Section 11.13.5.2
54	278240-003	47	Doc	DC Operating Conditions: Section 12.2
55	278240-003	47	Doc	Power Supply Voltages and Currents: Section 12.3
56	278240-003	49	Doc	Timing Parameters: Section 13.6
57	278240-003	50	Doc	Timing Parameters: Section 13.6
58	278240-003	50	Doc	Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2
59	278240-003	50	Doc	Boundary-Scan Interface Signals: Section 16.7
60	278240-003	51	Doc	Boundary Scan Interface Signals: Section 16.7

Identification Information

Ordering Information

Ordering Numbers	Speed (MHz)	Voltage (V)	Package
GDS1110AC	133	1.55	PBGA
GDS1110BC	206	1.75	PBGA

Errata

1. Incorrect Sign-Extended Value in Register After a Read Buffer Allocate

Problem: After a read buffer allocate, a Load Register Signed Halfword (LDRSH) or a Load Register Signed Byte (LDRSB) will not return the correct value in the register, due to long propagation delays in the sign extend logic.

Affected Step: A0, B0, B1, B2, and B4

Workaround: Execute the command twice and the data is guaranteed to be correctly sign-extended for the second read.

Status: No Fix

2. LCD Ghost Lines

Problem: The SA-1110 LCD when driving a color passive display has diagonal ghost lines and flicker. These ghost lines are image dependent and are more evident with intensities 3 and 11.

Affected Step: A0, B0, B1, B2, and B4

Workaround: None. There is a marked improvement by setting bits 11:10 in LCD Control Register 0 (Address 0h B010 0000) to 0x8. The actual setting of bits 11:10 should be experimented with to determine the best LCD performance.

Status: No Fix

3. High Current on VDDX During Reset

Problem: The SA-1110 exhibits high VDDX current under the scenario of power-on reset and hardware reset with subsequent VDD failure.

Affected Step: A0

Workaround: Use external logic to ensure that VDD powers up with VDDX and cannot be held low when hardware reset is asserted. In a typical application, this would require that VDD be enabled if either PWR_EN = 1 or nRESET = 0.

Status: Fixed

4. High Current on VDDX During Sleep

Problem: The SA-1110 exhibits high VDDX current (2.5 mA) during sleep.

Affected Step: A0

Workaround: None identified.

Status: Fixed

5. LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency

Problem: The LCD controller fails when the frame buffer is read from SDRAM that does burst transfers at the full-memory clock frequency (one-half CPU frequency). When using other memory types, which cannot burst at full-memory clock frequency, or using SDRAM at half-memory clock frequency (one-fourth CPU frequency), the LCD controller works correctly.

Affected Step: A0

Workaround: Set up SDRAM used for the LCD frame buffer to run at half-memory clock frequency.

Status: Fixed

6. USB Stalls When More Than One USB Client Is Present

Problem: When multiple USB clients are present, the USB stalls after the master completes a transmission to another device. The USB does not respond when the master addresses it.

Affected Step: A0

Workaround: Do not allow multiple clients on the USB bus.

Status: Fixed

7. SDRAM Auto-Power-Up Failure

Problem: If the memory controller is configured to allow SDRAM auto-power-down of minimum possible duration (SDCKE 1 low for exactly one and one-half memory clocks), the subsequent auto-power-up (SDCKE 1 goes high and appropriate SDCLK 2:1 starts running) may not work correctly.

Affected Step: A0

Workaround: For SDRAM transfers, increase RAS precharge time (MDCNFG:TRP2 or MDCNFG:TRP0) to be greater than or equal to 5. This forces the first SDRAM transfer following auto-power-up to be delayed, such that SDCKE 1 can be sampled high upon a rising edge of SDCLK 2:1 prior to sampling the next ACT command.

Status: Fixed

8. SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM

Problem: Because SMROM does not require the use of the SA-1110's counter for minimum SDRAM RAS precharge time, this counter is overridden during SMROM transfers. The override logic does not consistently use upper address bits to distinguish between SDRAM and SMROM. Therefore, when like-numbered SMROM and SDRAM chip selects (for example, nCS 0 and nRAS/nSDCS 0) are enabled, the RAS precharge counter may not work for those SDRAM chip selects.

Affected Step: A0

Workaround: Avoid enabling like-numbered chip selects for SMROM and SDRAM. For example, enable SMROM only on nCS 1:0 and SDRAM only on nRAS/nSDCS 3:2.

Status: Fixed

9. DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing

Problem: Asynchronous DRAM and SDRAM refreshes are allowed to interrupt burst transfers to any static, asynchronous memory type (ROM, SRAM, VLIO, or Flash) between 32-bit transfers. This works properly when any of those memory types are configured for non-burst timings (MCSx:RTx = 0 or 1). But when ROM/Flash is configured for burst timings (MSCx:RTx = 2 or 3), burst-of-4/8 aligned addresses may erroneously use the burst access time (MCSx:RDNx) rather than the intended non-burst access time (MSCx:RDFx). This happens when the refresh request (internally generated) occurs just prior to a burst-of-4/8 unaligned address. The problem affects burst-of-4 timings on either 16-bit or 32-bit data busses, or burst-of-8 timings on 16-bit busses.

Affected Step: A0 and B0

Workaround: Use non-burst timing (MSCx:RTx = 0) for ROM/Flash.

Status: Fixed

10. Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads

Problem: If a SA-1110 hardware, software, or watchdog reset occurs while SDRAM/SMROM is executing a read command, the SA-1110 de-asserts all control pins: SDCKE 1:0, SDCLK 2:0, nCS 3:0, nRAS/ nSDCS 3:0, nSDRAS, nSDCAS, nWE, nOE, and nCAS/DQM 3:0. This correctly prevents new commands from being started. But, because SDCKE 1:0 and SDCLK 2:0 are de-asserted within a few cycles of the last read command, that read may not complete. Instead, SDRAM/SMROM may continue to drive D 31:0 during reset assertion and after reset de-assertion: until a few cycles after SDCKE 1:0 and SDCLK 2:0 are asserted again and the final read data is driven. This continuous D 31:0 drive by SDRAM/SMROM may contend with read data from other memory devices or write data from the SA-1110 itself.

Affected Step: A0, B0, and B1

Workarounds (2) for Hardware Reset: Use the following workarounds for a hardware reset:

1. Do not use hardware reset after the initial power-on hardware reset.
2. During each assertion of the SA-1110's hardware reset pin (nRESET=0), temporarily remove power from SDRAM/SMROM VDD and VDDQ pins.

Workaround for Software Reset: Prior to executing a software reset, all outstanding SDRAM and SMROM transfers must be allowed to complete and the banks must be disabled via writes to the MDCNFG and SMCNFG registers.

1. If burst reads from SMROM are not already enabled, enable them without changing the number of row address bits, CAS latency, or RAS latency.
   a. Write MDCAS00, MDCAS01, and MDCAS02 with their present number of leads 1's, but filled through the 96th bit with the 2-bit repeating pattern of "0" followed by "1" (see Section 10.2.3.2 for explanation).
   b. Force a mode register set (MRS) command by writing SMCNFG with its present value. The MRS configures the SMROMs' internal mode registers for a burst length of eight.
2. If the instruction cache is not already enabled, enable it by setting bit 12 of the coprocessor 15 control register (see Chapter 5 and Chapter 6). This causes subsequent fetches to be performed as 8-word bursts.
3. Align the store instruction which alters SMCNFG to an 8-word address boundary. Locate the store instructions that alter MDCNFG and RSRR at the subsequent two addresses. Aligning these three instructions to the start of a cache line ensures that they are fetched together and executed prior to any other SMROM read.

Workaround for Watchdog Reset: Do not use watchdog reset. The combination of watchdog interrupt and software reset may be used instead of watchdog reset.

Status: Fixed

11. Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset

Problem: After any type of reset (hardware, software, watchdog, or sleep), an SMROM mode register set (MRS) command may be followed in less than three SDCLK cycles by an unnecessary SMROM precharge all (PALL) command. According to SMROM specifications, a minimum of three cycles is required between issue of MRS and any subsequent command. Issue of the unnecessary PALL command is dependent upon the precise timing of reset within the SDCLK cycle, and upon use of MDREFR:K0DB2=1.

Affected Step: A0, B0, and B1

Workaround: Confirm that SMROM are insensitive to the issue of unnecessary PALL commands that follow MRS commands by less than three SDCLK cycles.

Status: Fixed

12. UDC Not Responding to IN Packet After Receiving an SOF Packet

Problem: The host requests data from the UDC by sending an IN packet to Endpoint 2. The UDC must respond with a NAK signal if it does not currently have any data stored in the FIFO. Sporadically, the UDC does not respond with a NAK signal after an SOF packet is received.

Affected Step: A0, B0, and B1

Workaround: Connect a USB hub between the UDC and the host system.

Status: Fixed

13. Corruption of Internal Register Reads/Writes Following SDRAM/SDROM Reads

Problem: Reads and writes, from and to internal registers other than memory controller registers, can be corrupted if they immediately follow reads from SDRAM or SMROM, shown as follows:

1. Register reads immediately following reads from SDRAM on 16-bit data busses (MDCNFG:DWIDn=1), with SDCLK running at full memory clock frequency (MDREFR:KnDB2=0), and using delayed data latching.
2. Register reads/writes immediately following reads from SDRAM or SMROM on 32-bit data busses (MDCNFG:DWIDn=0), with SDCLK running at full memory clock frequency (MDREFR:KnDB2=0), and using non-delayed data latching*.

Note: See Section 10.2.3.2 of SA-1110 Developer's Manual for a description of delayed and non-delayed data latching. Delayed data latching must be used at high core clock frequencies (e.g.- 206MHz) and non-delayed data latching must be used at low core clock frequencies (e.g.- 100MHz).

Affected Step: A0, B0, and B1

Workaround: The following workaround applies:

1. For SDRAM on 16-bit data busses, use SDCLK running at half memory clock frequency (MDREFR:KnDB2=1)
2. For SDRAM or SMROM on 32-bit data busses, use either:
   - — a higher core clock frequency and delayed data latching, or;
   - — set the SDCLK to run at half memory clock frequency (MDREFR:KnDB2=1).

Status: Fixed

14. Failure on Sleep Request During Variable Latency I/O to Perform SDRAM Self-Refresh and Enter Sleep

Problem: If the memory controller receives a request to enter sleep mode during a variable latency I/O (VLIO) transfer, the SA-1110 may fail to put SDRAM into self-refresh (with SLFRSH command) and fail to enter sleep mode. In this case the corresponding VLIO chip select (nCS[3, 4, or 5]) and byte enables (nCAS/DQM[3:0]) may remain asserted indefinitely. This problem applies to sleep entry requests initiated by either software or a power supply fault.

Affected Step: A0, B0, B1, B2, Fixed on B4

Workaround: Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

Status: Fixed

15. Failure on Sleep Request During CBR Refreshes to Perform SDRAM Self-Refresh Prior to Entering Sleep

Problem: When the memory controller receives a request to enter sleep mode during a SDRAM/DRAM CBR refresh, the SA-1110 may fail to put SDRAM into self-refresh (with SLFRSH command) prior to entering sleep mode. Sleep mode is entered. This problem applies to sleep entry requests initiated by either software or a power supply fault.

Affected Step: A0, B0, B1, B2, Fixed on B4

Workaround: Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.

2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

Status: Fixed

16. Erroneous SDRAM Power-Down-Exit and Power-Down Following Self-Refresh and Sleep Entry

Problem: If the memory controller receives a request to enter sleep mode while any SDRAM banks are enabled, and SDRAM are properly put into self-refresh (with SLFRSH command), and sleep mode is properly entered, the SA-1110 may subsequently perform erroneous SDRAM Power-Down-Exit (PWRDNX) and Power-Down (PWRDN) commands. The PWRDNX command erroneously takes SDRAM out of self-refresh. The PWRDN command returns SDRAM to a low power state, but leaves it without CBR or self-refresh throughout sleep. This problem applies to sleep entry requests initiated by either software or a power supply fault.

Affected Step: B2, Fixed on B4

Workaround: Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values.
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

Status: Fixed

17. Corruption of Internal Register Reads/Writes Following Reads from SDRAM on 16-bit Data Busses at Full Memory Clock Frequency

Problem: If a read from SDRAM on a 16-bit data bus (MDCNFG:DWID0=1 or MDCNFG:DWID2=1) running at full memory clock frequency (MDREFR:K1DB2=0 or MDREFR:K2DB2=0, respectively) is immediately followed by a core read/write from/to an internal register other than memory controller registers, the register read/write data may be corrupted.

Affected Step: A0, B0, B1, B2, B4

Workaround: Configure all SDRAM for 32-bit data busses (MDCNFG:DWID0=MDCNFG:DWID2=0) or configure all SDRAM to run at half-memory clock frequency (MDREFR:K1DB2=MDREFR:K2DB2=1).

Status: No Fix

18. Failure on Sleep Request During SDRAM Read/Write Bursts to Precharge SDRAM Row Prior to Performing SDRAM Self-Refresh and Entering Sleep

Problem: When the memory controller receives a request to enter sleep mode during a burst read or write with SDRAM, the SA-1110 may fail to precharge the currently active SDRAM row prior to putting SDRAM into self-refresh (with SLFRSH command) and entering sleep mode. Because it is an illegal SDRAM operation to attempt self-refresh while a row is active, the resulting SDRAM behavior is indeterminate. However, the SA-1110 enters sleep mode. This problem applies to sleep entry requests initiated by either software or a power supply fault.

Affected Step: A0, B0, B1, B2, Fixed on B4

Workaround: Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

Status: Fixed

19. Failure to Reset UDC OUT Data Packet Toggle Checking to DATA0 on Endpoint 1 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS1:FST) and Clearing Sent Stall Bit (UDCCS1:SST)

Problem: When the UDC receives a command from the host (for example the ClearFeature(HALT) command) which requires the endpoint to reset its data packet toggle flag to DATA0 so that when

the host sends the next data packet to Endpoint 1, the UDC should expect the data packet to be of type DATA0. The UDC fails to reset its data packet toggle flag to DATA0 (and actually leaves it in its current state) after executing the proper sequence of setting the Force Stall Bit (UDCCS1:FST), clearing the Force Stall Bit, and then clearing the Sent Stall Bit (UDCCS1:SST).

Affected Step: A0, B0, B1, B2, Fixed on B4

Workaround: None.

Status: Fixed

20. Failure to Reset UDC IN Data Packet Toggle Generation to DATA0 on Endpoint 2 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS2:FST) and Clearing Sent Stall Bit (UDCCS2:SST)

Problem: When the UDC receives a command from the host (for example the ClearFeature(HALT) command), it requires the endpoint to reset its data packet toggle flag to DATA0. Therefore, the next data packet sent from Endpoint 2 to the host, must be of type DATA0. The UDC fails to reset its data packet toggle flag to DATA0 (and actually sets it to DATA1) after executing the proper sequence of setting the Force Stall Bit (UDCCS2:FST), clearing the Force Stall Bit, and then clearing the Sent Stall Bit (UDCCS2:SST).

Affected Step: A0, B0, B1, Fixed on B4

Workaround: None.

Status: Fixed

21. Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request

Problem: Non-maskable interrupt is not generated when the Receiver Overrun (ROR) status bit is set in the SSP status register. In addition, the ROR bit is set when data is placed in the ninth entry of the 12-entry receive FIFO.

Affected Step: A0, B0, B1, B2, B4

Workaround: The SSP Status Register ROR bit can be polled to determine if a receiver overrun has occurred. Software must detect if there was missing data due to an overrun. This can be accomplished by methods such as counting data packets, or adding a CRC packet, or implementing a checksum algorithm.

Status: Eval

22. LCD Controller Fails to Operate Correctly Following Reconfiguration

Problem: If the LCD Controller is configured and enabled following a reset event, and is subsequently disabled and reconfigured for different display characteristics, unpredictable behavior may result when the LCD controller is reenabled.

Affected Step: A0, B0, B1, B2, B4

Workaround: Configure and enable the LCD Controller only one time after a reset event.

Status: No Fix

23. Misaligned Word Accesses with 16-Bit Data Bus May Produce Incorrect Data

Problem: If a misaligned word (32-bit) access is attempted with the data bus configured for 16-bit operation, address bus bit 1 does not toggle as required to support the access. Additionally, the data bytes being transferred may be erroneously swapped.

Affected Step: A0, B0, B1, B2, B4

Workaround: Do not configure SA-1110 for operation with 16-bit data bus.

Status: No Fix

24. Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup

Problem: The software sleep status bit (PSSR:SSS) may inadvertently be set after sleep wakeup, even though the part was not put into sleep mode by setting the force sleep (PMCR:SF) bit.

Affected Step: A0, B0, B1, B2, B4

Workaround: Use a bit in the PWER registers as a substitute for the PSSR:SSS bit. You must choose a bit in PWER that corresponds to a bit set as an output in the GPDR in the application system. For example, if you use bit 5 of PWER as a flag to indicate whether the part went to sleep via software or hardware, then define PWER[5]=1 to mean that the part went to sleep via software. If you boot from a hard reset (RCSR:HWR = 1), ignore PWER[5]. When you are going to sleep via software, then the last thing to do before setting PMCR:SF bit, is to set PWER[5]=1. When the part wakes up, if RCSR:SMR bit is set (sleep mode reset), then read the PWER[5] bit to see if it was in sleep due to software (= 1) or not (= 0). This bit in the PWER register is now a substitute for the PSSR:SSS bit.

Status: No Fix

25. Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count)

Problem: When the SA1110's LCCR2: EFW (End of Frame Line Clock Wait Count) is **not** zero, LCCR1: ELW (End of Line Pixel Clock Wait Count) is mistakenly loaded into the End of Frame Wait Counter.

Affected Step: A0, B0, B1, B2, B4

Workaround: Always program LCCR2: EFW to zero. Use LCCR2: BFW (Beginning of Frame Line Clock Wait Count) to delay the next frame.

Status: Eval

26. Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller

Problem: Between two successive accesses to the SA1110's PCMCIA Interface, the Bus Arbiter might not recognize a pending, highest-priority request from the LCD Controller and, therefore, the LCD Controller is not granted bus access as it should be.

Affected Step: A0, B0, B1, B2, B4

Workaround: To unlock the Bus Arbiter, follow the PCMCIA access with a "dummy" store-to or load-from uncached/unbuffered memory space.

Status: Eval

27. Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written

Problem: A read back of the RTTR or RCNR register immediately after a load of the RTTR or RCNR register does not read back the loaded value. This is caused by a long propagation delay through the read back logic.

Affected Step: A0, B0, B1, B2, B4

Workaround: Execute some other instruction between the register load and the register read back.

Status: No fix.

28. Incorrect Address Decode in USB Controller

Problem: Generally, SA-1110 USB functionality is limited to a USB bus with a maximum of two USB devices, this bus would include the SA-1110 USB device. Alternately, there may be three or more USB devices on the bus if the SA-1110 USB device is assigned address 0x4. The following paragraphs explain in detail this environment.

The SA-1110 USB controller may incorrectly decode an address on the bus causing one of these problems:

1. USB Port responds to the wrong address
2. USB Port accepts data to the wrong address
3. Port may freeze because of various address and endpoint combinations on the bus

SA-1110 USB Port Responds to the Wrong Address

There are two conditions where the SA-1110 USB Port responds to an incorrect address:

1. Three or more devices and hubs in a system when the SA-1110 device is assigned to address 0x4
2. Three or more devices in a system when the SA-1110 device is assigned to an address other than 0x4

The SA-1110 USB functions properly when it is the only device in a system or with only one other device. In this case the SA-1110 USB device did not fail in laboratory tests. The following paragraphs explain what happens when an SA-1110 USB device is in a system with two or more other USB devices.

If an SA-1110 device is assigned to address 0x4, the error was not duplicated in the lab. However, if these conditions occur:

- An installed SA-1110 USB device is disconnected from your system,
- Another USB device is connected, and
- The SA-1110 USB device is re-connected,

Then the SA-1110 USB device will fail because it is no longer assigned to address 0x4.

After the SA-1110 USB device is disconnected, the host frees-up address 0x4 and it is assigned to the next device plugged into the system. If the SA-1110 device is simply disconnected and re-connected without disconnecting or connecting any other USB devices, the host again assigns address 0x4 to the SA-1110 device and the error does not occur.

If the SA-1110 USB device is not assigned to address 0x4, an error will occur. If the SA-1110 USB device is connected after address 0x4 has been assigned to another USB device, the failure occurs immediately. If the SA-1110 USB device is connected before address 0x4 has been assigned, no failure occurs unless the SA-1110 USB device is disconnected and re-connected. Hence, the major problem is when another device is assigned to address 0x4 in a system before the SA-1110 device is assigned an address.

Other address and endpoint combinations cause the SA-1110 USB device to incorrectly respond, thereby causing contention on the USB Bus. The table below shows some of the more likely combinations that cause an incorrect response. If the SA-1110 USB device is assigned to the address in the "SA-1110 Device" column and there is an access to the address and endpoint combination shown in the "Other Devices" column, the SA-1110 USB device incorrectly responds.

Other SA-1110 Erroneous Response Cases

Other Devices			SA-1110 Device	
Address	**Endpoint**	**crc**	**address**	**endpoint**
0x0F	0x0	0x03	0x00	0x1
0x04	0x0	0x05	0x00	0x2
0x0B	0x0	0x04	0x00	0x2
0x02	0x1	0x03	0x08	0x1
0x0D	0x1	0x02	0x08	0x1
0x06	0x1	0x04	0x08	0x2
0x09	0x1	0x05	0x08	0x2

USB Port Accepts Data to the Wrong Address

A few cases exist where the SA-1110 USB device incorrectly decodes an address and incorrectly accepts data that was intended for another USB device. This error only occurs during an OUT transaction, and could cause data corruption to the SA-1110 USB device. All of these cases occur when a particular address, endpoint, and CRC combination is incorrectly compared (by the SA-1110 USB) to the address assigned to the SA-1110 USB device and endpoint 0x1. The table below shows some of the address, endpoint, and CRC combinations that cause this error.

Some Addresses that cause the SA-1110 to Accept Bad Data

Other Devices			SA-1110 Device	
Address	**Endpoint**	**crc**	**address**	**endpoint**
0x02	0x1	0x03	0x08	0x1
0x0D	0x1	0x02	0x08	0x1
0x0F	0x0	0x03	0x00	0x1

The first two rows in the table above occur only with 16 or fewer devices in a system and where the SA-1110 USB device is assigned to address 0x8 and an OUT transaction occurs to address 0x2 or address 0xD at endpoint 0x1. The third row in the table above occurs only if 15 or more devices and hubs are in a system and where an OUT transaction occurs to address 0xF at endpoint 0 while the SA-1110 USB device has just been reset and does not yet have an address assigned. While these cases are rare and depend on the number of devices in the system as well as the type of transaction and the address being accessed, the error occurs if these conditions are met.

The SA-1110 USB Controller Freezes and Recovers

As with condition 1 and 2, condition 2 occurs when the SA-1110 USB device incorrectly decodes an address. In this case, however, the decode does not include an endpoint for the SA-1110 USB device. When this happens the SA-1110 USB device does not try to respond, rather it freezes while

waiting for more data to decode for a valid endpoint. This error, while frequently occurring, recovers as soon as a valid address, endpoint, and CRC combination are seen on the bus. The table below shows all of the combinations that cause the SA-1110 USB device to freeze when as many as 16 USB devices are in a system.

Addresses That Cause the SA-1110 USB Controller to Freeze

Other Devices			SA-1110 Device
address	**endpoint**	**crc**	**address**
0x04	0x2	0x00	0x00
0x09	0x3	0x00	0x00
0x03	0x4	0x00	0x01
0x0E	0x5	0x00	0x01
0x00	0x9	0x00	0x02
0x0D	0x8	0x00	0x02
0x07	0xF	0x00	0x03
0x0A	0xE	0x00	0x03
0x06	0x3	0x01	0x04
0x0B	0x2	0x01	0x04
0x01	0x5	0x01	0x05
0x0C	0x4	0x01	0x05
0x02	0x8	0x01	0x06
0x0F	0x9	0x01	0x06
0x05	0xE	0x01	0x07
0x08	0xF	0x01	0x07
0x00	0x0	0x02	0x08
0x0D	0x1	0x02	0x08
0x07	0x6	0x02	0x09
0x0A	0x7	0x02	0x09
0x04	0xB	0x02	0x0A
0x09	0xA	0x02	0x0A
0x03	0xD	0x02	0x0B
0x0E	0xC	0x02	0x0B
0x02	0x1	0x03	0x0C
0x0F	0x0	0x03	0x0C
0x05	0x7	0x03	0x0D
0x08	0x6	0x03	0x0D
0x06	0xA	0x03	0x0E
0x0B	0xB	0x03	0x0E
0x01	0xC	0x03	0x0F
0x0C	0xD	0x03	0x0F

While laboratory tests have shown this error will recover, it has not been fully characterized. It is suspected that either an SOF or EOP for another USB device causes the SA-1110 USB device to recover. However, in some cases an ACK to another address also helped the SA-1110 USB device recover. Since a wide variety of circumstances caused the SA-1110 USB device to easily recover, thorough testing was not done to find all recovery cases.

Affected Step: A0, B0, B1, B2, and B4

Workaround: None

Status: Eval

Specification Changes

1. SDLC Feature

The SDLC feature is not available in this release of the product.

2. SDLC Feature Not Supported

Effective January 2000, the SDLC feature is not supported by the SA-1110 device.

3. Modifications in SDRAM/SMROM Data Input Hold Time

Table 13-3 of the *Intel StrongARM SA-1110 Microprocessor Developer's Manual* and its underlying Note 1 have been changed. Specifically, the Tsdih guidelines for 133 MHz SA-1110 microprocessors using SDRAM or SMROM at 66 MHz have changed. Also, the Tsdih guidelines for 206 MHz SA-1110 microprocessors using SDRAM or SMROM at frequencies less than 103 MHz have also been changed.

Most significantly, for 133 MHz SA-1110 microprocessors with a 66 MHz SDRAM/SMROM clock, the specified read data latching mode has changed from delayed to non-delayed. The MDCASxx registers need to be programmed accordingly. Also, the Table 13-3 Note 2 technique of serpentine SDCLK routing delay must not be used with 133 MHz SA-1110 microprocessors.

For 206 MHz SA-1110 microprocessors using an SDRAM/SMROM clock frequency of less than 103 MHz, there are four options:

- Confirm that the system design satisfies the new Tsdih guidelines (see Table 13-3).
- Carefully use the Table 13-3 Note 2 technique to adjust the system design so that it satisfies the new Tsdih guidelines.
- Set MDREFR:KnDB2=1 to divide the SDRAM/SMROM clock frequency by two and automatically use non-delayed read data latching.
- Change the CPU frequency such that the new Tsdih guidelines are satisfied at the non-divided SDRAM/SMROM clock frequency.

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. GPCLK Control Register 1: Section 11.9.3

Add the following Note just under the second paragraph of this subsection:

Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

2. HSSP Data Register: Section 11.10.9

Add the following Note at the end of the fourth paragraph of this subsection:

Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

3. Receiver Overrun Flag (ROR) (read-only, noninterruptible): Section 11.11.8.6

Add the following Note just under the second paragraph of this subsection:

Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

4. External Clock Prescaler (ECP): Section 11.12.3.11

Add the following Note just under the second paragraph of this subsection:

Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

Replace table header with the following:

“MCP Control Register 0: MCCR0”

In the table, Bits 16–23 are replicated twice; once on page 11-138 and on page 11-139. Delete page 11-139.

5. USB Operation: Section 11.8.1

Change footnote on this page to:

“Access the most recent revision of the Universal Serial Bus Specification via the World Wide Web at http://www.usb.org/ .”

6. Packet Formats: Section 11.8.1.5

Replace the paragraph just above Figure 11-17 with the following:

“A start–of–frame (SOF) is a special type of token packet that is issued by the host once every 1 ms. The SOF packets consist of a sync, a PID, a frame number (which is incremented after each frame is transmitted), and a CRC5 field, as shown in Figure 11-17. Even though the UDC on the SA-1110 does not make use of the frame number field, the presence of the SOF packets every 1ms prevents the UDC from entering suspend mode.”

Replace Figure 11-17 figure title with the following:

“SOF Token Packet Format”

Replace the paragraph just above Figure 11-18 with the following:

“Data packets follow token packets, and are used to transmit data between the host and UDC. The two types of data packets as specified by the PID are: DATA0 and DATA1. These two types provide a mechanism to guarantee data sequence synchronization between the transmitter and receiver across multiple transactions. During the handshake phase, both communicate and agree which data token type to transmit first. For each subsequent packet transmitted, the data packet type is toggled (DATA0, DATA1, DATA0, and so on). A data packet consists of a sync, a PID, from 0 to 256 bytes of data, and a CRC16 field, as shown in the Figure 11-18.”

Replace Figure 11-18 with the following:

8 bits	8 bits	0–256 bytes	16 bits
Sync	PID	Data	CRC16

7. UDC Data Register: Section 11.8.12

Replace the text for this section with the following:

“The UDC data register (UDCDR) is an 8–bit register corresponding to both the top and bottom entries of the transmit and receive FIFOs, respectively. The UDC receive logic places data into the top of the receive FIFO. The data is transferred down the FIFO to the lowest location that is empty. When the UDCDR is read, the bottom entry of the 8-bit receive FIFO is accessed. After the read, the bottom FIFO entry is invalidated. This causes all FIFO data to automatically transfer down one location.

When the UDCDR is written, the topmost 8-bit transmit FIFO entry is accessed. After a write, the data is automatically transferred down the FIFO to the lowest available location. The UDC transmit logic:

- acquires 8-bit data values from the bottom of the transmit FIFO, one at a time;
- places the data into a serial shifter;
- and transmits this data out via the UDC pins.

Each time a data value is taken from the bottom FIFO entry, the location is invalidated. This causes all data in the FIFO to automatically transfer down one location.

The following table shows the location of the top and bottom of the transmit and receive FIFOs in the UDC data register. Both FIFOs are cleared when the SA-1110 is reset, when zero is written to the UDE, and when the UDD is written to one. After either of these actions takes place, prime the transmit FIFO by writing up to sixteen 8-bit values to the UDCDR before enabling the UDC.”

Replace the address header at the top of the table with the following:

“0h80000028”

8. Bit 2 Reserved: Section 11.8.3.3

Change this entire section (including title) to the following:

"Section 11.8.3.3 Resume Interrupt Mask (RESIM)

The resume interrupt mask (RESIM) bit masks or enables the resume interrupt request.

- When RESIM=1, the interrupt is masked. The RESIR bit in the Status/Interrupt Register cannot be set.
- When RESIM=0, the interrupt is enabled. Whenever a resume condition occurs, the RESIR bit is set.

A resume condition occurs after a suspend condition has occurred. A write of a 1 and then a write of a 0 to this bit resets the internal suspend state machine in order that future resume conditions are recognized.

Note: Programming RESIM=1 does not affect the current state of RESIR. It serves only to block future zero–to–one transitions of RESIR.

9. Suspend/Resume Interrupt Mask (SRM): Section 11.8.3.7

Change this entire section (including title) to the following:

"Section 11.8.3.7 Suspend Interrupt Mask (SUSIM)

The suspend interrupt mask (SUSIM) bit masks or enables the suspend interrupt request.

- When SUSIM=1, the interrupt is masked, and the SUSIR bit in the Status/Interrupt Register cannot be set.
- When SUSIM=0, the interrupt is enabled, and whenever a suspend condition occurs, the SUSIR bit is set.

Note: Programming SUSM=1 does not affect the current state of SUSIR. It serves only to block future zero–to–one transitions of SUSIR."

10. Register 14 – Debug Support (Breakpoints): Section 5.2.13

Added a paragraph immediately preceding the Data Breakpoint Control Register table. The paragraph now appears as follows:

The DBAR, DBVR, DBMR and DBCR registers are Read/Write registers. The IBCR is a Write-Only register.

11. Data Caches (Dcaches): Section 6.2

Removed the second to last sentence in the first paragraph, which was: "Replacements in the minicache use the same round-robin pointer mechanism as in the main data cache." Changed the last sentence in the first paragraph. The first paragraph now appears as follows:

The SA-1110 contains two logically separate data caches: the main data cache and the mini data cache (or minicache). The main data cache, an 8 Kbyte write-back Dcache, has 256 lines of 32 bytes (8words) in a 32-way set-associative organization. It is intended for use during most data accesses. This cache allocates on loads to spaces marked B=1 and C=1. Replacements in the main data cache are selected according to a set of round-robin pointers. At reset, the pointer in each block of the Dcache points to way zero of each 32-way block. As lines are allocated, the pointers

are incremented to the next way of the set. After way 31 is allocated, the next line fill replaces (and copies back to memory, if dirty) the data in way zero. The minicache is a 512-byte write-back cache. It has 16 lines of 32 bytes (8 words) in a two-way set-associative organization and provides an alternate caching structure for dealing with large data structures that could thrash the main data cache. This cache allocates on loads to spaces marked B=0 and C=1. The minicache is only two-way set-associative and its replacement algorithm is a simple least-recently-used (LRU) mechanism.

12. Writes to a Bufferable and Noncacheable Location (B=1,C=0): Section 6.3.2.2

The second sentence has been changed and a fourth sentence has been added. This section now appears as follows:

If the write buffer is enabled and the processor performs a write to a bufferable but noncacheable location and misses in the Dcaches, the data is placed in the write buffer and the CPU continues execution. The write buffer performs the external write sometime later. Store multiples are **not** merged in the write buffer when B = 1, C = 0.

13. Unbufferable and Noncacheable Writes (B=0, C=0): Section 6.3.2.3

Renamed this section title from: Unbufferable Writes (B=0).

14. Writes to a Non-Bufferable and Cacheable Location (B=0, C=1): Section 6.3.2.4

Section 6.3.2.4 added. The paragraph for this section appears as follows:

When store multiples occur to a page that is cacheable but not buffereable (B=0,C=1), the write data will be merged into the write buffer and burst writes will occur to memory.

15. Read Buffer (RB): Section 6.4

Changed the third sentence in the first paragraph. The paragraph now appears as follows:

The SA-1110 contains a software-programmable read buffer that can increase the performance of critical loop code by prefetching data. The RB enables the preallocation of read-only data into one of four 32-byte buffers without stalling the pipe. For subsequent loads that hit in the RB, data is sourced from the buffer instead of the Dcaches at a rate of 1 word per core clock (as long as the load address hits in the TLB of the DMMU). Also, because the programmer specifies which entry of the RB is used, critical data can be “locked” in to eliminate bus latency.

16. Read Buffer: Section 6.4

The third sentence in the fifth paragraph has been changed and now appears as follows:

It is possible for a portion of a cache block at a given virtual address to be contained in one RB entry while another portion of the same block is contained in another RB entry.

17. Read Buffer: Section 6.4

Add the following note to the end of this section:

Note: The Write Buffer must be drained before attempting to load the Read Buffer.

18. GPIO Alternate Functions: Section 9.1.2

In row GPIO 19 in the Unit column, modify the contents to be Serial Port 4: SSP. This row now appears as follows:

Pin	Alternate Function	Direction	Unit	Signal Description
GP 19	SSP_CLK	Input	Serial port **4**:SSP	Sample clock input

19. Real-Time Clock: Section 9.3

In the second paragraph, modified the fourth sentence. The paragraph now appears as follows:

In addition to the counter [RTC counter register (RCNR)], the RTC incorporates a 32-bit alarm register (RTAR). The RTAR may be programmed with a value to be compared against the counter. On each rising edge of the 1-Hz clock, the counter is incremented and then compared to the RTAR. If the values match and the alarm interrupt is enabled, then a status bit is set. This status bit is also routed to the interrupt controller and may be programmed to generate a CPU interrupt.

In the second paragraph, modified the first sentence. The paragraph now appears as follows:

Another status bit is available that is set whenever the 1 Hz clock interrupt occurs. Each status bit may be cleared by writing a one to the status register in the desired bit position. The 1-Hz clock is generated by dividing down the 32.768-kHz crystal oscillator output. This divider logic is programmable to allow the user to “trim” the counter to adjust for inherent inaccuracies in the crystal frequency. This trimming mechanism permits the user to adjust the RTC to an accuracy of +/- 5 seconds per month. The trimming procedure is described later in this section.

Added the following note.

Note: The 32.768 kHz crystal may take 2-10 seconds to stabilize after a hardware reset. The Power Manager Oscillator Status Register (0x9002001c) bit Oscillator OK (bit 0) is set when the 32.768 kHz clock has stabilized after a hardware reset.

20. RTC Status Register (RTSR): Section 9.3.3

Changed AL and HZ bit descriptions.

0h 9001 0010 **RTSR** **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												**HZE**	**ALE**	**HZ**	**AL**
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?

Bits	Name	Description
0	AL	RTC alarm interrupt detected. 0 – No alarm interrupt has been detected. 1 – An alarm interrupt has been detected (RTNR matched RTAR).
1	HZ	1-Hz rising-edge interrupt detected. 0 – No rising-edge interrupt has been detected. 1 – A rising-edge interrupt has been detected.

21. Sleep Mode: Section 9.5.3

The second sentence has been changed and now appears as follows:

In the transition from run or idle to sleep mode, the SA-1110 performs an orderly shutdown of on-chip activity, applies an internal reset to the processor, and then negates the PWR_EN pin indicating to the external system that the VDDI (1.5-V supply) can be driven to zero volts.

22. DRAM Refresh Control Register (MDREFR): Section 10.2.2

Added the following sentence to the end of the first paragraph:

Writes to reserved bits are ignored and reads return zeros.

23. SMROM Configuration Register (SMCNFG): Section 10.3

Added the following sentence to the end of the first paragraph:

Writes to reserved bits are ignored and reads return zeros.

24. 8-, 16-, and 32-Bit Data Bus Operation: Section 10.6.1

This section title has been changed to “8-, 16-, and 32-Bit Data Bus Operation” (was previously “32-Bit Data Bus Operation”).

25. DMA Device Address Register (DDARn): Section 11.6.1.1

Changed the reset values for bits 31:26 from 0 to “?”.

DDARn **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA 31	DA 30	DA 29	DA 28	DA 27	DA 26	DA 25	DA 24	DA 23	DA 22	DA 21	DA 20	DA 19	DA 18	DA 17	DA 16	DA 15	DA 14	DA 13	DA 12	DA 11	DA 10	DA 9	DA 8	DS 3	DS 2	DS 1	DS 0	DW	BS	E	RW
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

(Sheet ? of ?)

26. DMA Device Address Register (DDARn): Section 11.6.1.1

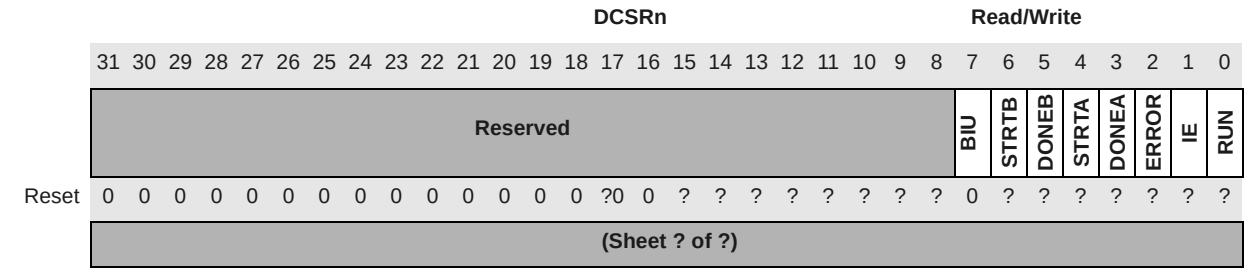
The values for the BS column for Serial Port 4 in Table 11-6 have been changed and now appear corrected in the table. The value for the DS 3:0 column for MCP receive (audio) in Table 11-6 has been changed and is now corrected in the table.

Table 11-6 Valid Settings for the DDARn Register

Unit Name	Function	Device Address	DDAR Fields					
			DA 31:8	DS 3:0	DW	BS	E	RW
Serial port 4	MCP transmit (audio)	0x 8006 0008	0x818002	1010	1	**0**	0/1	0
	MCP receive (audio)	0x 8006 0008	0x818002	1011	1	**0**	0/1	1
	MCP transmit (telecom)	0x 8006 000C	0x818003	1100	1	**0**	0/1	0
	MCP receive (telecom)	0x 8006 000C	0x818003	1101	1	**0**	0/1	1
	SSP transmit	0x 8007 006C	0x81C01B	1110	1	**0**	0/1	0
	SSP receive	0x 8007 006C	0x81C01B	1111	1	**0**	0/1	1

27. DMA Control/Status Register (DCSRn): Section 11.6.1.2

Changed DMA control/status register bit-0 from RUNE to RUN and changed the reset value of BIU (Bit 7) from "?" to "0".



28. DMA Control/Status Register (DCSRn): Section 11.6.1.2

Add this note to the end of Section 11.6.1.2:

Note: Never clear the BIU bit by writing to DCSR_Clear because this leaves the DMA status register bit BIU (viewed via DCSR_Read) in an undefined state and can only be recovered by reset. Always write 0x7F to DCSR_Clear to clear DCSRn before programming the DMA channel.

29. DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4

Changed the DMA buffer A transfer count register description in the table from "transfer count is 8 Kbyte." to "transfer count is 8191 bytes."

Bits	Name	Description
12..0	TCA 12..0	Transfer count (buffer A). This field is a 13-bit value and contains the current transfer count (in bytes) for the transfer to or from buffer A. The maximum value programmed via this transfer count is 8191 bytes.
31..13	—	Reserved. These bits are reserved and read as zeros. Writes to this field have no effect.

30. DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6

Change the DMA buffer B transfer count register description in the table from "transfer count is 8 Kbyte." to "transfer count is 8191 bytes."

Bits	Name	Description
12..0	TCB 12..0	Transfer count (buffer B). This field is a 13-bit value and contains the current transfer count (in bytes) for the transfer to or from buffer B. The maximum value programmed via this transfer count is 8191 bytes.
31..13	—	Reserved. These bits are reserved and read as zeros. Writes to this field have no effect.

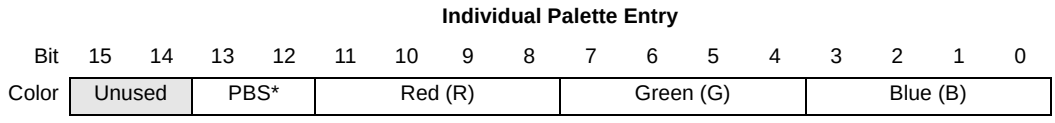
31. Frame Buffer: Section 11.7.1.2

In the first table in this section, “0x - 4 bits per pixel” has been changed to “00 - 4 bits per pixel.” The first table in this section now appears as follows:

Bit	Name	Description
13..12	PBS	Pixel bit size. 0**0** – 4 bits per pixel, 16-entry palette, 32 bytes of palette buffer transferred each frame to palette. 01 – 8 bits per pixel, 256-entry palette, 512 bytes of palette buffer transferred each frame to palette. 10 – 12 bits per pixel in passive mode (PAS=0), 16 bits per pixel in active mode (PAS=1). Palette unused, however, 32 bytes of “dummy” palette data is transferred each frame to palette. Palette data must be zero-filled. 11 – Reserved. **Note**: Two 4-bit pixels are packed into each byte, and 12-bit pixels are right justified on half-word boundaries.

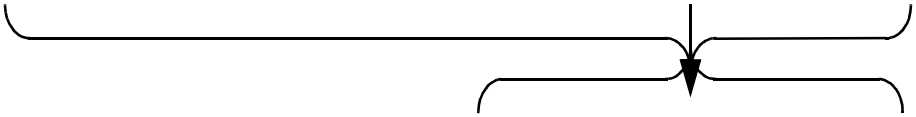
Also in this section, changed 254 to 255 in Figure 11-3. The figure now appears as follows:

Figure 11-3. Palette Buffer Format



Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mono	Unused		PBS*		Unused								Monochrome (M)			

*__Note:__ Pixel bit size (PBS) is contained only within the first palette entry (palette entry 0).



16- or 256-Entry Palette Buffer

Bit	31	16	15	0
Base + 0x0	Palette entry 1		Palette entry 0	
Base + 0x4	Palette entry 3		Palette entry 2	
.				
.				
Base + 0x1C	Palette entry 15		Palette entry 14	
Base + 0x20	Palette entry 17		Palette entry 16	
.				
.				
.				
Base + 0x1FC	Palette entry 255		Palette entry 254	
Base + 0x200	**Start of Encoded Pixel Data**			

Note: Entries 16 through **255** do not exist for 4-, 12- and 16-bit/pixel modes.

Little Endian Palette Entry Ordering

Bit	31	16	15	0
Base + 0x0	Palette Entry 0		Palette Entry 1	
Base + 0x4	Palette Entry 2		Palette Entry 3	
.				
.				

Big Endian Palette Entry Ordering

32. Passive/Active Display Select (PAS): Section 11.7.3.7

In the third paragraph, the fifth and sixth sentences have been updated with a single sentence so that users can clear GAFR 6:9 in 4- or 8-bit /pixel mode.

Figure 11-9 shows which bits within each frame buffer entry (for 16-bit/pixel mode) and which bits within a selected palette entry (for 4- and 8-bit/pixel mode) are sent to the individual LCD data pins. In active mode, GPIO pins 2..9 are also used. Note that the user must configure GPIO pins 2..5 as outputs (for 4- and 8-bit/pixel mode), and GPIO pins 2..9 as outputs (for 16-bit/pixel mode) by setting the appropriate bits within the GPIO pin direction register (GPDR) and GPIO alternate function register (GAFR). See the General-Purpose I/O section for configuration information. When in 4- or 8-bits/pixel mode, the user should clear GAFR 6:9 to disable the LCD alternate

function and, thereby, prevent unpredictable data from being driven onto GPIO 6:9. In general, the user may clear any number of GAFR bits 2..9, to allow the GPIO unit to assume control of unused GPIO pins for normal digital I/O depending on the required number of data pins

33. Passive/Active Display Select (PAS): Section 11.7.3.7

Removed the first sentence in Footnote 1, which was:

GPIO pins 6..0 are grounded by the LCD in this mode.

Also removed Vss from above GPIO9, GPIO8, GPIO7, and GPIO6 in Figure 11-9. Figure 11-9 and Footnote 1 appear as follows:

Figure 11-9. Frame Buffer/Palette Bits Output to LCD Data Pins in Active Mode

16-Bit/Pixel Mode
Frame Buffer Entry

	R 5	R 4	R	R 2	R	R	G4	G 3	G 2	G1	G 0	B 4	B 3	B 2	B 1	B 0
	R 4	R 3	R	R 1	R 0	G 5	G4	G 3	G 2	G1	G 0	B 4	B 3	B 2	B 1	B 0
	R 4	R 3	R 2	R 1	R 0	G 4	G3	G 2	G 1	G 0	B 5	B 4	B 3	B 2	B 1	B 0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Pin	GPIO 9	GPIO 8	GPIO 7	GPIO 6	GPIO 5	GPIO 4	GPIO 3	GPIO 2	LDD 7	LDD 6	LDD 5	LDD 4	LDD 3	LDD 2	LDD 1	LDD 0

4- or 8-Bit/Pixel Mode
Selected Palette Entry

					R 3	R 2	R 1	R 0	G 3	G 2	G 1	G 0	B 3	B	B	B 0
Bit					11	10	9	8	7	6	5	4	3	2	1	0
Data Pin	GPIO 9	GPIO 8	GPIO 7	GPIO 6	GPIO 5	GPIO 4	GPIO 3	GPIO 2	LDD 7	LDD 6	LDD 5	LDD 4	LDD 3	LDD 2	LDD 1	LDD 0

[1]However, if GAFR bit 6..9 are cleared within the system control module, these pins can be used as normal GPIO pins.

34. Palette DMA Request Delay (PDD): Section 11.7.3.10

Removed last sentence from the third paragraph, which was “Note that writes to reserved bits are ignored and reads returns zeros.” The third paragraph now appears as follows:

The following table shows the location of all 10 bit-fields located in LCD control register 0 (LCCR0). The user must program the control bits within all other control registers before setting LEN=1 (a word write can be used to configure LCCR0 while setting LEN after all other control registers have been programmed), and also must disable the LCD controller when changing the state of any control bit within the LCD controller.

35. Palette DMA Request Delay (PDD): Section 11.7.3.10

Changed description of Bits 11:10 from "Reserved" to “LCCR0” and added bit description.

11..10	LCCR0	LCD Control Register 0 Bits: 11 10 0 0 – Values after reset 0 1 – Vertical slant correction pattern 0, modulation rate is 4/15 and 11/15 1 0 – Vertical slant correction pattern 1, modulation rate is 4/15 and 11/15 1 1 – Reserved

36. Beginning-of-Frame Line Clock Wait Count (BFW): Section 11.7.5.4

Changed the second sentence in the second paragraph for the description of bits 15:10 in the LCD Control Register 2. The bit description now appears as follows:

0h B010 0024 LCCR2: LCD Control Register 2 Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BFW								EFW								VSW						LPP									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15..10	VSW	Vertical sync pulse width. In active mode (PAS=1), value (from 1 to 64). Used to specify number of line clock periods to pulse the L_FCLK pin at the end of each frame after the end-of-frame wait (EFW) period elapses. Frame clock used as VSYNC signal in active mode. In passive mode (PAS=0), value (from 1 to 64). Used to specify number of extra line clock periods to insert after the end-of-frame. Note that the width of L_FCLK is not affected by VSW in passive mode and that line clock does transition during the insertion of the extra line clock waitstate periods. Also note that both EFW and BFW should be set to zero in passive mode. VSYNC width = (VSW+1).

37. Pixel Clock Divider: Section 11.7.6.1

In the second sentence in this section, changed the PCD value from 225 to 255. The second sentence now appears as follows:

PCD can be any value from 1 to 2**5**5 (0 is illegal) and is used to generate a range of pixel clock frequencies from CCLK/6 to CCLK/514 (where CCLK is the programmed frequency of the CPU clock).

38. Output Enable Polarity (OEP): Section 11.7.6.7

In the table describing LCCR3, the value in the description for the PCD row was modified, as indicated in bold. The PCD row now appears as follows:

0h B010 0028 LCCR3: LCD Control Register 3 Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								OEP	PCP	HSP	VSP	API				ACB								PCD							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7..0	PCD	Pixel clock divisor. Value (from **1** to 255). Used to specify the frequency of the pixel clock based on the CPU clock (CCLK) frequency. Pixel clock frequency can range from CCLK/6 to CCLK/514. Pixel Clock Frequency = CCLK/2(PCD+2). Note that PCD must be programmed with a value of 1 or greater (PCD = 8'h00 is illegal).

39. DMA Channel 1 Current Address Register: Section 11.7.9

Changed the title bar for the register description from Read/Write to Read Only. The title bar appears as follows:

0h B010 0014	DCAR1: DMA Channel 1 Current Address Register	Read Only

40. Output FIFO Underrun Lower Panel Status (OUL) (read only, maskable interrupt): Section 11.7.10

Changed title from read/write to read only.

41. Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12

A note has been added after the second paragraph indicating that when the interrupt to the LCD Controller is first unmasked by programming ICMR: 12 to one, an unwanted interrupt is immediately generated. The note appears as follows:

Note: When the interrupt to the LCD Controller is first unmasked by programming ICMR: 12 to one, an unwanted interrupt is immediately generated. To avoid this interrupt, LCSR: LDD (LCD disable done flag) should be cleared (by writing a one to it) before unmasking ICMR: 12.

42. LCD Disable Done Flag (LDD): Section 11.7.11.12

Changed the reset value (bolded) and the name of bit 0 in the register table to match the name used in the description (LDD).

0h B010 0004 **LCSR: LCD Status Register** **Read/Write and Read-Only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				OUU	OOU	OUL	OOL	IUU	IOU	IUL	IOL	ABC	BER	BAU	LDD
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**

Bits	Name	Description
0	LDD	LCD disable done flag. 0 – LCD has not been disabled and the last active frame completed. 1 – LCD has been disabled and the last active frame has just completed.

43. LCD Controller Register Locations: Section 11.7.12

In the second sentence in this section, changed the figure references. The second sentence now appears as follows:

Figures 11-10 to **Figure 11-14** describe the LCD controller timing parameters.

44. UDC Endpoint Data Register: Section 11.8.10

Changed the Bottom of Endpoint 0 FIFO and Top of Endpoint 0 FIFO reset values from 0 to “?”.

	0h 8000 001C			UDCD0				Read/Write
	7	6	5	4	3	2	1	0
	Bottom of Endpoint 0 FIFO							
Reset	?	?	?	?	?	?	?	?
	Read Access							
	7	6	5	4	3	2	1	0
	Top of Endpoint 0 FIFO							
Reset	?	?	?	?	?	?	?	?

45. UDC Data Register: Section 11.8.12

Changed the Bottom of Receive FIFO and Top of Transmit FIFO reset values from 0 to “?”.

	0h 8000 0028			UDCDR				Read/Write
	7	6	5	4	3	2	1	0
	Bottom of Receive FIFO							
Reset	?	?	?	?	?	?	?	?
	Read Access							
	7	6	5	4	3	2	1	0
	Top of Transmit FIFO							
Reset	?	?	?	?	?	?	?	?

46. HP-SIR * Enable (HSE): Section 11.10.4.1

The second sentence has been changed and now appears as follows:

When HSE=0, HP-SIR * modulation is disabled, and if UART operation is enabled (ITR=0), it is used for normal serial transmission rather than IrDA communication.

47. Sample Clock GPIO: Section 11.11.3.5

In the third paragraph, second sentence, modify the GPIO number as indicated in bold. The sentence now appears as follows:

When the external sample clock function is enabled, serial port 1 uses the GPIO 18 pin and serial port 3 uses **GPIO 20**.

48. UART Data Register: Section 11.11.6

Changed the reset values of Bottom of Receive FIFO Data and Top of Transmit FIFO Data from zero to “?”.

0h 8005 0014 — UTDR — Read/Write

	10	9	8	7	6	5	4	3	2	1	0
	ROR	FRE	PRE	Bottom of Receive FIFO Data							
Reset	0	0	0	?	?	?	?	?	?	?	?
	Read Access Note: ROR, FRE, PRE are not read, but rather are transferred to corresponding status bits in UTSR1 each time a data value is transferred to UTDR.										

	7	6	5	4	3	2	1	0
	Top of Transmit FIFO Data							
Reset	?	?	?	?	?	?	?	?

49. SSP Transmit and Receive FIFOs: Section 11.12.7.3

In the fourth paragraph, deleted the fourth sentence and modified the last sentence. The paragraph now appears as follows:

The width of each entry within the FIFOs is 16 bits. However, the SSP supports data sizes of 4 through 16 bits. Any data that is less than 16-bits wide must be left-justified when writing or DMAing data to the transmit FIFO. Figure 11-36 shows the required data alignment for the transmit and receive FIFOs. The user must left-justify data to be transmitted, however, data read from the receiver is automatically right-shifted the appropriate amount, requiring no further modification before using the results.

50. SSP Data Register: Section 11.12.11

Changed the “Top of Receive FIFO” to the” Top of Transmit FIFO” and changed the reset values of Bottom of Receive FIFO and Top of Transmit FIFO from zero to “?”.

0h 8007 006C — SSP Data Register: SSDR — Read/Write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Bottom of Receive FIFO															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
	Read Access															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Top of Transmit FIFO															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
	Write Access															

51. PPC Pin Direction Register: Section 11.13.3

Changed the reserved bit reset values from 0 to 1 in the PPC pin direction register table.

0h 9006 0000 PPC Pin Direction Register: PPDR Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										SFRM	SCLK	RXD4	TXD4	RXD3	TXD3	RXD2	TXD2	RXD1	TXD1	L_BIAS	L_FCLK	L_LCLK	L_PCLK	LDD 7	LDD 6	LDD 5	LDD 4	LDD 3	LDD 2	LDD 1	LDD 0
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(Sheet ? of ?)

52. PPC Pin State Register: Section 11.13.4

Changed the reserved bit reset values from 0 to 1 and bits 21:0 to “?” in the PPC pin state register table.

0h 9006 0004 PPC Pin State Register: PPSR Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										SFRM	SCLK	RXD4	TXD4	RXD3	TXD3	RXD2	TXD2	RXD1	TXD1	L_BIAS	L_FCLK	L_LCLK	L_PCLK	LDD 7	LDD 6	LDD 5	LDD 4	LDD 3	LDD 2	LDD 1	LDD 0
Reset	1	1	1	1	1	1	1	1	1	1	?	?	?	?	?	?	v	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

(Sheet ? of ?)

53. PPC Pin Assignment Register: Section 11.13.5.2

Changed the reserved bit reset values from 0 to 1 in the PPC pin assignment register table.

0h 9006 0008 PPC Pin Assignment Register: PPAR Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													SPR	Reserved					UPR	Reserved											
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1

(Sheet ? of ?)

54. DC Operating Conditions: Section 12.2

In Table 12-2, rows Ioh and Iol have been removed and row ESD has had information added along with note 5, as indicated in bold. Table 12-2 now appears as follows:

Table 12-2. SA-1110 DC Operating Conditions

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vihc	IC input high voltage	0.8 × VDDX	—	VDDX	V	1, 2
Vilc	IC input low voltage	0.0	—	0.2 × VDDX	V	1, 2
Vohc	OCZ output high voltage	0.8 × VDDX	—	VDDX	V	1, 3
Volc	OCZ output low voltage	0.0	—	0.2 × VDDX	V	1, 3
Iohc	High-level output current	—	—	– 2	mA	—
Iolc	Low-level output current	—	—	2	mA	—
Ta	Ambient operating temperature	0	—	70	°C	—
Iin	IC input leakage current	—	10	—	µA	—
Cin	Input capacitance	—	5	—	pF	4
ESD	HBM model ESD	—	1	**750**	V	**5**

NOTES:
1. Voltages measured with respect to VSS.
2. IC – CMOS-level inputs (includes IC and ICOCZ pin types).
3. OCZ – Output, CMOS levels, tristateable.
4. Parameter guaranteed by design.
5. **PLL supply (Vddp)**.

55. Power Supply Voltages and Currents: Section 12.3

Several rows of Table 12-3 have had information added and the note has been modified, as indicated in bold. This section now appears as follows:

Table 12-3. SA-1110 Power Supply Voltages and Currents

Parameter	SA-1110		Units
	AC	BC	
Typical VDD	1.55	1.75	V
Maximum operating frequency	133	206	MHz
Maximum run mode power (total VDD + VDDX)	TBD	TBD	mW
Typical run mode power (total VDD + VDDX)	240	400	mW
Maximum idle mode power† (total VDD + VDDX)	TBD	TBD	mW
Typical idle mode power† (total VDD + VDDX)	75	100	mW
Maximum sleep mode current † (total VDD + VDDX, with VDD = 0)	**75**	75	uA
Typical sleep mode current † (total VDD + VDDX, with VDD = 0)	**50**	50	uA
VDD			
Minimum internal power supply voltage	1.47	**1.65**	V
Nominal internal power supply voltage	1.55	1.75	V
Maximum internal power supply voltage	1.63	**2.1**	V
VDDX			
Minimum external power supply voltage	3.00	3.00	V
Nominal external power supply voltage	3.30	3.30	V
Maximum external power supply voltage	3.60	3.60	V

† Room temperature specification.

Note: Only maximum values are guaranteed by manufacturing test screen. **Due to end-of-life status for B1 components, B-1 data has been eliminated from** Table 12-3**.**

56. Timing Parameters: Section 13.6

As indicated in bold, several parameters have changed in Table 13-3. Note 1 has been modified and Note 3 has been added to bottom of the table.

Table 13-3. SA-1110 AC Timing Specifications and Guidelines for SDRAM/SMROM

Pin Name	Symbol	Parameter	AC or BC (133 MHz or 206 MHz maximum operating frequency)	SDCLK Frequency (MHz)	Non-Delayed or Delayed Latching on Read Data	Min	Unit	Note
Memory Bus								
A<25:0>, D<31:0>, nRAS/nSDCS<3:0>, nCAS/DQM<3:0>, nCS<3:0>, nSDRAS, nSDCAS, nWE, nOE, SDCKE<1:0>	Tsdos	SDRAM/ SMROM output setup time to SDCLK<2:0> rise	AC	28 - 66		**2.2**	ns	**3**
			BC	28 - 103		**2.2**	ns	**3**
A<25:0>, D<31:0>, nRAS/nSDCS<3:0>, nCAS/DQM<3:0>, nCS<3:0>, nSDRAS, nSDCAS, nWE, nOE, SDCKE<1:0>	Tsdoh	SDRAM/ SMROM output hold time from SDCLK<2:0> rise	AC	28 - 66		2.2	ns	
			BC	28 - 103		2.2	ns	
D<31:0>	Tsdis	SDRAM/ SMROM data input setup time to SDCLK<2:0> rise	AC	28 - **66**	Non-Delayed	**7.2**	ns	1
			BC	28 - 62	Non-Delayed	9.3	ns	1
				62 - 103	Delayed	2.7	ns	1
D<31:0>	Tsdih	SDRAM/ SMROM data input hold time from SDCLK<2:0> rise	AC	28 - **66**	Non-Delayed	2.7	ns	1
			BC	28 - 62	Non-Delayed	2.7	ns	1
				62 - 69	Delayed	**5.5**	ns	1, 2
				69 - 7**6**	Delayed	4.**7**	ns	1, 2
				7**6** - 84	Delayed	4.1	ns	1, 2
				84 - 91	Delayed	**3.6**	**ns**	**1, 2**
				91 - 98	**Delayed**	**3.1**	**ns**	**1, 2**
				98 - 103	Delayed	2.7	ns	1

NOTES:

1. **Tsdis and Tsdih are specified for non-delayed read data latching on 133 MHz (AC) and 206 MHz (BC) devices, and for delayed read data latching at the maximum SDCLK frequency on BC devices (103 MHz when using a 3.6864 MHz crystal). All other Tsdis and Tsdih values (i.e.- those for delayed read data latching on BC devices with SDCLK between 62 MHz and 98 MHz) should be considered as guidelines, and are not guaranteed for use under all operating conditions.**
2. The larger Tsdih values can be achieved by intentionally adding delay to SDCLK (e.g., by using serpentine board routing). However, the system designer must carefully evaluate the resulting degradation to input setup time and output hold time: Tsdis and Tsdoh increase and decrease, respectively, from the corresponding table values.
3. **When SDRAM/SMROM is configured to run at one-half the memory clock frequency (e.g., MDREFR:K0DB2 = 1 for SMROM), the minimum output setup time is increased from Tsdos by approximately one memory clock period. This helps to accommodate SMROM, which typically requires both a lower frequency and larger setup times than SDRAM.**

57. Timing Parameters: Section 13.6

As indicated in Table 13-5, Trxds min is now 11 ns (was previously 0 ns) and Trxdh is 0 ns (was previously 4 ns).

Table 13-5 SA-1110 AC Timing Table: MCP Interface and LCD Controller

Pin Name	Symbol	Parameter	Min	Max	Unit	Note
MCP (CODEC) Interface						
SFRM_C	Tsfrmv	SCLK_C rise to SFRM_C driven valid	—	21	ns	—
RXD_C	Trxds	RXD_C valid to SCLK_C fall (input setup)	**11**	—	ns	—
	Trxdh	SCLK_C fall to RXD_C invalid (input hold)	**0**	—	ns	—
TXD_C	Ttxdv	SCLK_C rise to TXD_C valid	—	22	ns	—
LCD Controller						
L_LDD<7:0>	Tpclkdv	L_PCLK rise/fall to L_LDD<7:0> driven valid	—	14	ns	1
L_LCLK	Tpclklv	L_PCLK fall to L_LCLK driven valid	—	14	ns	2
L_FCLK	Tpclkfv	L_PCLK fall to L_LFCLK driven valid	—	14	ns	2
L_BIAS	Tpclkbv	L_PCLK rise to L_BIAS driven valid	—	14	ns	2

58. Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2

The Stepping row of the table has had information for B4 added (as indicated in bold) and now appears as follows:

Stepping	Stepping revision of the SA-1110 0000 = A0 stepping 0100 = B0 stepping 0101 = B1 stepping 0110 = B2 stepping **1000 = B4 stepping**

59. Boundary-Scan Interface Signals: Section 16.7

Removed the reference to note 8 in the last two rows of Table 16-1. The last two rows of this table now appear as follows:

Table 16-1. SA-1110 Boundary-Scan Interface Timing

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
Tbsrs	**TMS** setup to TRr	10	—	—	ns	—
Tbsrh	**TMS** hold from TRr	10	—	—	ns	—

NOTES:
1. Assumes a 25-pF load on TDO. Output timing derates at 0.072 ns/pF of extra load applied.
2. TDO enable time applies when the TAP controller enters the Shift-DR or Shift-IR states.
3. TDO disable time applies when the TAP controller leaves the Shift-DR or Shift-IR states.
4. For correct data latching, the I/O signals (from the core and the pads) must be set up and held with respect to the rising edge of TCK in the CAPTURE-DR state of the SAMPLE/PRELOAD and EXTEST instructions.
5. Assumes that the data outputs are loaded with the ac test loads.
6. Data output enable time applies when the boundary-scan logic is used to enable the output drivers.
7. Data output disable time applies when the boundary scan is used to disable the output drivers.
8. TCK may be stopped indefinitely in either the low or high phase.

60. Boundary Scan Interface Signals: Section 16.7

Changed the introductory sentence for Table 16-1 to indicate that these are guidelines for timing signals. The updated sentence now appears as follows:

Table 16-1 shows the SA-1110 boundary-scan interface timing guidelines.


POWERED
ARM
TM