# Intel® StrongARM* SA-1110 Development Board

## Specification Update

***June 2000***

**Notice:** The Intel® StrongARM* SA-1110 Development Board may contain design defects or errors known as errata. Characterized errata that may cause the board's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278325-003

# Contents

# Revision History

| Date | Version | Description |
|---|---|---|
| 6/16/00 | 003 | Added section 4.17, Video Output Design, as a specification clarification to the *Intel® StrongARM* SA-1110 Evaluation Board User's Guide*. Updated section 2.4 titled: Using the ARM ADS with the SA-1110 Development Platform. Moved existing SA-1110 Build Changes from the SA-1110 Development Board Hardware Release Notes to this document. Implemented minor changes to the *Intel® StrongARM* SA-1110 Evaluation Board Schematics* and the *Intel® StrongARM* SA-1110 Evaluation Board Parts List.* Updated Figure 1 in *Intel® StrongARM* SA-1110 Evaluation Board Cables* document. Added reset values to tables 4-5, 4-6, and 4-7. |
| 3/22/00 | 002 | Changed the power up procedures in Section 2 and changed the document title referenced for success and failure indications. Added section 2.4 titled: Using the ARM ADS with the SA-1110 Development Platform. Changed the description of GP[19]. Changed the description of the number of layers. |
| 1/31/00 | 001 | This is the new Specification Update document. It contains all identified errata published prior to this date. |

# Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## Affected Documents/Related Documents

| Title | Order |
|---|---|
| *Intel® StrongARM* SA-1110 Microprocessor Development Board User's Guide* | 278278-005 |
| *Intel® StrongARM* SA-1110/SA-1111 Development Kit Quick Start Procedures User's Guide* | 278339-002 |
| *Intel® StrongARM* SA-1110 Development Board Hardware Release Notes* | 278234-004 |
| *Intel® StrongARM* SA-1110 Microprocessor Development Board Schematics* | 278279-005 |
| *Intel® StrongARM* SA-1110 Development Board Parts List* | 278280-004 |
| *Intel® StrongARM* SA-1110 Development Board Cables* | 278331-001 |

# Nomenclature

**Errata** are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

***Note:*** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

# Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® StrongARM* SA-1110 Microprocessor Development Board (SA-1110 Development Board), order number SA1110DEVBD. Intel may fix some of the errata in a future stepping of the evaluation platform, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

## Codes Used in Summary Table

### Stepping

| | |
|---|---|
| X: | Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping. |
| (No mark) or (Blank box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |

### Page

| | |
|---|---|
| (Page): | Page location of item in this document. |

### Status

| | |
|---|---|
| Doc: | Document change or update will be implemented. |
| Fix: | This erratum is intended to be fixed in a future step of the component. |
| Fixed: | This erratum has been previously fixed. |
| NoFix: | There are no plans to fix this erratum. |
| Eval: | Plans to fix this erratum are under evaluation. |

### Row

| | |
|---|---|
| **\|** | Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document. |

# Errata

| No. | Board Revision | | | Page | Status | ERRATA |
|---|---|---|---|---|---|---|
| | 1.*xx* | 2.*xx* | | | | |
| 1 | X | X | | 12 | Fix. | Pressing the reset button while the unit is reading data from SDRAM may result in a hang condition. |
| 2 | X | | | 12 | Fix | High core power consumption on Revision A SA-1110 devices may cause power management problems |

# Specification Changes

| No. | System Revision | | | Page | Status | SPECIFICATION CHANGES |
|---|---|---|---|---|---|---|
| | 2 | 4 | 5 | | | |
| 1 | X | | | 13 | | Li-Ion batteries not shipped with systems except for system revisions 4.0 and beyond |
| 2 | X | X | X | 13 | | Some components are not installed on the SA-1110 Development Board |
| 3 | X | X | X | 13 | | Some components require special instructions |
| 4 | X | X | X | 14 | | Some components may be substituted |
| 5 | X | X | X | 14 | | Some components may be used for future performance enhancements |
| 6 | X | X | X | 14 | | Engineering change orders due to specification changes |
| 7 | X | X | X | 15 | | Engineering change orders due to backlight backlight inverter addition |

# Specification Clarifications

| No. | System Revision | | | Page | Status | SPECIFICATION CLARIFICATIONS |
|---|---|---|---|---|---|---|
| | 2 | 4 | 5 | | | |
| 1 | X | X | X | 16 | | Added Video Output Design Section to Chapter 4 |

# Documentation Changes

| No. | Document Revision | Page | Status | DOCUMENTATION CHANGES |
|---|---|---|---|---|
| 1 | 278278-005 | 18 | Doc | Intel® StrongARM® SA-1110 Development Board Software: Section 2.1.3 |
| 2 | 278278-005 | 18 | Doc | Board Control Register: Table 4-6 |
| 3 | 278278-005 | 18 | Doc | Connecting Power from an AC Adapter: Section 2.2.1 |
| 4 | 278278-005 | 21 | Doc | Connecting Power from the Li-Ion Battery: Section 2.2.2 |

# Documentation Changes

| No. | Document Revision | Page | Status | DOCUMENTATION CHANGES |
|---|---|---|---|---|
| 5 | 278278-005 | 22 | Doc | Using the ARM* ADS with the SA-1110 Development Platform: Section 2.4 |
| 6 | 278278-005 | 24 | Doc | Intel® StrongARM* SA-1110 GPIO Pin Descriptions: Section 4.3.2 |
| 7 | 278278-005 | 24 | Doc | Physical Description: Section 2.1 |
| 8 | 278278-005 | 24 | Doc | USB Client Port: Section 4.18 |
| 9 | 278280-004 | 25 | Doc | Intel® StrongARM* SA-1110 Development Board Parts List Section 1.0 |
| 10 | 278279-005 | 25 | Doc | Intel® StrongARM* SA-1110 Development Board Schematics Section 1.0 |
| 11 | 278331-001 | 25 | Doc | Intel® StrongARM* SA-1110 Development Board Cables Section 1.0 |
| 12 | 278331-001 | 26 | Doc | Intel® StrongARM* SA-1110 Development Board Cables Figure 1 |
| 13 | 278278-005 | 26 | Doc | System Configuration Bit Description Table 4-5 |
| 14 | 278278-005 | 27 | Doc | Board Control Bit Register Table 4-6 |
| 15 | 278278-005 | 30 | Doc | Board Status Register Table 4-7 |

# Identification Information

## Markings

This document contains errata for the SA-1110 Development Board. The board's revision that is affected by this errata can be identified as order number SA1110DEVBD. All SA-1110 Development Boards are labeled with two stickers for indicating the order number of the board, the serial number, the board's revision, and the system revision.

The sticker on side 2 near L1 identifies the order number of the board and provides a serial number and the board's revision number in the following format: SA111DEVBD VSxxxxxxx R2.0X, where SA1111DEVBD is the order number, VSxxxxxxx is the serial number and R2.0X is the board's revision number. For the board's revision number, the R2 indicates a pass 2 module while the .0X indicates the module build changes, such as engineering change orders.

A second sticker on side two near the USB connector indicates the system type and the system revision in the following format: SA1110DEVBD-BOX REV:X.0, where SA1110DEVBD-BOX indicates this is an SA-1110 Development Board system and REV:X.0 indicates the system revision. System revision information determines what is provided with the board.

# Errata

## 1. Pressing the reset button while the unit is reading data from SDRAM may result in a hang condition.

**Problem:** There is about a 10% chance of a hang condition occurring upon any press of the reset button. This is a documented problem with the SA-1110 microprocessor component, for more information see the *Intel® StrongARM® SA-1110 Microprocessor Specification Update*. The hang condition leaves the SDRAM driving the main data bus. Pressing reset will not clear the condition and removing input power for a few seconds is not long enough for the unit to properly reset to a cold start mode.

**Implication:** The system hangs and remains in a hang state.

**Workaround:** The hang condition can be cleared by unplugging all connections from the unit including the base station header, compact flash card and power input jack and the J22 battery enable jumper. The unit must be allowed to remain unpowered for at least three minutes in order for the battery backup capacitor to bleed down to zero volts.

**Status:** Fix.

## 2. High core power consumption on Revision A SA-1110 devices may cause power management problems

**Problem:** Board revision 1 of the SA-1110 Development Boards were shipped with revision A SA-1110 devices that have a high core power problem. These revision A SA-1110 devices consume too much power for power management related development, however these devices are still suitable for most non-power management development.

**Implication:** Board revision 1 of the SA-1110 Development Boards (with revision A components) may not be suitable for developing power management applications.

**Workaround:** Upgrade your SA-1110 Development Board with a revision B component.

**Status:** Fix.

# Specification Changes

## 1. Li-Ion batteries not shipped with systems except for system revisions 4.0 and beyond

Only systems revisions 4.0 and beyond have Li-Ion batteries shipped with them.

## 2. Some components are not installed on the SA-1110 Development Board

Section I of the SA-1110 Development Board Hardware Release Notes indicated that the following components were note installed on the SA-1110 Development Board. The information at the time was a last minute update and is now moved into this specification update.

The following components are not installed:

### Table 1. Components Not Installed

| Item | Schematic Sheet | Reference Designator | Component Value | Part Number |
|---|---|---|---|---|
| 1.1 | 2 | R52 | 100K Ohm Resistor | 13-0100K-X |
| 1.2 | 7 | R103 | 10 Ohm Resistor | 13-00010-X4 |
| 1.3 | 8 | R158 | 511K Ohm Resistor | 13-0511K-X4 |
| 1.4 | 9 | R107, R128, R133, R155, R165 | Zero Ohm Jumper | 13-00000-X4 |
| 1.5 | 10 | R23 | 825K Ohm Resistor | 13-0825K-X4 |
| 1.6 | 10 | R13 | 237K Ohm Resistor | 13-0237K-X4 |
| 1.7 | 10 | R134 | 1.5M Ohm Resistor | 13-01P5M-X4 |
| 1.8 | 10 | R10 | 100K Ohm Resistor | 13-0100K-X4 |
| 1.9 | 2 | R55, R63, R64 | 100K Ohm Resistor | 13-0100K-X4 |
| 1.10 | 2 | E1 (Socket pairs) | Mill-MAX BGA Socket<br>Mill-MAX BGA Carrier | 12-TM256-BS<br>12-TM256-CC |
| 1.11 | 3 | E11,E12 (sockets) | Meritec Socket | 12-TM177-NP |

## 3. Some components require special instructions

Section 2 of the SA-1110 Development Board Hardware Release Notes indicated that the following components require special instructions on the SA-1110 Development Board. The information at the time was a last minute update and is now moved into this specification update.

The following components require special instructions:

R147 and R148 are redundant pull-up resistors on JTAG-TCK and JTAG_TMS. These resistors may remain or be removed from the SA-1110 Development board.

## 4. Some components may be substituted

Section 3 of the SA-1110 Development Board Hardware Release Notes indicated that the following components may be substituted on the SA-1110 Development Board. The information at the time was a last minute update and is now moved into this specification update.

The following components may be substitued:

### Table 2. Components that may be substituted

| Item | Part Number | Primary Vendor P/N | Secondary Vendor/P/N |
|---|---|---|---|
| 2 | 10-100UF-XD | AVX TPSD107K010R0150 | AVX TPSD107K010R0100 |
| 9 | 10-TM161-NP | Panasonic ECU-E1H470JCQ | Kemet<br>C0402C470J5GAC |
| 14 | 10-TM139-NP | Novacap 1206Z223Z201NT | Novacap 1206B223Z201NT |
| 84 | 13-00010-X4 | Panasonic ERJ-2RKF10R0X | Dale CRCW040210R0FT |
| 26 | 23-TM100-NP | Samsung KM416S8030T-G8 | Toshiba TC59SM716FT80 |
| 127 | 12-EVQPU-SW | Panasonic EVQ-PUJ02K | Bourns Switch<br>7914J-001-00E<br>(Use at Ref Des S1-S8) |

## 5. Some components may be used for future performance enhancements

Section 4 of the SA-1110 Development Board Hardware Release Notes indicated that the following components may be used for future performance enhancements or as minimum design requirements on the SA-1110 Development Board. The information at the time was a last minute update and is now moved into this specification update.

The following components may be used for future performance enhancements:

### Table 3. Components that may be used for future performance enhancements

| Item | Reference Designator | Description |
|---|---|---|
| 26 | E2, E4 | Samsung 128Mb TSOP KM416S8030T-G8<br>Minimum part – Samsung 64 Mb SDRAM, 125Mhz, TSOP 54<br>Enhanced part – Samsung 256 Mb SDRAM, 125Mhz,TSOP 54 |
| 33 | E11, E12 | Intel 28F128J3A<br>Minimum part – Intel FlashFile(tm) 28F160S3, 16-Mbit Memory TSOP 56<br>Enhanced part – Intel StrataFlash(tm) 28F320J3A, 32-Mbit Memory TSOP 56<br>– Intel StrataFlash(tm) 28F640J3A, 64-Mbit Memory TSOP 56<br>– Intel StrataFlash(tm) 28F128J3A, 128-Mbit Memory TSOP 56 |

## 6. Engineering change orders due to specification changes

Section 5 of the SA-1110 Development Board Hardware Release Notes indicated engineering change orders (ECO's). The information at the time was a last minute update and is now moved into this specification update.

The following ECO's have been implemented on the SA-1110 Development Board.

***Note:*** Wire Guage is 30 AWG and is green in color

| ECO | Change |
|---|---|
| 5.1 | Added wire from E38 Pin 1 to E38 Pin 2, wire should be ~1/4 inch suitable for removal by breaking wires by end user. |
| 5.2 | Positioned Cap C111 so that its end is soldered to the end of C112, mounted capacitor pair at ~45' angle so that one end is soldered to C111's pad near the 'C' of the C111 silk-screen and the other end to the pad of C112 near the 'C' of C112's silk-screen. Added wire from junction of C111 and C112 to through-hole ground near the '2' in silk-screen of C112.<br>Sheet 11 of the schematics shows C111 and C112 connected to LCOM--with this eco they are now connected to GND. |
| 5.3 | Flush cut J2 pins 1 through 20 and pins C1 through C4 (24 pins nearest J4) such that they do not cause damage to cables being plugged into J4. |
| 5.4 | Added a 1/4" wire from the through hole between D1 and the C54 super cap to the shield of D1. |
| 5.5 | Rotated R56 90' clockwise leaving only the pin 2 side hooked up. Ran a short (1/4" long) eco wire from the unattached side of R56 to AUDIO3P3V power on C80 pin1. |

## 7. Engineering change orders due to backlight backlight inverter addition

The following ECO's have been implemented on the SA-1110 Development Board to support backlight issues:

***Note:*** Wire Guage is 30 AWG and is green in color

| ECO | Change |
|---|---|
| 6.1 | Ran an ECO wire from J22 pin 2 to J13 pin 3 (this is a long wire that is tacked down). A 100K ohm 1/8 W coaxial resistor has been added between J13 pins 1 and 5. |
| 6.2 | A cable to connect J13 to CN1 has been added to the kit. This connection has a Linfinity inverter part number LXM1615-04-30050 and a cable Linfinity part number LX9506. The cable comes with a single connector on the CN1 inverter end. This 5 wire 2 inch cable has 5 Berg part number 77138-001 connectors and one Burg part number 90312-005 connector housing. This cable plugs from J13 to CN1.<br>The cable pin wiring from J13 and CN1 is as follows:<br>J13 CN1<br>1 2<br>2 4<br>3 1<br>4 3<br>5 5<br>The cable from the backlight plugs directly into the inverter CN2 and is indexed to prevent it from being plugged in backwards. |

# Specification Clarifications

## 1. Added Video Output Design Section to Chapter 4

Added Video Output Design in Section 4.17. Section 4.17 now appears as follows in the *Intel® StrongARM* SA-1110 Evaluation Board User's Guide*:

## 4.17 Video Output Design

The TV video output design in the SA-1110 Development board uses an ADV7171* NTSC/PAL encoder. The ADV7171 offers the following features:

- 16-bit pixel stream needed by SA-1110 TV video applications.
- Four DACs to allow simultaneous output of CVBS and RGB signals. This is very useful in TV core designs where the ADV7171 will drive the CRT RGB circuitry directly.
- Programmable color subcarrier PLL allows nonstandard video timing while maintaining color lock in the TV. This allows the SA-1110 to use the standard 3.6864 MHz crystal. The 4.2.2 YUV pixel interface to the ADV7171 from the SA-1110 uses 16 LCD data lines 8 of which are GPIOs.

The clock for the ADV7171 must be twice that of the 12.27 MHz LCD clock supplied by the SA-1110 when it is programmed with TV video timings. This clock doubler is implemented in the LCD CPLD.

### 4.17.1 SA-1110 Core Clock Frequency

The following is a discussion of how the SA-1110 core timing is adapted to TV timing. The purpose of this discussion is to provide an understanding of how the SA-1110 can be adapted to TV timing.

The goal is to find a 3.xxxx MHz crystal frequency that is as close as possible to the 3.6864 MHz nominal frequency and that has an integer multiple close to the 206 MHz maximum SA-1110 core clock. At the same time this 2XX MHz core clock must have an integer divisor that produces exactly 12.272725 MHz.

First find a multiple of 12.272725 MHz that comes closest to the highest core frequencies specified in the clock chapter of the *SA-1110 Microprocessor Technical Reference Manua*l. Then substitute the exact 12.272725 MHz multiple and re-deriving the 3.XXXX MHz crystal required to generate a 2XX MHZ clock that is an exact multiple of 12.272725 MHz. This approach results in a new 3.681818 MHz crystal frequency that is within less than 0.15% of the optimal 3.6864 MHz. 3.681818 MHz times 4 times 15 yields the desired 220.90 MHz core clock while 220.90 MHz divided by 18 yields the 12.272725 MHz required for the TV video encoder. The SA-1110 reference design will use the standard 3.6864 MHz crystal. To compensate for the color subcarrier video timing errors that this produces in the encoder color burst generator, color subcarrier PLL control registers in the ADV7171 are programmed to compensate for this error. The 147MHz SA-1110 clock selection also results in a 0.15% accurate TV clock.

The SA-1110 reference design diagnostic manager contains example code that adjusts the SA-1110 LCD timing parameters to allow the ADV7171 to operate in color with the full range of core clock selections.

## 4.17.2 Interlaced Video

An NTSC frame of 525 lines displayed at 30 Hz interlaced consists of two fields of 262.5 lines displayed at 60 Hz. Normally this is achieved in a video controller by having the vertical timing generator count half-lines (instead of full lines) and programming it to 525 half-lines. This produces a vsync every 262.5 lines and provides the ½ line offset between fields required for interlaced timing. Since there is no provision for the interlaced timing in the SA-1110 LCD controller, the interlaced timing must be done somewhat differently.

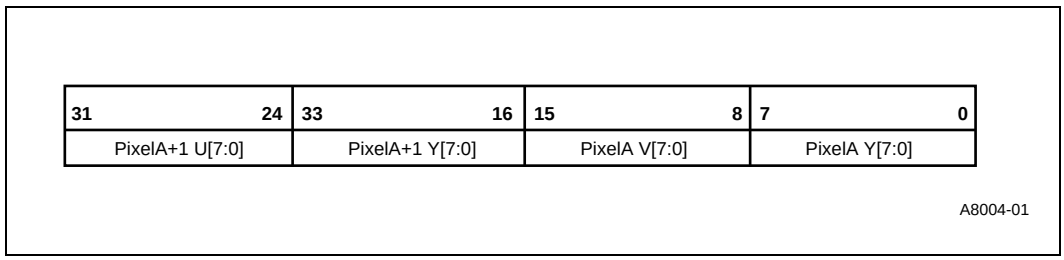
## 4.17.3 Video Output Interlaced Timing Generation

The SA-1110 LCD controller is programmed for 525 lines of video displayed at a 30 Hz rate. The ADV7171 tracks this video timing and will regenerate the missing vertical sync pulse at the correct ½ line point resulting in a 262.5 line 60Hz interlaced timing output.

## 4.17.4 Interlaced Display Buffer

The video image in the SA-1110 DRAM must be written in interlaced order and with regard to where the two fields are normally blanked. Although this complicates the rendering code, it is possible to design rendering routines that are just as efficient as normal line sequential rendering. The interlaced frame buffer image in SA-1110 DRAM contains YUV components in 4.2.2 format. Each 32-bit word in the DRAM frame buffer contains four 8-bit video components appearing as UYVY.

**Figure 4-6. Interlaced Frame Buffer**




***Note:*** The representation of the color information in SA-1110 memory is an arbitrary selection between UYVY and YUYV. In the board design, the ADV7171 inputs Y on bits 7:0 and UV on bits 15:8.

Video out data in a YUV format has an advantage over video processed by an RGB display device. When video is processed to an RGB display device, such as a SVGA LCD display, an extra rendering step to convert from YUV to RGB is necessary. Maintaining the video image in its native YUV color space avoids this computationally intensive step and results in higher frame rates for H324 video conferencing and allows real time 30 FPS CCIR601 video pass through.

# Documentation Changes

## 1. Intel® StrongARM® SA-1110 Development Board Software: Section 2.1.3

This section has been replaced with the following text:

The following source and executable files are available from the StrongARM section in the developer's area on the Intel website:

- Angel debug monitor – Software component for StrongARM based on ARM version 1.2 that loads an application from a remote host computer or application flash.
- Set of microHal libraries – Lowest level software that provides initialization for the StrongARM evaluation boards. This layer, provided as source-code for a library, resides between the actual hardware and any Real Time Operating System (RTOS) or user application.
- Diagnostics – A set of test programs that analyze the functions of SA-1110 Development Boards and SA-1111 Development Modules.
- A set of sample I/O drivers are provided and available for developers using Windows* CE.

## 2. Board Control Register: Table 4-6

The values for bit 10, LCD12or16, have been transposed. The definitions for bits 19 and 20 are now I2CENAB and IRDECODE. The rows for bits 10, 19, and 20 now appear as follows:

**Table 4-6. Board Control Register**

| Bits | Name | Description |
|---|---|---|
| 10 | LCD12or16 | LCD 12bpp or 16bpp output select<br>Configures the PZ3128 CPLD to map the SA-1110 LCD data pins as 12 bit RGB444 or 16 bit RGB565.<br>0 – 12RGB<br>1 – 16RGB |
| 19 | I2CENAB | I2C Switch Enable<br>0 – Off<br>1 – On<br>Must be set to zero to allow compact flash cards to function |
| 20 | IRDECODE | IR Decode Enable<br>0 – Off<br>1 – On<br>Must be set to zero to allow IRDA to function |

## 3. Connecting Power from an AC Adapter: Section 2.2.1

This section has been modified, renamed, renumbered and now appears as follows:

## 2.3 Providing Power for Only the SA-1110 Development Board

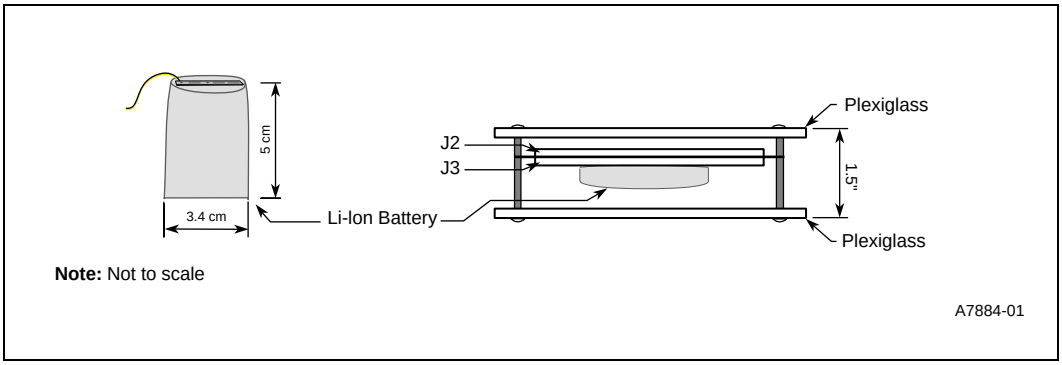
Use the following procedure to provide power only for the SA-1110 Development Board. To provide power for the SA-1110 Development Board and the SA-1111 Development Module, see Section 2.3.

***Caution:*** The following procedure assumes that the jumper (shunt) for J22, the Master Power Clip for the Li-ion battery, has been removed and that all power associated with the SA-1110 Development Board is off. For more information about Li-ion battery considerations, see Chapter 6.

***Note:*** A very high value capacitor of 0.33 Farads (super cap) is connected in parallel with the power input from J10. This capacitor provides enough power to support the system for several minutes in sleep mode when power from J10 is removed.

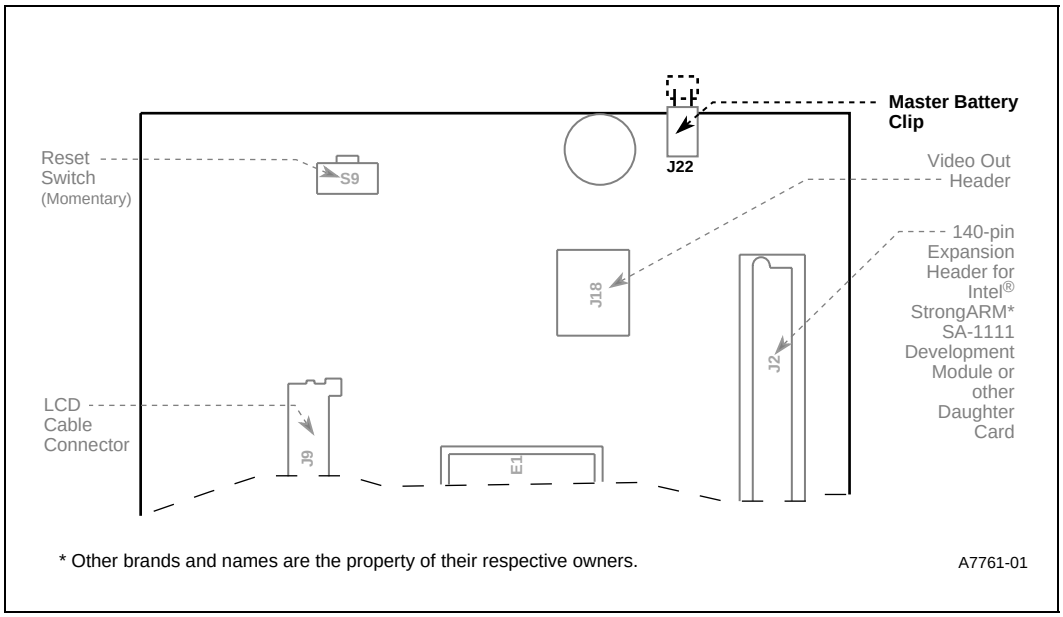
1. Verify that the Li-Ion battery is installed on the SA-1110 Development Board and that the battery harness is connected to J4 (see Figure 2-3 for the location of the Li-Ion battery).

**Figure 2-3. Li-Ion Battery Location**



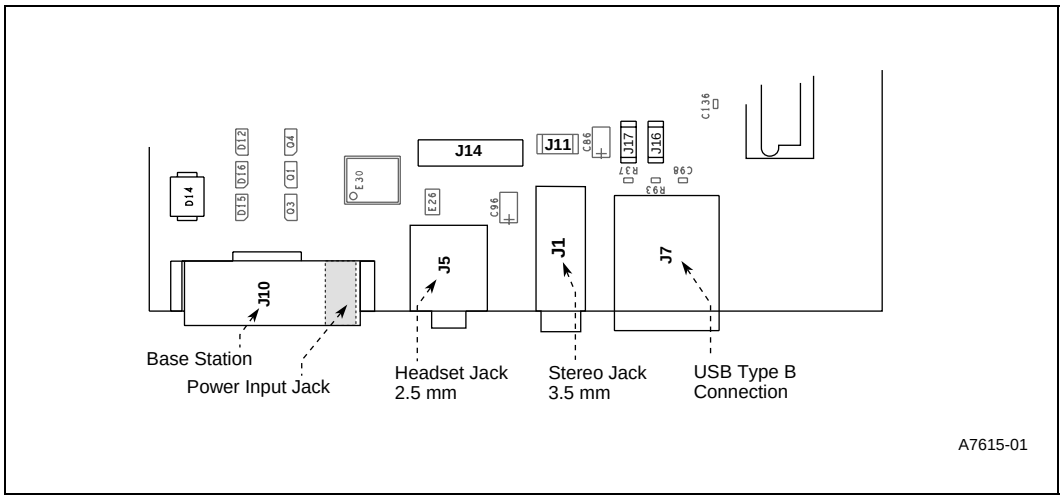
2. Verify that the jumper (shunt) for J22 is **inserted** on the Master Power Clip (J22 should appear covered).

**Figure 2-4. Master Power Clip Location**




3. Select the appropriate AC adapter to DC converter device (wall brick) depending upon whether you are in a 110-volt or 220-volt environment.
4. Insert the power jack that is connected to the wall brick into J10 (see Figure 2-5 for the location of J10).

**Figure 2-5. AC Power Input Jack Location**




***Note:*** The power jack may have to be rotated to its flat side to accommodate any other connectors in J10.

5. Plug in the wall-brick into an AC outlet.
6. See the *Intel® StrongARM* SA-1110/SA-1111 Development Kit Quick Start User's Guide* for success and failure indications of start-up diagnostic results and how to proceed.

To disconnect power, remove the power jack from J10 and remove the Master Power Clip from J22 and wait for the super cap to discharge (typically less than 5 minutes).

***Note:*** If sleep mode was entered as a result of VDD_FAULT or BATT_FAULT signals, GPIO 0 and GPIO 1 are the only wake up events that can bring the SA-1110 out of sleep mode.

## 4. Connecting Power from the Li-Ion Battery: Section 2.2.2

This section has been modified, renamed, renumbered and now appears as follows:

## 2.3 Providing Power for the SA-1110 Development Board and the SA-1111 Development Module

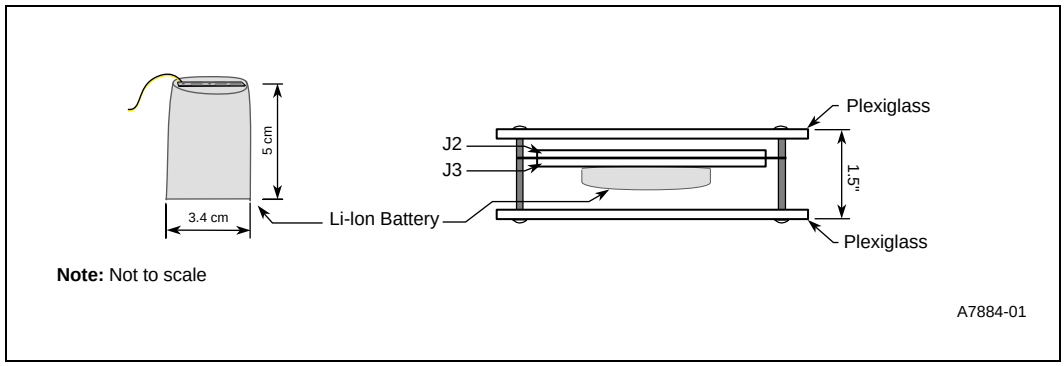
Use the following procedure to provide power for the SA-1110 Development Board and the SA-1111 Development Module. To provide power for only the SA-1110 Development Board, see Section 2.2.

***Caution:*** The following procedure assumes that all power associated with the SA-1110 Development Board is off. For more information about Li-ion battery considerations, see Chapter 6.

***Note:*** A very high value capacitor of 0.33 Farads (super cap) is connected in parallel with the power input from J10. This capacitor provides enough power to support the system for several minutes in sleep mode when power from J10 is removed.

1. Disconnect the battery harness from J4 and remove the Li-Ion battery from the SA-1110 Development Board (see Figure 2-6 for the location of the Li-Ion battery).

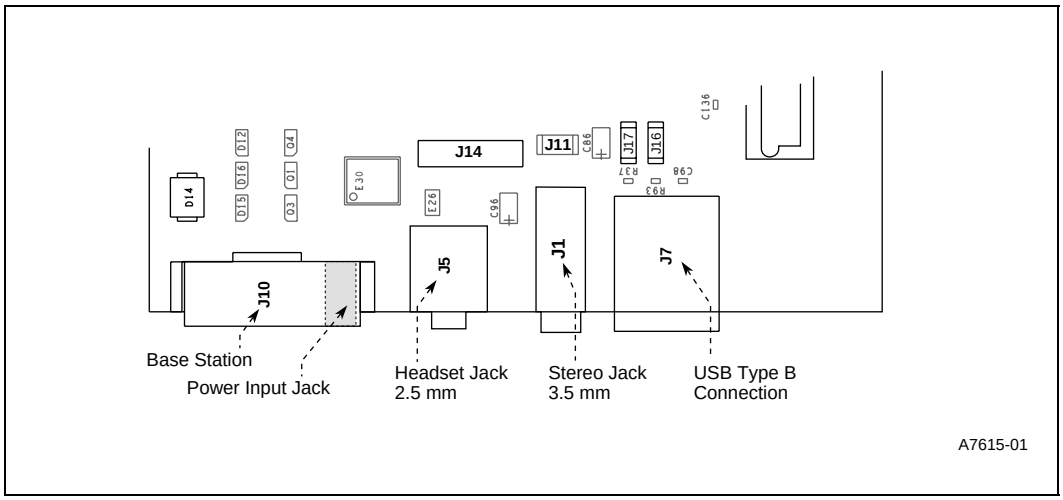
**Figure 2-6. Li-Ion Battery Location**




2. Assemble the SA-1110 Development Board with the SA-1111 Development Module, as described in the *Intel® StrongARM® SA-1111 Companion Chip Development Board User's Guide*.
3. Select the appropriate AC adapter to DC converter device (wall brick) depending upon whether you are in a 110-volt or 220-volt environment.

4. Insert the power jack that is connected to the wall brick into J10 (see Figure 2-7 for the location of J10).

**Figure 2-7. AC Power Input Jack Location**




***Note:*** The power jack may have to be rotated to its flat side to accommodate any other connectors in J10.

5. Plug in the wall-brick into an AC outlet.
6. See the *Intel® StrongARM* SA-1110 Development Board Quick Start User's Guide* for success and failure indications of start-up diagnostic results and how to proceed.

To disconnect power, remove the power jack from J10 and wait for the super cap to discharge (typically less than 5 minutes).

***Note:*** If sleep mode was entered as a result of VDD_FAULT or BATT_FAULT signals, GPIO 0 and GPIO 1 are the only wake up events that can bring the SA-1110 out of sleep mode.

## 5. Using the ARM* ADS with the SA-1110 Development Platform: Section 2.4

Add Section 2.4 to Section 2. Section 2.4 appears as follows:

# 2.4 Using the ARM* ADS with the SA-1110 Development Platform

The ARM Developer Suite (ADS) is provided in the SA-1110 Development Platform kit. The ARM ADS is a cross-development tool set for ARM processors and is provided with an integrated development environment. The ARM ADS includes a debugger that allows the debugging of applications running on the target SA-1110 Development Platform.

When running the ARM debugger, one part runs on the host (this part includes the user interface) and the other part runs on the target (the SA-1110 Development Platform). The host and target interact across a communications channel. By default, the SA-1110 Development Platform uses its RS232 port to communicate with the host. The software that runs on the target is called the *remote debug stub* or *debug monitor*. The debug monitor used with the SA-1110 Development Platform is a program called Angel.

## 2.17.5 Angel* Firmware

To use the ARM ADS with the SA-1110 Development Platform, Angel must be resident. See the Angel readme file for information on installing Angel.

## 2.17.6 Connecting the SA-1110 Development Platform to the Host

After installing the ARM ADS on the host system, connect the SA-1110 Development Board to the host using the base station cable that is supplied in the SA-1110 Development Platform kit. This split cable contains the Dsub9 serial port, Dsub25 JTAG, and RJ11 phone jack connectors. Connect the Dsub9 connector to the RS-232 serial port on the host. The black Base Station connector of the split cable containing the POTS and RS-232 signals must be connected to the Base Station header on side 1 (J10) of the SA-1110 Development Board.

The same serial connections and cable as described in the preceding paragraph can be used and is the recommended method for providing serial communications between the host and SA-1110 Development Platform when the companion SA-1111 Development Module is attached. For this to work, ensure that switchpak 2 (SW2), switch 3 (SW2-3) on the SA-1111 Development Module is in the ON position. For the location of SW2, refer to the SA-1111 Development Module User's Guide. Alternatively, serial communications between the host and target can be provided by the double-female Dsub9 terminated RS232 cable that comes in the SA-1111 Development Module kit and the serial ports (UART1 and UART3) on the SA-1111 Development Module. Refer to the *Intel*® StrongARM* *SA-1111 Development Module User's Guide* and the Angel software kit's readme.txt for more information on using those serial ports.

The 9-pin RS232 cable connected to the Base Station serial port (J10) on the SA-1110 Development Board cannot be connected at the same time as the UART1 serial port (J16) on the SA-1111 Development Module. Connecting them at the same time will corrupt the data on the UART1.

## 2.17.7 Bringing Up the Angel* Debug Monitor

To configure the debug environment, power up the SA-1110 Development Platform and invoke the ARM AXD Debugger on the host system. Select the Options menu and choose the Configure Target option. In the Choose Target dialog, select the ADP target and press the "Configure" button. The Remote_A Connection dialog appears. Press the Select button and choose the ARM serial driver. Press the "Configure" button. The Setup Serial Connection dialog will appear. Select the appropriate serial port (COM1..4) that is being used on the host for communicating to the SA-1110 Development Board. Select 115200 from the Baud Rate drop-down list. Only reduce the connection speed if you experience communications problems. Press "OK".

The following settings also should be made in the Remote_A Connection dialog:

Heartbeat – Should be disabled (not checked)

Endian – "Little" should be selected

Channel Viewers – Should be disabled (not checked)

Press "OK" in the Remote_A Connection dialog box to save the new settings. Press "OK" in the Choose Target box to accept the ADP target and activate remote debugging. A banner is printed in the RDI Log window of the AXD Debugger announcing the presence of the Angel Debug Monitor on the SA-1110 Development Platform.

### 2.17.8 Running an Application

The ARM ADS comes with some example applications that can be built and run. Follow the instructions above under Section 2.17.6 and connect the SA-1110 Development Platform to the host. On the host, invoke CodeWarrior for ARM Developer Suite. From the Files menu, select Open and navigate to the directory where the ARM SDK is installed. By default this directory is Program Files\ARM\ARM Developer Suite. Open the random number test project file, randtest.mcp, that can be found in Program Files\ARM\ARM Developer Suite\Examples\explasm. A window for the randtest project will appear. From the Project menu, select the "Make" option. The output window will display the progress and status of the build; there should be no errors.

Before running the randtest application, ensure that the SA-1110 Development Platform is connected to the host and apply power to it. It is assumed that the connections and remote configuration options have already been properly set as described in the previous Section 2.17.6 and Section 2.17.7. From the main CodeWarrior window select the Project menu and choose the "Run" option. The ARM AXD Debugger will be invoked. The Angel Debug Monitor will be started and the randtest application will be run. The console window will display the results of ten calls to the randomnumber() routine.

For more information on using the ADS, refer to the reference manual and user's guide in the Program Files\ARM\ARM Developer Suite\pdf directory or to the ARM web site at http://www.arm.com. A software kit containing Angel sources, images, and build directions for the SA-1110 Development Platform are provided on Intel's website at http://www.developer.intel.com under the StrongARM processors products software library.

## 6. Intel® StrongARM* SA-1110 GPIO Pin Descriptions: Section 4.3.2

Row GP[19] in Table 4-4 has been modified and now appears as follows:

**Table 4-4. GPIO Pin Descriptions**

| Pin Name | Signal Name | Description |
|---|---|---|
| GP[19] | SSP_UDA 1341 Extrn_Clk | SSP UDA1341 stereo codec external clock input |

## 7. Physical Description: Section 2.1

The description of the number of layers in the first paragraph has been changed and now appears as follows:

Figure 2-1 and Figure 2-2 shows the physical layout of the SA-1110 Development Board. The SA-1110 Development Board uses a 6-layer, micro-via, double-sided surface mount technology.

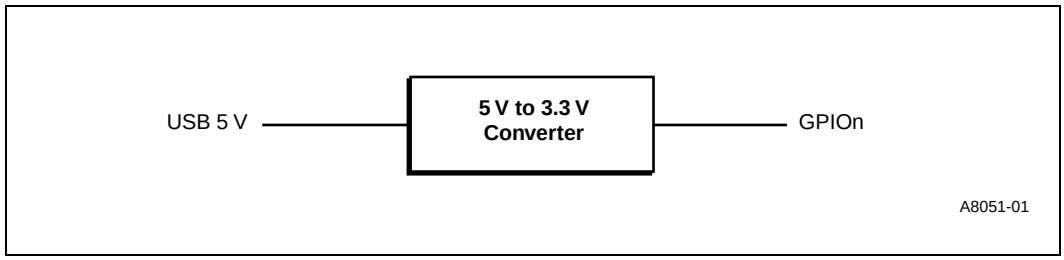
## 8. USB Client Port: Section 4.18

This section has been updated as follows:

The SA-1110 Development Board includes a standard USB client jack that allows the SA-1110 Development Board to communicate up to 12 Mbs as a USB client. This port may be used for high speed system synchronization between the SA-1110 Development Platform and a host PC.

To allow the USB to wake up a sleeping SA-1110 Development Board when it is plugged into a USB host port, the following circuit is required:

**Figure 4-8. Waking Circuit**




The USB port implementation on the SA-1110 Development board attempted to supply up to 500 mA of current at 5 V for use by the SA-1110 Development Board. However, this implementation does not conform to USB specifications for bus powered devices.

The SA-1110 device cannot support a bus powered device model because when the host initiates a suspend, the device is required to consume less than 500 µA (for more information, see section 7.2.3 of the USB specification, version 1.1). The device cannot limit its current consumption to 500 µA unless it enters sleep mode. Unfortunately, if the device enters sleep mode, all of the UDC registers are reset, and then it will not respond to its host-assigned address.

To prevent the SA-1110 Development Board from drawing power from the USB host, remove D6.

## 9. Intel® StrongARM* SA-1110 Development Board Parts List Section 1.0

The only section that changed in this document was the note indicating that it is for phase 5. The note appears as follows:

This document and module are for the Phase 5 hardware build of this product. For the latest information and updates, see the hardware release notes that are provided in hardcopy format, and the software readme.txt files that are provided in the software kits.

## 10. Intel® StrongARM* SA-1110 Development Board Schematics Section 1.0

The only section that changed in this document was the note indicating that it is for phase 5. The note appears as follows:

This document and module are for the Phase 5 hardware build of this product. For the latest information and updates, see the hardware release notes that are provided in hardcopy format, and the software readme.txt files that are provided in the software kits.

## 11. Intel® StrongARM* SA-1110 Development Board Cables Section 1.0

The note has been updated to indicate Phase 5. The note appears as follows:

This document and module are for the Phase 5 hardware build of this product. For the latest information and updates, see the hardware release notes that are provided in hardcopy format, and the software readme.txt files that are provided in the software kits.

## 12. Intel® StrongARM* SA-1110 Development Board Cables Figure 1

Figure 1, which is a B-size drawing, has been updated in this document. Because Figure 1 is so large, see Intel's website for Developers to see the latest drawing.

This document and module are for the Phase 5 hardware build of this product. For the latest information and updates, see the hardware release notes that are provided in hardcopy format, and the software readme.txt files that are provided in the software kits.

## 13. System Configuration Bit Description Table 4-5

Added reset values to Table 4-5. Table 4-5 now appears as follows::

### Table 4-5. System Configuration Bit Descriptions

| | System Configuration | | | | | | | | | | | | | | | | | | | | | SA-1110 Development Board | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Reserved | | | | | | | | | | | | | | | | | | | | | | SA-1111 | GFX | Reserved | | Flash_Size | | SDRAM_ Sizes | | Reserved | |
| Reset[a] | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? |

| Bits | Name | Type | Description |
|---|---|---|---|
| 1:0 | Reserved | — | — |
| 3:2 | SDRAM_ Size | Read only[b] | SDRAM size<br>11 – 128 Mbit devices. 32 Mbyte total bank size<br>10 – 64 Mbit devices. 16 Mbyte total bank size<br>01 – 256 Mbit devices. 64 Mbyte total bank size<br>00 – Reserved |
| 5:4 | Flash_Size | Read only[b] | Flash size<br>11 – 128 Mbit devices. StrataFalsh™ 32 Mbyte total bank size<br>10 – 32 Mbit devices. StrataFalsh™ 8 Mbyte total bank size<br>01 – 16 Mbit devices. FlashFile™ 4 Mbyte total bank size<br>00 – 64 Mbit devices. StrataFalsh™ 16 Mbyte total bank size |
| 7:6 | Reserved | — | — |
| 8 | GFX | Read only[b] | Graphics Accelerator board<br>0 – Present<br>1 – Not Present |
| 9 | SA-1111 | Read only[b] | SA-1111 Development Module<br>0 – Present<br>1 – Not Present |
| 31:10 | Reserved | — | — |

a. A question mark (?) indicates that this value is unknown at reset.
b. The values written in this bit are readable, but cannot be modified by software.

## 14. Board Control Bit Register Table 4-6

Added reset values to Table 4-6. Table 4-6 now appears as follows:

### Table 4-6. Board Control Register (Sheet 1 of 4)

**0x1200,0000 — Board Control Register — SA-1110 Evaluation Module**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Reserved | | | | | | | | Spk_Off | Rad_On | Qmute | IRDECODE | I2CENAB | Rad_WU | COM_RTS | COM_DTR | Vib_On | D8_LED | D9_LED | RS232En | LCD On | LCD12or16 | Light | Audio_On | CF_Bus_On | Stereo_LB | IRDA_MD[1:0] | | IRDA_FSEL | SOFT_RST | CF_RST GFX_RST | CF_PWR NEP_RST |
| Reset[a] | ? | ? | ? | ? | ? | ? | ? | ? | 1 | 0 | ? | ? | ? | ? | ? | ? | 0 | 1 | 1 | 0 | 0 | ? | 0 | 0 | 1 | ? | ? | ? | ? | ? | 0 | 0 |

| Bits | Name | Type | Description |
|---|---|---|---|
| 0 | CF_PWR | Write Only[b] | Compact Flash Power<br>0 – CF power off<br>1 – CF 3.3V power on<br>Must be programmed to 0 when system goes to sleep. |
| 1 | CF_RST GFX_RST | Write Only[b] | Codec Reset<br>0 – Holds UCB1300, ADI7171, and UDA1341 in reset<br>1 – Allows UCB1300, ADI7171 and UDA1341 to run<br>Must be programmed to 0 when system goes to sleep. |
| 3 | IRDA_FSEL | Write Only[b] | IRDA Frequency select<br>0 – SIR<br>1 – MIR/FIR<br>Controls IRDA chip data rate. Refer to IRDA chip vendor spec for details |
| 5:4 | IRDA_ MD[1:0] | Write Only[b] | IRDA Mode 1:0 Range/Power select<br>00 – Max range and power<br>01 – Shutdown. Power off<br>10 – 2/3 range and power<br>11 – 1/3 range and power<br>Must be programmed to 01 when system goes to sleep |
| 6 | Stereo_LB | Write Only[b] | Stereo Loopback<br>0 – Stereo loopback off<br>1 – Stereo loopback on<br>Stereo loopback is used by the system applications to route audio signals in the SA-1110 Development Board. Loopback is also used by diagnostic software. |
| 7 | CF_Bus_On | Write Only[b] | Compact Flash bus on<br>0 – CF BUS ON<br>1 – CF BUS off (float)<br>Must be programmed to 0 when Xbus daughter boards are present<br>Must be programmed to 1 when system goes to sleep |

### Table 4-6. Board Control Register (Sheet 2 of 4)

**0x1200,0000 — Board Control Register — SA-1110 Evaluation Module**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Reserved | | | | | | | | Spk_Off | Rad_On | Qmute | IRDECODE | I2CENAB | Rad_WU | COM_RTS | COM_DTR | Vib_On | D8_LED | D9_LED | RS232En | LCD On | LCD12or16 | Light | Audio_On | CF_Bus_On | Stereo_LB | IRDA_MD[1:0] | | IRDA_FSEL | SOFT_RST | CF_RST GFX_RST | CF_PWR NEP_RST |
| Reset[a] | ? | ? | ? | ? | ? | ? | ? | ? | 1 | 0 | ? | ? | ? | ? | ? | ? | 0 | 1 | 1 | 0 | 0 | ? | 0 | 0 | 1 | ? | ? | ? | ? | ? | 0 | 0 |

| Bits | Name | Type | Description |
|---|---|---|---|
| 8 | Audio_On | Write Only[b] | Audio power on<br>0 – UDA1341, MIC and DAA power off<br>1 – UDA1341, MIC and DAA power on<br>Must be programmed to 0 when system goes to sleep.<br>Note that the UCB1300 has its own internal power down modes and is not controlled by this signal. |
| 9 | Light | Write Only[b] | Backlight<br>0 – Backlight off<br>1 – Backlight on<br>Must be programmed to 0 when system goes to sleep |
| 10 | LCD12or16 | Write Only[b] | LCD 12bpp or 16bpp output select<br>Configures the PZ3128 CPLD to map the SA-1110 LCD data pins as 12 bit RGB444 or 16 bit RGB565.<br>0 – 12RGB<br>1 – 16RGB |
| 11 | LCD On | Write Only[b] | LCD power on<br>0 – LCD and control logic power off<br>1 – LCD and control logic power on<br>Must be programmed to 0 when system goes to sleep |
| 12 | RS232En | Write Only[b] | RS 232 transceiver enable<br>Controls power on RS232 level converters.<br>0 – RS232 force power off<br>1 – RS232 enable auto power on<br>Must be programmed to 0 when system goes to sleep |
| 13 | D9_LED | Write Only[b] | Red LED<br>0 – LED on<br>1 – LED off<br>Application dependant. General application usage. May be used by developers as general-purpose indicator or as a scope trigger.<br>Must be programmed to 1 when system goes to sleep. |
| 14 | D8_LED | Write Only[b] | Green LED<br>0 – LED on<br>1 – LED off<br>Application dependant. General application usage. May be used by developers as a general-purpose indicator or as a scope trigger.<br>Must be programmed to 1 when system goes to sleep. |

## Table 4-6. Board Control Register (Sheet 3 of 4)

**0x1200,0000 — Board Control Register — SA-1110 Evaluation Module**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Reserved | | | | | | | | Spk_Off | Rad_On | Qmute | IRDECODE | I2CENAB | Rad_WU | COM_RTS | COM_DTR | Vib_On | D8_LED | D9_LED | RS232En | LCD On | LCD12or16 | Light | Audio_On | CF_Bus_On | Stereo_LB | IRDA_MD[1:0] | | IRDA_FSEL | SOFT_RST | CF_RST GFX_RST | CF_PWR NEP_RST |
| Reset[a] | ? | ? | ? | ? | ? | ? | ? | ? | 1 | 0 | ? | ? | ? | ? | ? | ? | 0 | 1 | 1 | 0 | 0 | ? | 0 | 0 | 1 | ? | ? | ? | ? | ? | 0 | 0 |

| Bits | Name | Type | Description |
|---|---|---|---|
| 15 | Vib_On | Write Only[b] | Vibration motor (quiet alert)<br>0 – Motor off<br>1 – Motor on<br>Must be programmed to 0 when system goes to sleep.<br>This device uses significant power and should be used sparingly to conserve battery usage. |
| 16 | COM_DTR | Write Only[b] | COMport Data Terminal Ready<br>Must be programmed to 0 when system goes to sleep |
| 17 | COM_RTS | Write Only[b] | COMport Request To Send<br>Must be programmed to 0 when system goes to sleep |
| 18 | Rad_WU | Write Only[b] | Radio wake up interrupt<br>0 – No interrupt<br>1 – Interrupts CPU in radio module<br>Must be programmed to 0 when system goes to sleep |
| 19 | I2CENAB | Write Only[b] | I2C Switch Enable<br>0 – Off<br>1 – On<br>Must be set to zero to allow compact flash cards to function |
| 20 | IRDECODE | Write Only[b] | IR Decode Enable<br>0 – Off<br>1 – On<br>Must be set to zero to allow IRDA to function |
| 21 | Qmute | Write Only[b] | Quick Mute<br>0 – Audio on<br>1 – Audio mute |

**Table 4-6. Board Control Register (Sheet 4 of 4)**

**0x1200,0000 — Board Control Register — SA-1110 Evaluation Module**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Reserved | | | | | | | | Spk_Off | Rad_On | Qmute | IRDECODE | I2CENAB | Rad_WU | COM_RTS | COM_DTR | Vib_On | D8_LED | D9_LED | RS232En | LCD On | LCD12or16 | Light | Audio_On | CF_Bus_On | Stereo_LB | IRDA_MD[1:0] | | IRDA_FSEL | SOFT_RST | CF_RST GFX_RST | CF_PWR NEP_RST |
| Reset[a] | ? | ? | ? | ? | ? | ? | ? | ? | 1 | 0 | ? | ? | ? | ? | ? | ? | 0 | 1 | 1 | 0 | 0 | ? | 0 | 0 | 1 | ? | ? | ? | ? | ? | 0 | 0 |

| Bits | Name | Type | Description |
|---|---|---|---|
| 22 | Rad_On | Write Only[b] | Radio Power On<br>0 – Radio power off<br>1 – Radio power on<br>Must be programmed to 0 when system goes to sleep.<br>This device uses significant power and should be used sparingly to conserve battery usage. During transmission the radio may consume 10 times more power then the rest of the system. |
| 23 | Spk_Off | Write Only[b] | Speaker Off<br>0 – Speaker amplifier power on<br>1 – Speaker amplifier power off<br>Must be programmed to 1 when system goes to sleep<br>This device may use significant power and should be used sparingly to conserve battery usage. |
| 31:24 | Reserved | — | — |

a. A question mark (?) indicates that this value is unknown at reset.
b. The values written to these bits are not readable. A record of them must be maintained by software.

## 15. Board Status Register Table 4-7

Added reset values to Table 4-7. Table 4-7 now appears as follows

*Note:* The BSR is updated ***after*** each read to the BSR—to capture the present value of the BSR, two consecutive read operations are required.

### Table 4-7. Board Status Register

**Physical Address** **32-Bit Register** **SA-1110 Evaluation Board**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Rad_RI | Rad_DCD | Rad_DSR | Rad_CTS | COM_DSR | COM_CTS | COM_DCD | RS232_Valid | Reserved | | | | | | | | | | | | | | | | | | | | | | | |
| Reset[a] | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? |

| Bits | Name | Type | Description |
|---|---|---|---|
| 23:0 | Reserved | Read only[b] | — |
| 24 | RS232_ Valid | Read only[b] | MAX3244 RS232 transceiver detects a valid RS232 level |
| 25 | COM_DCD | Read onlb[b] | COM port Carrier Detect[c] |
| 26 | COM_CTS | Read only[b] | COM port Clear To Send |
| 27 | COM_DSR | Read only[b] | COM port Data Set Ready |
| 28 | Rad_CTS | Read only[b] | Radio port Clear To Send |
| 29 | Rad_DSR | Read only[b] | Radio port Data Set Ready |
| 30 | Rad_DCD | Read only[b] | Radio port Carrier Detect |
| 31 | Rad_RI | Read only[b] | Radio port Ring Indicator |

a. A question mark (?) indicates that this value is unknown at reset.
b. The values written in this bit are readable, but cannot be modified by software.
c. Not implemented in Phase 5, always reads 0.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