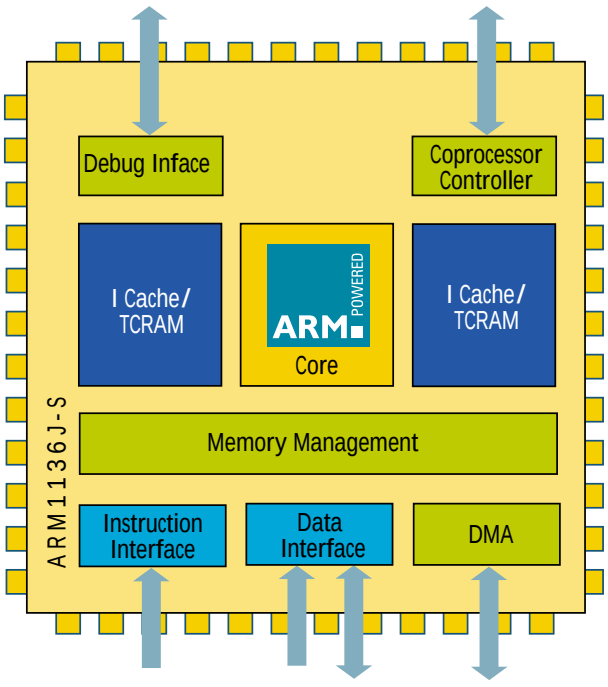
400 MHz ARM1136J-S™ High Performance Processor Core

OVERVIEW

LSI Logic offers the ARM1136J-S™ processor core synthesized onto our G*flx*™ 0.11 micron (drawn) high performance process technology, supporting clock frequencies of up to 400 MHz.

The ARM1136J-S macrocell, licensed from ARM® Limited, is a fully synthesized processor core featuring an industry leading combination of high-performance, low-power, small size, and high code density, to addresss next generation high performance SoC applications. The high performance 8-stage pipeline 32-bit RISC core has extensive 64-bit bussing, and includes Jazelle™ technology from ARM for Java acceleration. The LSI Logic G*flx* implementation of the ARM1136J-S core has 16K byte instruction and data caches, 16K/16K instruction and data tightly coupled memories (TCMs), and a memory management unit (MMU). The TCMs of the ARM1136J-S support a new optional SmartCache mode of operation whereby they can be automatically loaded from any contiguous external memory space just by supplying the appropriate memory base address. In conjunction with the ARMv6 AMBA byte lane strobe extensions, the ARM1136J-S core supports unaligned data access. Words and halfwords can be aligned to any byte boundary, enabling access to compacted data structures without any software overhead. The core has quad 64-bit AMBA™ AHB-Lite instruction and data system interfaces, a separate 32-bit AHB interface available for dedicated peripherals, and a separate vector



ARM1136J-S High Performance Processor Core

PERFORMANCE FEATURES

- 400 MHz G*flx* ARM1136J-S processor core [1] [2]
  - LSI Logic G*flx* 0.11 micron (drawn) 1.2V process technology
  - 16K/16K Byte instruction and data caches
  - 16K/16K instruction and data TCM memories with optional SmartCache operation
  - 0.6 mW/MHz power dissipation [2]

ARCHITECTURE

- High performance 8-stage pipeline 32-bit processor
- Powerful ARMv6 ISA supporting the ARM, Thumb, DSP, and Java instruction sets
- Six 64/32-bit system interfaces to meet high bandwidth requirements
- Full MMU support for Windows® CE, Linux, Palm OS®, Symbian OS™, and Java OS
- Direct-attach vector interrupt controller interface for improved interrupt response
- Unaligned data access support
- EmbeddedICE-RT™ logic for real-time debug

Notes:
[1] Worst case conditions

LSI LOGIC®

400 MHz ARM1136J-S™ Processor Core

interrupt controller (VIC) interface. The ARM1136J-S core implements the powerful ARMv6 instruction set and includes an enhanced 16 x 32-bit multiplier for optimal support of the ARM DSP extensions.

LSI Logic is a leading supplier of the most complex ASIC SoC solutions, with over 20 years in the industry and more than 20,000 ASIC designs behind us. Our extensive CoreWare® intellectual property (IP) offering includes a full range of ARM, MIPS® and ZSP™ DSP cores, a broad range of peripherals and application specific IP, reference designs, platforms, and comprehensive integration support.

FUNCTIONALITY

The ARM1136J-S processor features:

- High Performance Integer Processor
  - 8-stage integer pipeline to support clock frequencies up to 400 MHz
  - Separate load-store and arithmetic pipelines
  - Branch Prediction and Return Stack
  - Integral EmbeddedICE-RT logic
  - External coprocessor support
  - Dedicated vectored interrupt interface and low-latency interrupt mode for fast real-time performance
  - Real-time trace support
- High Performance Memory System
  - 16k Byte Instruction and Data Caches, including a non-blocking Data Cache with Hit-Under-Miss (HUM)
    - Caches are virtually indexed and physically addressed
    - 64-bit interfaces to both caches
    - Bypassable write buffer
  - Level One Tightly-Coupled Instruction and Data Memory (TCM) for use as local RAM with DMA, or as SmartCache
  - Instruction and Data Memory Management Units (MMUs), managed using Micro-TLB structures backed by a unified main TLB
  - Multiple high-performance 64-bit memory system AMBA interfaces for high-bandwidth requirements
  - Unaligned data access support in conjunction with ARMv6 AMBA byte lane strobe extensions
  - ARMv6 memory system architecture accelerates OS context-switch by up to 70%
- Powerful ARMv6 Instruction Set Architecture
  - ARM Thumb® instruction set reduces memory bandwidth and size requirements by up to 35%
  - Industry-leading Jazelle™ technology for 8x Java performance acceleration
  - ARM DSP extensions
  - SIMD (Single Instruction Multiple Data) media processing extensions

For more information please call:

LSI Logic Corporation
North American Headquarters
Milpitas, CA
Tel: 866 574 5741

LSI Logic Europe Ltd.
European Headquarters
United Kingdom
Tel: 44 1344 426544
Fax: 44 1344 481039

LSI Logic KK Headquarters
Tokyo, Japan
Tel: 81 3 5463 7165
Fax: 81 3 5463 7820

LSI Logic web site
www.lsilogic.com

LSI Logic logo design is a registered trademark of LSI Logic Corporation. ARM and Thumb are registered trademarks of ARM Limited. ARM1136J-S, Jazelle, AMBA, and EmbeddedICE-RT are trademarks of ARM Limited. MIPS is a registered trademark of MIPS Technology Inc. Java is a trademark of Sun Microsystems. Symbian OS is a trademark of Symbian Ltd. All other brand names and product names may be trademarks of their respective companies.

LSI Logic Corporation reserves the right to make changes to any products and services herein at any time with out notice. LSI Logic does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing by LSI Logic; nor the purchase, lease, or use of a product or service from LSI Logic convey a license under any patent, copyright, trademark rights, or any other of the intellectual property rights of LSI Logic or of third parties.

Copyright ©2003 by LSI Logic Corporation.
All rights reserved.

303.A.SR.W

LSI LOGIC®