ARM®

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JAZELLE™ TECHNOLOGY

For Java™ Applications

jazelle™

In the rapidly developing market for Java enabled appliances, ARM® Jazelle technology offers a unique combination of high performance, low system cost and low power demand, that cannot be matched by JIT compilation, coprocessor or dedicated Java-processor methods.

ARM Jazelle technology provides an extension to the world's leading 32-bit embedded RISC architecture, enabling ARM processors to execute Java bytecode directly in hardware and delivering unparalleled Java performance on the ARM architecture. Platform developers now have the freedom to run Java applications alongside established OS, middleware and application code — all on a single processor.

Typical Jazelle Technology Applications

Wireless

- Voice handset, smartphone, communicator and PDA devices with connection to Java-enabled m-commerce, games or information services

Home Entertainment

- Set-top box, home gateway and internet appliances offering Java-enabled shopping, banking, e-commerce, games and information services

Home Automation

- Intelligent appliances, building management systems, security, heating/cooling

Automotive

- Driver information, delivery of local guides and information
- Audio / video entertainment systems

Features

- High-efficiency Java bytecode execution, >1000 Caffeine Marks @ 200MHz
- Ultra-low Java system cost
- Low power consumption for battery operated wireless embedded devices
- Single chip MCU, DSP and Java solution
- No duplication of on-chip memory, bussing, debug or trace resources
- ARM support code causes no increase in VM size
- Java JIT compiler performance without the disadvantages
- Integrated into a number of ARM CPU cores
- Complete development kit including documentation and reference
- Run existing OS and middleware
- Supported by leading OS
- Supports leading Java run-times
- Rapid ASIC or ASSP integration with reduced time-to-market

	Expected CaffeineMark Performance CM/MHz	Estimated Energy Efficiency mJoules/CM	Integrated Development Environment	Additional Memory Burden	Additional Hardware Implementation Cost	Legacy Code/ RTOS Support
SUN Standard JVM (on ARM9)	0.7	Poor	✗	Zero		✓
ARM Optimized JVM (on ARM9)	1.7	Good	✓	Zero		✓
JIT Compiler	6.2[1]	Good[1]	✗	>100KB[2]		✓
Dedicated Java Processor	2.8	Fair	✗	>16KB	>100k Gates	✗
Co-processor	2.9	Fair	✗	>16KB	>60k Gates	✓
ARM Jazelle	6.0	Excellent	✓	Zero	12k Gates	✓

1 Subject to compile overhead 2 Plus RAM cache

Performance Without Penalty

High Performance

Jazelle technology offers significantly improved performance when compared to typical software JVMs. This improvement is achieved by accelerating some 95% of executed bytecodes directly in Jazelle hardware, while less frequently used bytecodes are supported with highly optimized sequences of ARM instructions. This delivers a performance figure of 6.0 CM/MHz representing more than 1000 CaffeineMarks in a typical 200MHz 0.18µm reference implementation.

Low Silicon Cost

ARM Jazelle technology has been engineered for minimum system cost. The hardware bytecode decoder logic is implemented in less than 12k gates — much smaller than dedicated processors or co-processors that typically consume 60k to 100k gates. Similarly, Jazelle does not require the additional memory resources demanded by JIT techniques. Jazelle achieves a single-chip MCU, DSP and Java capable solution that allows full reuse of all on-chip memory, bussing, debug and trace resources.

Compact Memory Footprint

The Jazelle technology support code replaces part of the standard JVM code without increasing the overall size of the virtual machine. This extraordinary level of efficiency, combined with the minimal gate count, makes Jazelle technology ideal for products where low system cost is of paramount importance.

Jazelle technology acceleration of Java execution approaches the performance levels achieved with just-in-time (JIT) compilation techniques — but without the associated penalties. A JIT compiler typically consumes a memory footprint of 100 KBytes and then demands RAM cache as the compiled code expands by a factor of up to 8 times.

Low Power Consumption

The Jazelle technology-enabled core uses 87% less energy per CaffeineMark than an equivalent non-accelerated ARM core. This figure is at least 10 times better than co-processor solutions and far less than JIT compilation techniques that are CPU intensive with correspondingly higher power demands.

Ease of System Integration

Jazelle technology is fully integrated into the industry-leading ARM RISC architecture and is completely compatible with the ARM interrupt and exception model — giving easy design and integration with existing operating systems, Java run-times, middleware and applications. These factors, together with rapid single processor ASIC or ASSP integration, allow a short time-to-market and make Jazelle technology the ideal solution for phones, appliances and home-gateway products.

Real-Time Performance

Applications like home gateway and phone solutions demand excellent real-time performance from a processor to run the network protocol software and middleware. The Jazelle architecture extensions enable the processor to maintain fast interrupt response and provide real-time performance.

Jazelle Technology Enabled Cores

ARM has integrated Jazelle technology into two cores: the ARM926EJ-S™ and the ARM7EJ™, and has integrated the technology into the ARM10™ family of cores, to provide a fully compatible roadmap for Jazelle technology-enabled products.

The ARM926EJ-S soft macrocell is a fully synthesizable, high-performance 32-bit RISC processor comprising a Jazelle technology-enhanced processor core, instruction and data caches, tightly coupled memory (TCM) interfaces, memory management unit (MMU), and separate instruction and data AMBA™ AHB bus interfaces.

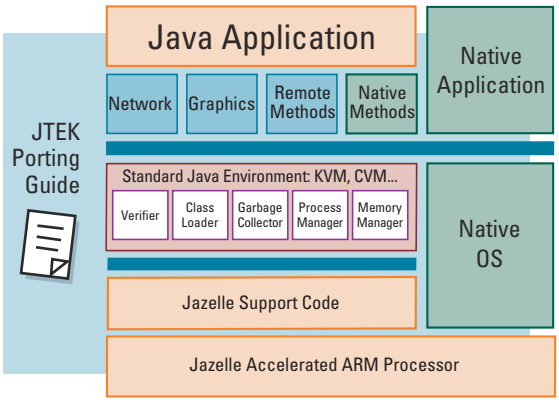
The size of the instruction and data cache, and instruction and data TCMs can all be independently selected, providing complete flexibility and enabling the ARM926EJ-S solution to be tailored to specific application needs. The MMU supports virtual memory based platform operating systems such as the Symbian Platform, Linux and Windows CE.

The ARM926EJ-S solution provides system designers running platform operating systems access to a portable and flexible product in the ARM9™ family performance range in a single CPU core. The solution offers complete compatibility with existing operating systems, application code, and the ability to compile performance-critical applications (e.g. graphics libraries) for execution in native mode. Ideal for home entertainment, smartphones and PDA applications.

The ARM7EJ solution is a compact CPU without cache memory, specifically designed for applications demanding the lowest power consumption and where absolute performance is less critical. It has a memory interface identical to that of the ARM7TDMI-S™, and features an enhanced multiplier design for improved DSP performance. Ideal for Java-enabled voice handsets, intelligent appliances and home automation applications.

The Jazelle Technology/Virtual Machine Interface

Jazelle technology-enabled cores are complemented by Jazelle Support Code that manages the interface between the core hardware, the virtual machine and the operating system.



The Jazelle Support Code, which will only be available to Sun licensees, permits the virtual machine to access the full benefits of Jazelle technology by replacing the interpreter and invoker methods within the VM. The support code is highly optimized for both speed and size and greatly simplifies the task of porting a virtual machine to the Jazelle platform.

The Jazelle Technology Enabling Kit (JTEK) comprises all the necessary support code source, documentation and tools that are required to integrate Jazelle technology into a virtual machine and operating system. JTEK is available for CLDC and CDC, and can be ported to all popular OS.

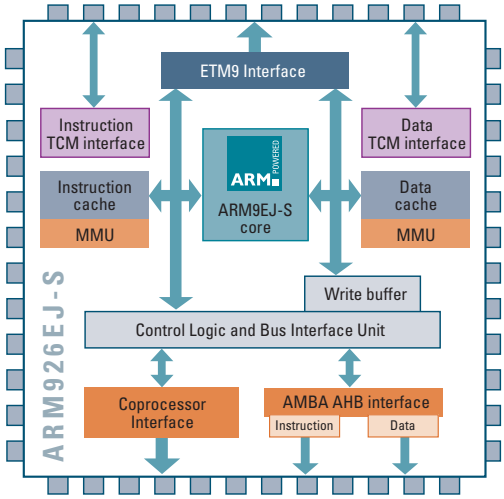
ARM processors traditionally support two instruction sets; ARM state, with 32-bit instructions and Thumb state which compresses the most commonly used instructions into 16-bit format. The Jazelle technology extends this concept by adding a third instruction set, Java bytecode, to the capability of the processor, together with a new Java state.

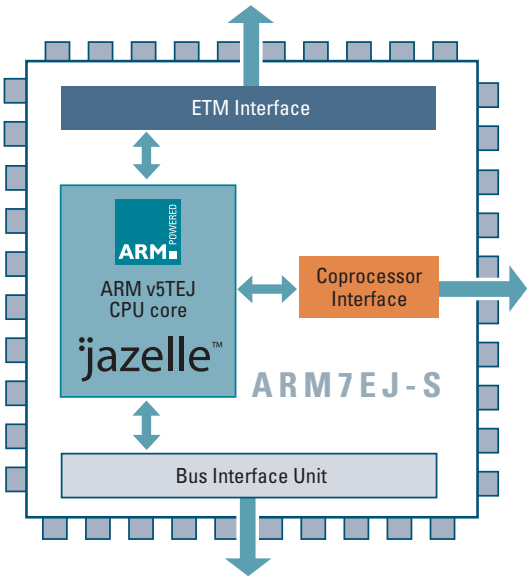
When presented with Java bytecode, the Jazelle Support Code switches the processor into Java state using a dedicated branch instruction. In Java state, the processor reassigns several ARM registers to accommodate Jazelle machine state and Java operands — ensuring compatibility with existing operating systems, interrupt handlers and exception code. Up to four stack elements are maintained in ARM registers to reduce memory access to a minimum; this is an important contributor to the excellent performance of the processor when executing a Java application. Stack spill and underflow is handled automatically by the hardware.

Minimum interrupt latency is maintained across both ARM state and Java state. Since bytecode execution can be restarted, an interrupt automatically triggers the core to switch from Java state to ARM state for the execution of the interrupt handler. This means that no special provision has to be made for handling interrupts while executing bytecode — whether in hardware or software.

Product Roadmap

The Jazelle Support Code provides a simple, progressive method for integrating Jazelle technology into any system. The VMA support code achieves excellent levels of Java performance with non-Jazelle cores by using software Java acceleration. When a Jazelle enabled core with hardware Java acceleration is targeted, then the VMZ version of the support code is used to enable maximum Java performance. This permits a phased approach where by existing designs can be transferred to the full benefits of Jazelle technology.





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Development Tools Support

As a part of ARM's ongoing commitment to provide the development community with the tools required to develop and debug applications and systems on ARM based cores, ARM is developing extensions to its industry leading tools suite to enable the use of the Java language on ARM accelerated VMs from ARM's Jazelle Partners.

The ARM Java Technology Pack (AJTP) is available as an add-on to ARM's Multi-ICE JTAG emulator. This allows standard Java Debuggers that support the Java Debug Wire Protocol (JDWP) to connect to ARM accelerated VMs using a standard JTAG connection. This approach enables developers to use their Java Development Tools of choice to create and debug their application over JTAG. In addition a C/C++ debugger such as ARM's AXD can be simultaneously connected to the target via the same Multi-ICE unit, allowing debug of systems software as well as Java code.

The ARM Instruction Set Simulator (ARMulator) available as part of ARM Developer Suite (V1.2 or later), has been enhanced to support the Jazelle Architectural Extension. This allows Java applications to be tested on ARM accelerated VMs available from ARM's Jazelle Partners before hardware is available.

DEBUG FOR JAVA APPLIANCES INCORPORATING KVM