TRITON™ XXS

The “extra small” XScale™ based TRITON™ module is a complete computer installed on a small board measuring just 59mm x 32mm – ideal for small space restricted, power sensitive embedded designs. TRITON™ includes a 400MHz Intel® XScale™ processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of a LCD screen, and the standard-PCMCIA-interface permits simple extension and integration into a target system.

XScale™

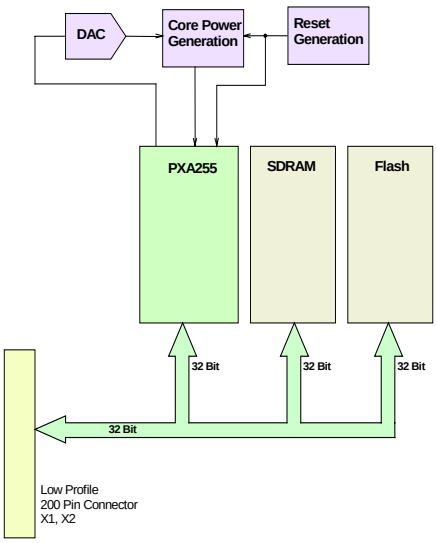
Intel's new XScale™ processor family increases efficiency and decreases processor power consumption. The Intel® XScale™ microarchitecture is based on the solid and widely used foundation of the Intel® StrongARM technology. Optimized for the development of highly efficient mobile internet devices, and for network infrastructure applications, Intel® StrongARM and Intel® XScale™ are compatible with the ARM architecture, which in turn guarantees the compatibility of software solutions.
Turbo mode enables the processor to scale its performance as high or as low as necessary in a single clock cycle, which helps conserve battery lifetime while still meeting performance requirements. In addition, the new micro-power management features for these devices allow the processors to potentially use less than half the power at the same performance levels of the Intel StrongARM SA-1110 applications processor.

Redboot™

TRITON™ is delivered with pre-installed Redboot™ firmware. Redboot™ supports several low-level-debugging options and file download via serial XModem. These files can additionally be stored into the permanent flash-memory to be started by command or power-on.

TRITON™ XXS features:

- Intel XScale™ PXA255 (400 MHz)
- 64 MByte mobile SDRAM (32-bit@100Mhz)
- 32 Mbyte Flash memory (32-bit)
- 3 asynchronous, 1 synchronous serial interfaces
- LCD controller
- PC-CARD / compact-flash interface
- I²S, AC97 interface available
- Complete 32-bit memory interface available
- JTAG interface
- Single 3,3V power supply
- Programmable Core Generator
- Min. power consumption 3.5mW (standby, 64MB SDRAM)
- Redboot™ firmware
- Ultra-Low-Profile overall dimensions 59 x 32 x 6,6mm³



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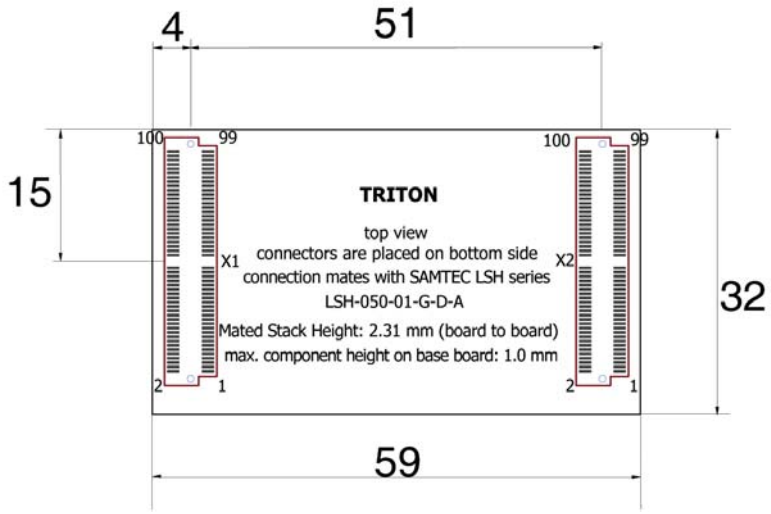
top view

rear view – LTH connectors used on TRITON



NOTE:
The pin number organization for the SAMTEC LTH connectors is different to SAMTEC's datasheet! Use the numbering scheme shown here for your designs.

Ordering information

Order Number (Valid Combination)	PXA255	SDRAM	Flash
TRITON-XXS/400/64S/32F	400MHz	64MB	32MB

The order number is formed by a combination of the elements below. Other options are possible for a minimum order quantity of 100 pieces.

TRITON-XXS/400/ 64S/ 32F/ I

I: Industrial Temperature (-40°C to 85°C)
16F: 16Mbyte Intel Strata-Flash / **32F**: 32Mbyte Intel Strata-Flash
32S: 32Mbyte SDRAM / **64S**: 64Mbyte SDRAM
200: 200MHz / **300**: 300MHz / **400**: 400MHz

X1 connector pin out

Pin	Signal	Description	Pin	Signal	Description
1	BITCLK / GPIO28	AC97 Audio Port bit clock (output)	2	nCS1 / GPIO15	Chip Select [1]
3	48MHz_GPIO7	48 MHz clock [1]	4	32kHz / GPIO12	32 kHz clock [1]
5	SDATA_IN1 / GPIO32	AC97 Audio Port data in (input)	6	GPIO3	General Purpose I/O-Pin [1]
7	ACRESET#	AC97 Audio Port reset signal (output)	8	MMCMD	Multimedia Card Command [1]
9	SDATA_OUT / GPIO30	AC97 Audio Port data out (output)	10	MMDAT	Multimedia Card Data [1]
11	GND	GND	12	GND	GND
13	SYNC / GPIO31	AC97 Audio Port sync signal (output)	14	MMCCLK / GPIO6	Multimedia Card Clock [1]
15	SDATA_IN0 / GPIO29	AC97 Audio Port data in (input)	16	PWM1 / GPIO17	Pulse Width Modulation channel 1
17	PWM0 / GPIO16	Pulse Width Modulation channel 0	18	SSPTXD / GPIO25	Synchronous Serial Port Transmit Pin
19	SSPRXD / GPIO26	Synchronous Serial Port Receive Pin	20	SSPSFRM / GPIO24	Synchronous Serial Port Frame Pin
21	SSPSCLK / GPIO23	Synchronous Serial Port Clock Pin	22	TMS	JTAG Test Mode Select
23	TDO	JTAG Test Data Out	24	TRST#	JTAG Test Reset
25	TCK	JTAG Test Clock	26	RESET_IN#	**PXA255** Reset Input [1]
27	TDI	JTAG Test Data In	28	RESET_OUT#	Reset Output
29	GND	GND	30	GND	GND
31	BATT_FAULT#	Battery Fault, switch into sleepmode	32	MMCSS0 / GPIO8	Multimedia Card chip select 0 [1]
33	GPIO0	General Purpose I/O-Pin	34	BTRXD / GPIO42	Bluetooth UART Receive Pin (3,3V-Level)
35	GPIO1	General Purpose I/O-Pin	36	BTTXD / GPIO43	Bluetooth UART Transmit Pin (3,3V-Level)
37	PIOIS16# / GPIO57	PCMCIA Interface I/O select 16 Bit	38	BTCTS / GPIO44	Bluetooth UART Clear to Send (3,3V-Level)
39	PWAIT# / GPIO56	PCMCIA Interface Wait	40	BTRTS / GPIO45	Bluetooth UART Ready to Send (3,3V-Level)
41	PSKTSEL / GPIO54	PCMCIA Interface Socket Select	42	FFRXD / GPIO34	Full Function UART Peceive Pin (3,3V-Level)
43	PIOW# / GPIO51	PCMCIA Interface I/O Write	44	FFTXD / GPIO39	Full Function UART Transmit (3,3V-Level)
45	PCE2# / GPIO53	PCMCIA Interface High Byte Enable	46	FFDCD / GPIO36	Full Function UART Carrier Detect (3,3V)
47	PIOR# / GPIO50	PCMCIA Interface I/O Read	48	FFCTS / GPIO35	Full Function UART Clear To Send (3,3V)
49	+3,3V	power supply	50	+3,3V (VCCN)	power supply (VCCN) [1]
51	+3,3V	power supply	52	+3,3V (VCCN)	power supply (VCCN) [1]
53	NSSP_RxD / GPIO84	Network SSP Receive [1]	54	FFRI / GPIO38	Full Function UART Ring Ind. (3,3V Level)
55	NSSP_CLK / GPIO81	Network SSP Clock [1]	56	FFDSR / GPIO37	Full Function UART Data Set Rdy. (3,3Vl)
57	NSSP_TxD / GPIO83	Network SSP Transmit [1]	58	FFDTR / GPIO40	Full Function UART Data Term. Rdy. (3,3V)
59	NSSP_FRM / GPIO82	Network SSP Frame Signal [1]	60	FFRTS / GPIO41	Full Function UART Rdy. To Send (3,3V)
61	GND	GND	62	GND	GND
63	USB_N	USB-Port neg. Pin (3,3V-Level)	64	L_BIAS / GPIO77	LCD bias drive
65	USB_P	USB-Port pos. Pin (3,3V-Level)	66	LDD13 / GPIO71	LCD interface data bus
67	SDA	I2C data signal	68	LDD9 / GPIO67	LCD interface data bus
69	SCL	I2C clock signal	70	LDD3 / GPIO61	LCD interface data bus
71	L_LCLK / GPIO75	LCD Interface Line Clock	72	LDD8 / GPIO66	LCD interface data bus
73	LDD1 / GPIO59	LCD interface data bus	74	L_PCLK / GPIO76	LCD Interface Pixel Clock
75	GND	GND	76	GND	GND
77	LDD2 / GPIO60	LCD interface data bus	78	LDD11/ GPIO69	LCD interface data bus
79	L_FCLK / GPIO74	LCD Interface Frame Clock	80	LDD12 / GPIO70	LCD interface data bus
81	LDD5 / GPIO63	LCD interface data bus	82	LDD10 / GPIO68	LCD interface data bus
83	LDD14 / GPIO72	LCD interface data bus	84	LDD15 / GPIO73	LCD interface data bus
85	LDD0 / GPIO58	LCD interface data bus	86	LDD7 / GPIO65	LCD interface data bus
87	GND	GND	88	GND	GND
89	LDD6 / GPIO64	LCD interface data bus	90	IR_RXD / GPIO46	IrDA Receive Pin (3,3V- Level)
91	LDD4 / GPIO62	LCD interface data bus	92	IR_TxD / GPIO47	IrDA Transmit Pin (3,3V-Level)
93	PCE1# / GPIO52	PCMCIA Interface Low Byte Enable	94	GPIO11	General Purpose I/O-Pin
95	POE# / GPIO48	PCMCIA Interface Output Enable	96	GPIO10	General Purpose I/O-Pin
97	PREG# / GPIO55	PCMCIA Interface Register Select	98	PWE# / GPIO49	PCMCIA Interface Write Enable
99	GND	GND	100	GND	GND

[1] Modified TRITON pinout used on this module)

X2 connector pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	GND	2	GND	GND
3	RD/WR#	Read not Write	4	WE#	Memory Write Enable
5	MBGNT / GPIO13	Memory Controller grant [1)]	6	OE#	Memory Output Enable
7	nSDCKE0	SMROM or synchronous Flash clock enable	8	RDY	Ready Pin (Wait)
9	SDCLK0	SMROM or synchronous Flash clock	10	nCS2	Chip Select
11	GND	GND	12	GND	GND
13	SDCLK2	SDRAM banks 2/3 clock	14	nCS3	Chip Select
15	MBREQ / GPIO14	Mem. Controller alternate bus master request [1)]	16	nCS4	Chip Select
17	nSDCS2	SDRAM Chip Select for banks 2	18	nCS5	Chip Select
19	nSDCAS	SDRAM column address strobe (CAS)	20	MD16	memory data bus
21	GND	GND	22	GND	GND
23	nSDRAS	SDRAM row address strobe (RAS)	24	MD17	memory data bus
25	DQM3	data output byte enable 3	26	MD18	memory data bus
27	DQM2	data output byte enable 2	28	MD19	memory data bus
29	DQM1	data output byte enable 1	30	MD20	memory data bus
31	DQM0	data output byte enable 0	32	MD21	memory data bus
33	GND	GND	34	GND	GND
35	MA25	Memory address bus	36	MD22	memory data bus
37	MA24	Memory address bus	38	MD23	memory data bus
39	MA23	Memory address bus	40	MD24	memory data bus
41	MA22	Memory address bus	42	MD25	memory data bus
43	GND	GND	44	GND	GND
45	MA21	Memory address bus	46	MD26	memory data bus
47	MA20	Memory address bus	48	MD27	memory data bus
49	MA19	Memory address bus	50	MD28	memory data bus
51	MA18	Memory address bus	52	MD29	memory data bus
53	GND	GND	54	GND	GND
55	MA17	Memory address bus	56	MD30	memory data bus
57	MA16	Memory address bus	58	MD31	memory data bus
59	DREQ0 / GPIO20	DMA Request Channel 0	60	DREQ1 / GPIO19	DMA Request Channel 1
61	MA15	Memory address bus	62	MD15	memory data bus
63	MA14	Memory address bus	64	MD7	memory data bus
65	MA13	Memory address bus	66	MD14	memory data bus
67	MA12	Memory address bus	68	MD6	memory data bus
69	GND	GND	70	GND	GND
71	MA11	Memory address bus	72	MD13	memory data bus
73	MA10	Memory address bus	74	MD5	memory data bus
75	MA9	Memory address bus	76	MD12	memory data bus
77	MA8	Memory address bus	78	MD4	memory data bus
79	GND	GND	80	GND	GND
81	MA7	Memory address bus	82	MD11	memory data bus
83	MA6	Memory address bus	84	MD3	memory data bus
85	MA5	Memory address bus	86	MD10	memory data bus
87	MA4	Memory address bus	88	MD2	memory data bus
89	GND	GND	90	GND	GND
91	MA3	Memory address bus	92	MD9	memory data bus
93	MA2	Memory address bus	94	MD1	memory data bus
95	MA1	Memory address bus	96	MD8	memory data bus
97	MA0	Memory address bus	98	MD0	memory data bus
99	GND	GND	100	GND	GND

[1)] Modified TRITON pinout used on this module)

Memory-Map

In the Intel PXA255 Developer's Manual you will find the memory map of the PXA255 processor on pages 2-19 and 2-20. The TRITON-XXS uses the memory as follows:

```
0xA000 0000 - 0xA3FF FFFF  64 MBytes SDRAM

0x01FC 0000 - 0x01FF FFFF  256 kBytes reserved flash area (FIS directory)
0x01F8 0000 - 0x01FB FFFF  256 kBytes reserved flash area (RedBoot config)
0x0004 0000 - 0x01F7 FFFF  31,5 MBytes flash area available
0x0000 0000 - 0x0003 FFFF  256 kBytes reserved flash area (RedBoot)
```

Note

The flash memory has an erase block size of 256 kBytes.

Internally used GPIO pins

The following PXA255 GPIO pins are internally used on the TRITON-XXS module:

GPIO number	direction	Used for …
4	Output	I²C clock pin for core voltage DAC
5	I/O	I²C data pin for core voltage DAC