Board Bring Up (BBU) Program for Intel® PXA27x Processor Developer's Kit

Software Release Notes

Release Version 1.04.006, Beta 3

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Order Number: 278960-010

Contents

1.0 Description

This package contains version 1.04.006 Beta 3 of the Board Bring Up (BBU) program for the Intel® PXA27x Processor Developer's Kit (kit), using the Intel® PXA27x processor (PXA27x processor). The BBU program is useful for providing low-level access to all registers and most peripherals as a confidence test for the kit. This program is co-resident in flash memory with the Power On Self Test (POST).
Although this software has been tested, it is to be used as EXAMPLE SOFTWARE ONLY and cannot be used "as is" for production systems. No warranty, expressed or implied, is to be associated with this software and the user assumes all risk.

Note: This release of the BBU has been validated on the Intel® PXA270 processor, the Intel® PXA271 processor and the Intel® PXA272 processor.

1.1 Kit Contents

This kit includes a self-extracting file BBU_PXA27x_V1_04_006.exe which contains:

- BBU Binary Files
  The binary version of BBU that can be programmed into either the flash memory on the Intel® PXA27x processor card (processor card) or the flash memory on the Intel® PXA27x Processor Developer's Kit Main Board (main board). There are binary files that support different processor configurations and can be found in the installation directory.
  - BBU_PXA270_128SDRAM_V1_04_006.bin
    The BBU that is programmed into the 128 MB processor or the main board flash memory that supports the C0/C5 stepping or greater of the Intel® PXA270 processor configuration (32 bit).
  - BBU_PXA270_PXA272_64SDRAM_V1_04_006.bin
    The BBU that is programmed into the 64 MB processor or the main board flash memory that supports the C0/C5 stepping of the Intel® PXA270 processor and the C0 stepping of the Intel® PXA272 processor configurations (32 bit).
  - BBU_PXA271_32SDRAM_V1_04_006.bin
    The BBU that is programmed in the 32 MB processor or the main board flash memory that supports the C0 stepping of the Intel® PXA271 processor (16 bit). See Daughter Card SW1 Settings for information on setting SW1-6 for 16-bit operation.
- RelNote_BBU_MB.pdf
  The release notes that describe this release (this file) can be found in the installation directory.
- BBU_MB_V1_04_006_Source.zip
  The source code for the BBU programs.
- SWLicense.pdf
  A copy of the general software End-User License Agreement (EULA) can be found in the installation directory.

1.2 Related Documentation

Related documentation for this kit includes:

- *Intel® PXA27x Processor Developer's Kit User's Guide* – a complete list of all related documentation, including a manufacturer's data sheet for each device, in the Related Documents section of the Introduction and Startup chapter. The Diagnostics section contains a complete description of the BBU program.
- *Flash Memory Programmer for Intel Development Platforms Release Notes* – details of the JFlashMM software.
- *Intel® XDB JTAG Debugger for Intel® JTAG Cable User's Manual* – This document describes how to use the Intel® XDB JTAG Debugger to download images into the kit flash memory. It also provides hardware and software requirements for performing this operation.

For these documents plus the latest software and hardware updates, contact your Application Engineer (AE).

1.3 Software Required

The following software is required:

- JFlashMM 5.01.007 or higher, or the Intel® XDB JTAG Debugger
- HyperTerminal* or Tera Term Pro* installed on your PC

1.4 Supported Hardware Revisions

The stepping of the processor card can be viewed from Coprocessor 15 Register 0 – ID Register Definition by using the BBU PID command. The stepping of the processor card is also reported by the JFlashMM utility on any access to the kit. The image has been tested with the following kit specifications as shown in Table 1.

Table 1 Kit Specifications

Main Board Revision	Main Board ECO Revision	Daughter Card Revision	Daughter Card ECO Revision	Intel® PXA27x Processor Stepping	PMIC Card Revision	PMIC ECO Revision
2.1	C	1.2	E	PXA270 C0, C5 PXA271 C0 PXA272 C0	1.2	D

2.0 Known Problems

- **Problem:** The KEYP command may not decode all of the keys correctly while in key function mode. However, register dump mode does decode all of the keys correctly.
  Workaround: None.
- **Problem (Intel® PXA270 processor C5 stepping and Intel® PXA271 processor only):** The system hangs when using the Initialize System Clocks command (`ISCS`) when the BBU is running from SDRAM. The `ISCS` command functions properly when the BBU is running out of flash memory.
  Workaround: None.

3.0 Hardware Required

The following hardware is required:

- Intel® JTAG Cable assembly
- DB-9 Null-Modem serial cable

All applicable ECOs must be applied in order for the software to operate properly.

4.0 Procedure

The following procedures assume that the CPLD code and FPGA code have been pre-programmed on the kit.

There are two banks of flash memory on the kit. One bank is on the processor card and the other is on the main board. The JFlashMM software is used for programming the flash memory. Intel recommends that the BBU software be installed on the flash memory of the processor card.

Note: The kit has a BBU and POST co-resident in flash on the processor card. The BBU and the POST program can be executed through commands or by switch settings shown in Factory Default Switches and Setup for the Kit.

4.1 Testing Environment Setup

The following procedure, which only needs to be performed once, is required to set up the testing environment.

4.1.1 Flash Programming Software

Two applications can be used for programming the flash memory with BBU image. The easiest method is to use JFlashMM. Another method, which has a speed advantage, is to use the Intel® XDB JTAG Debugger for Intel® JTAG Cable.

4.1.1.1 Pointer to the JFlashMM Software

For more information on JFlashMM software refer to the *Flash Memory Programmer for Intel Development Platforms Release Notes*. Run the downloaded software to install the JFlashMM software on your PC.

4.1.1.2 Pointer to the Intel® XDB JTAG Debugger

You can use Intel® XDB JTAG Debugger for programming the flash memory. Contact your AE or local service organization for information about how to obtain this software and the related documentation.

4.1.2 HyperTerminal* Setup

HyperTerminal is a terminal emulator that is normally installed on your PC. It is used as the primary I/O device for BBU. This version of BBU has a selectable baud rate and port selection for the terminal. Create a terminal setup with the following characteristics as shown in Table 2.

Table 2 Hyper Terminal Settings

Setting	Value
Baud Rate	115,200 or 9,600 baud
Data Bits	8
Parity	None
Stop Bits	1
Flow Control	None

Note: As an alternative to HyperTerminal, many users prefer Tera Term Pro* which is a popular freeware terminal emulator that works very well with BBU and POST. Tera Term Pro V2.3 (or later) may be downloaded from the Internet.

4.2 Factory Default Switches and Setup for the Kit

Refer to the following sections for the appropriate switch settings for the kit.

4.2.1 Serial Communications for the BBU

Connect the DB-9 Serial connection to the FFUART on the processor card or the BTUART on the main board. See the SW18 setting in table 3.

4.2.2 Default Switch Setup

The default switch settings for the BBU/POST, Daughter Card SW1 Positions, and Daughter Card SW2 Positions are described in the following sections.

4.2.2.1 BBU/POST Switch Settings

Table 3 describes the switches relevant to BBU or POST. The factory default settings are required for a standard execution of the BBU. For a comprehensive list of all switches, see the *Intel® PXA27x Developer's Kit User's Guide*.

Note: The BBU will also run standalone on the daughter card. When the main board is not present, the BBU communicates over the FFUART at 9600 baud and the core bus frequencies run at their Power On Reset (POR) values.

Table 3 BBU/POST Default Switch Settings

Switch ID	Description	Default Setting	Action
SW5	IrDA	DOT	Connects the IrDA circuitry to the controller.
SW8	Flash Width Select	DOT	Must be set to the DOT position.
SW7	SWAP Flash	DOT	DOT=Daughter Card Flash NO DOT= Main Board Flash
SW09	FPGA_RESET	DOT	Run
SW10	NBATT_Fault	DOT	Normal
SW11	nVDD_Fault	DOT	Normal
SW12	Operating Frequency for BBU	A	See the SW12+SW13 switch settings table in the *Intel Diagnostics for Intel® PXA27x Processor Developer's Kit User's Guide* for more information.
SW13	Operating Frequency for BBU	D	See the SW12+SW13 switch settings table in the *Intel Diagnostics for Intel® PXA27x Processor Developer's Kit User's Guide* for more information.
SW14	Fast Bus Select	NO DOT	DOT = normal memory bus operation NO DOT = Fast Bus operation.
SW15	SDCLK Select	DOT	DOT = MClk/2 NO DOT = MClk
SW16	Turbo Mode	NO DOT	DOT = Turbo mode off NO DOT = Turbo mode on
SW17	Alternate Boot	NO DOT	DOT = Boot POST NO DOT = Boot BBU
SW18	Alternate I/O	DOT	DOT = FFUART for I/O NO DOT = BTUART for I/O
SW19	Alternate Baud Rate	DOT	DOT = 115200 Baud NO DOT = 9600 Baud (must be in DOT position to be compatible with POST)

4.2.2.2 Daughter Card SW1 Settings

Table 4 identifies the default settings for each of the switches in SW1 on the daughter card.

Table 4 Daughter Card SW1 Default Switch Settings

Switch ID	Default Setting	Description
SW1-8	On	On = Intel® PXA27x processor clock is from PXTAL (Crystal or OSC) Off = Intel®PXA27x processor clock is from CLK_PIO
SW1-7	Off	On = Communications processor internal boot Off = Communications processor external boot
SW1-6	On	On = Intel® PXA270 processor or Intel®PXA272 processor boots in 32-bit mode Off = Intel® PXA271 processor boots in 16-bit mode
SW1-5	On	On = Flash Memory Bank Off = Image Memory Bank
SW1-4	Off	On = Communications processor MSL Baseband is connected Off = Communications processor MSL Baseband is not connected
SW1-3	On	General purpose switch for CPLD configuration
SW1-2	Off	On = Connect Communications Processor nCS1 to SRAM1 and SRAM2. Off = Connect Communications Processor nCS1 to SRAM1 and nCS2 to SRAM2
SW1-1	On	On = Intel® JTAG chain connections are determined by JTAG_SEL (SW2). Off = Intel® JTAG chain is connected to CPLD1.

4.2.2.3 Daughter Card SW2 Settings

Table 5 identifies the default settings for each of the switches in SW2 on the daughter card.

Table 5 Daughter Card SW2 Default Switch Settings

SW2-1	SW2-2	Description
On (default)	On (default)	Intel® JTAG chain is connected to Intel® PXA27x processor
On	Off	Intel® JTAG chain is connected to the Communications Processor
Off	On	Intel® JTAG is connected to Intel® PXA27x processor and the Communications Processor
Off	Off	Intel® JTAG chain is connected to Intel® PXA27x processor, Communications Processor, CPLD2, EEPROM, and the FPGA

4.2.3 Flash Programming Setup

There are two images normally programmed into the flash memory on the processor card. The BBU is programmed at address 0, and may be run without POST being loaded into flash memory. POST is programmed to start at address 0x40000.

4.2.3.1 Intel® XDB JTAG Debugger for Intel® JTAG Cable

Connect the Intel® JTAG Cable assembly from your PC parallel port to the JTAG TAP (J4) on the daughter card. Refer to the *Intel® XDB JTAG Debugger for Intel® JTAG Cable User's Manual* for instructions on using the flash memory programming plug-in.

4.2.3.2 JFlashMM

To program your flash memory, connect the Intel® JTAG Cable assembly from your PC parallel port to the JTAG TAP (J4) on the daughter card. Refer to the *Flash Memory Programmer for Intel Development Platforms Release Notes* for information on using JFlashMM.

- The BBU binary is programmed at the default location of address 0. JFlashMM defaults to address 0 and does not require a parameter for this address.
- The BBU binary is programmed at address 0 using the following command (32 bit):

```
>JFlashmm bulbcx BBU_PXA270_PXA272_V1_04_006.bin
```

4.2.4 Running the BBU Program

The BBU program executes upon kit power up and messages appear on the terminal emulator application. The HEX LEDs on the main board will display "0000 0000" when the BBU code boots.

Once the BBU prompt appears (`bbu>`), the program is ready to accept commands from the user.

5.0 Command Summary

A command summary is available from the BBU program by typing `help`. Commands may be in any combination of upper and lower case characters. The `delete` (backspace) key allows you to correct mistyped commands.

For a complete list of all BBU commands, refer to the Diagnostics section of the *Intel® PXA27x Processor Developer's Kit User's Guide*.

6.0 Changes for Release 1.04.006

- Changed the address where the boot ROM is mapped to when the BBU is moved into SDRAM from 0x0400_0000 to 0x1800_0000 to support platforms with 128 MB of SDRAM.
- Changed the address where the alternate boot ROM is mapped to when the BBU is moved into SDRAM from 0x0C00_0000 to 0x1C00_0000 to support platforms with 128 MB of SDRAM.
- Added the `CBUF` command that enables/disables a BBU command recall buffer. When enabled, the user can recall a previously typed BBU command by pressing the up/down arrows on the terminal emulator.
- Added an optional parameter to the `MSG1` command that allows the user to change the default background color on the LCD from blue to any 16-bit color by typing in any value from 0x0 to 0xFFFF.

7.0 Build Instructions

- The BBU source files included in this kit were used to build the BBU binary files using the Intel® C++ Software Development Tool Suite for Palm* OS, Symbian* OS, Nucleus* OS, and OS-Independent Systems (Tool Suite).
- Be sure to use the path names exactly as they were extracted from the zip file. The build file for BBU is located in `C:\Bulverde\BBU_Programs\MSBBUP` and has the file name `MSBBUP.NWW`. Clicking on this file name will start the Tool Suite.
- To prepare to build the Intel® PXA270 processor and Intel® PXA272 processor versions of BBU, click on `Tools` then `Build Manager`. In the Buildmode box select the `MSBBUP` option.
- To prepare to build the Intel® PXA271 version of BBU, click on `Tools` then `Build Manager`. In the Buildmode box select the `PXA271` option.
- To build the selected BBU program, click on `Project` then `Rebuild All`.
- The BBU binary file will be found in directory: `C:\Bulverde\BBU_Programs\MSBBUP\MSBBUP` or `C:\Bulverde\BBU_Programs\MSBBUP\PXA271` depending on the buildmode selected above.