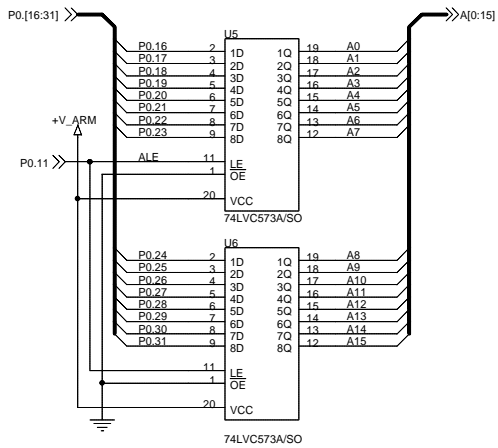
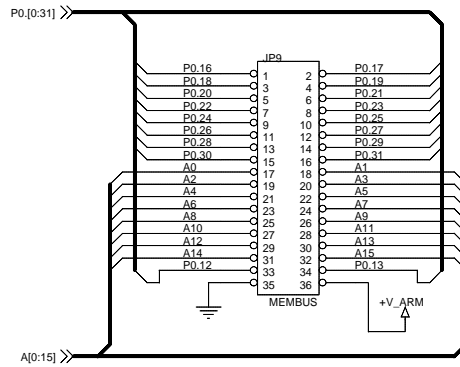


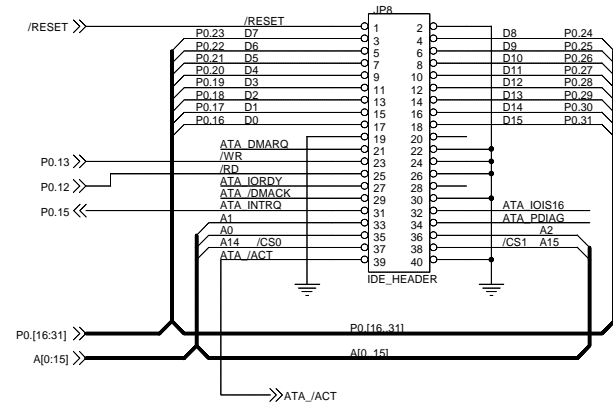
MEMORY BUS ADDRESS LATCH



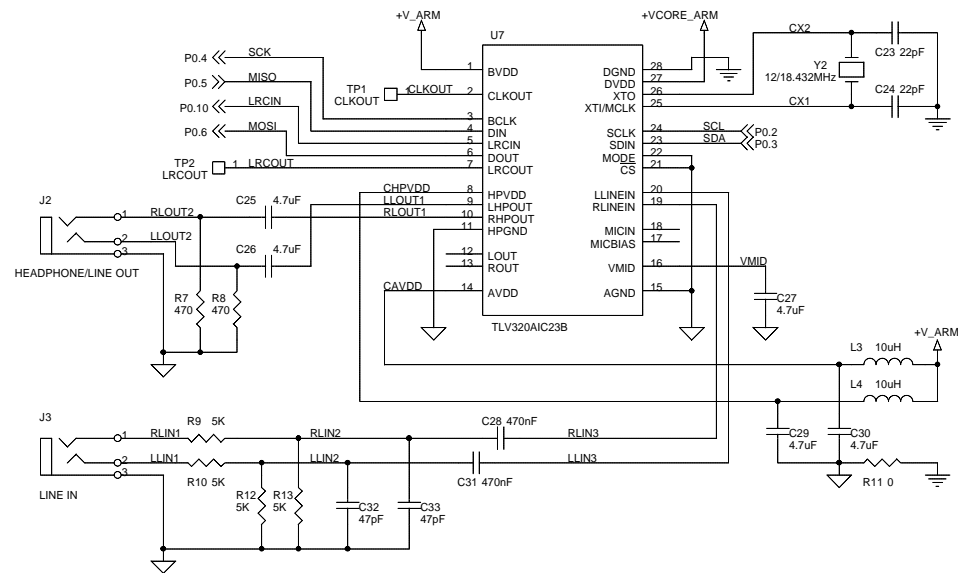
MEMORY BUS INTERFACE



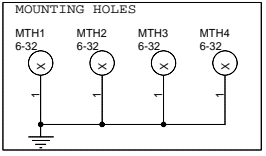
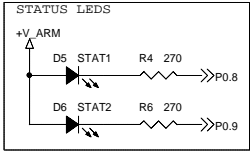
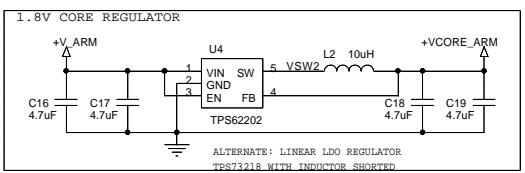
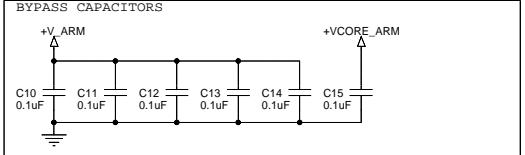
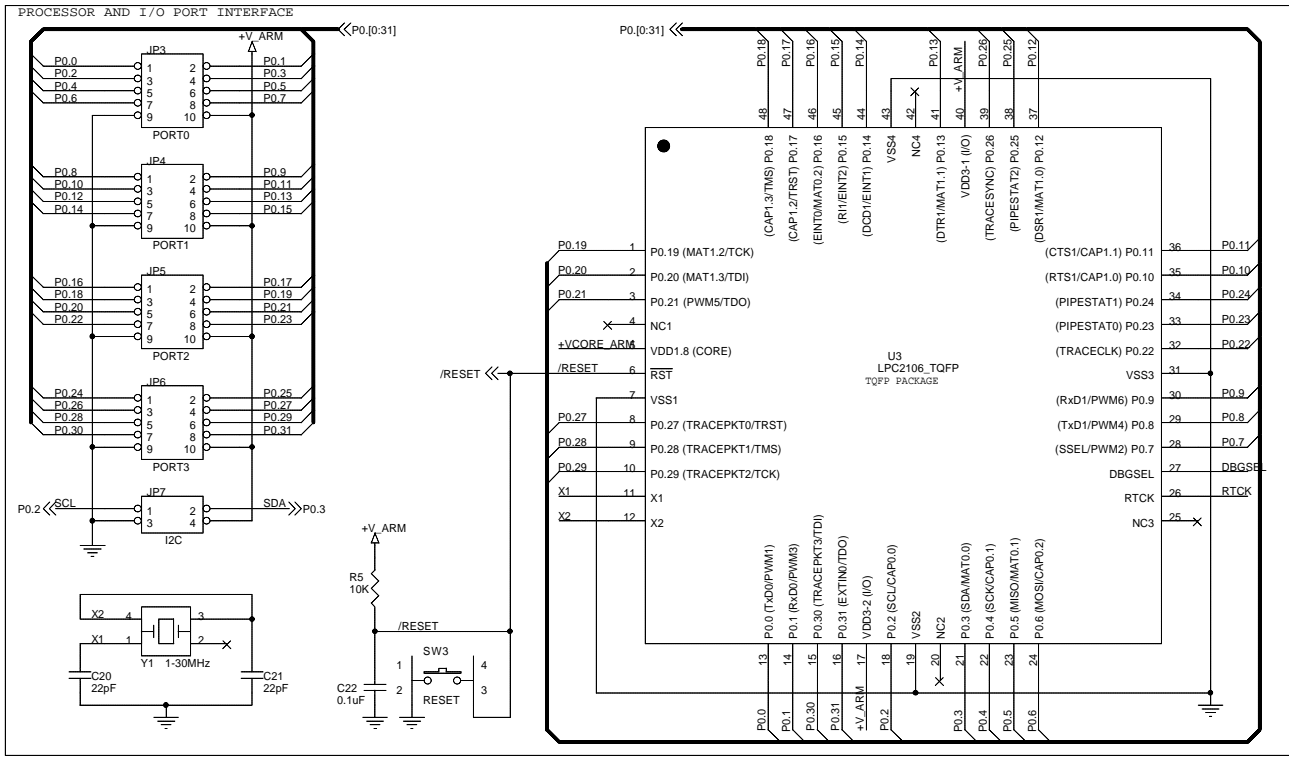
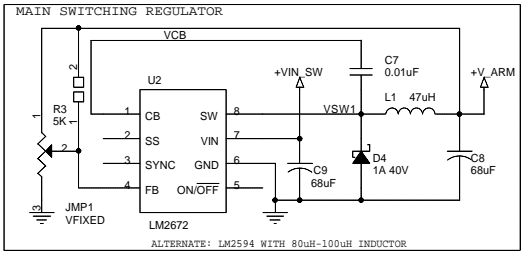
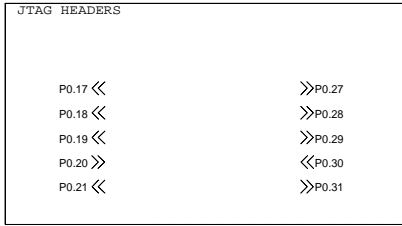
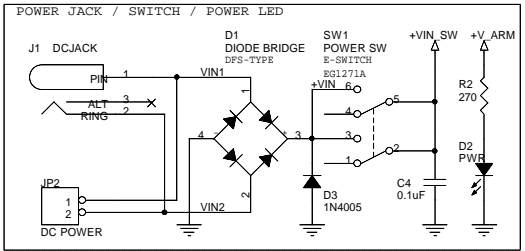
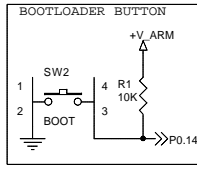
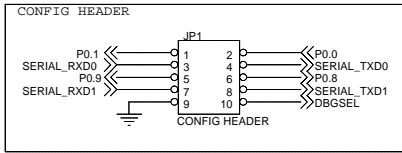
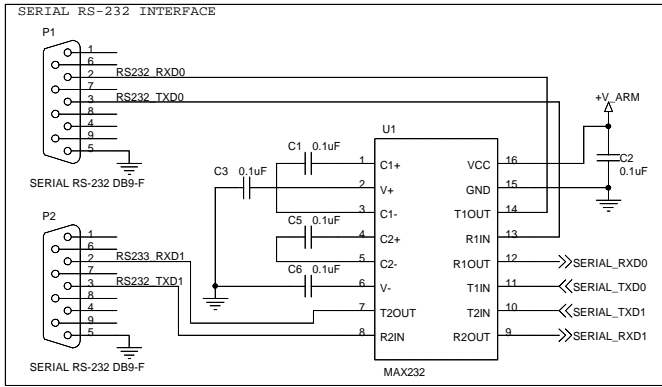
IDE/ATA INTERFACE



STEREO AUDIO CODEC



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