Combining On-chip SRAM with External SDRAM to Construct a Low-latency LCD Frame Buffer

INTRODUCTION

The NXP LH79520 has 32KB of on-chip SRAM. Systems that require high performance and low power can use this memory as an on-chip frame buffer. Unfortunately, 32KB is not enough memory for most color displays. For example, a 320 × 240 8-bits per pixel display requires 75KB. Even so, because on-chip memory is so much faster and consumes so much less power than SDRAM, using on-chip SRAM for part of a larger frame buffer is still worth the effort. This application note describes how to configure your system to make on-chip SRAM and SDRAM appear like one large, contiguous memory that has lower latency and consumes less power than when using SDRAM alone.

MEMORY CONFIGURATIONS

The LH79520 has an ARM720T core. The ARM720T has an MMU that makes it necessary to make the distinction between physical memory addresses and virtual memory addresses. If the MMU is active in the ARM720T core, code executes in the processor from virtual memory addresses. A virtual address can map to a completely different physical address.

At first glance, the task of merging the SRAM and SDRAM sounds like a job for the MMU. Unfortunately, the MMU performs address translation for the processor core only. DMA peripherals like the Color LCD Controller (CLCDC) are not part of the ARM720T core, so DMA peripherals use physical addresses only. In order to merge on-chip SRAM and SDRAM into one contiguous physical address space, you have to take advantage of LH79520's REMAP capability and the on-chip SRAM's address mirroring property.

After reset, the LH79520 has the memory map that corresponds to the leftmost map shown in Figure 1. By setting the REMAP register in the LH79520's Reset, State, and Power Controller (RCPC) to 0b10, your program will move the on-chip SRAM bank next to the SDRAM memory. Since the on-chip SRAM is only 32KB, there is a big gap between the last address of on-chip SRAM, 0x00007FFF, and the first address of SDRAM, 0x20000000.

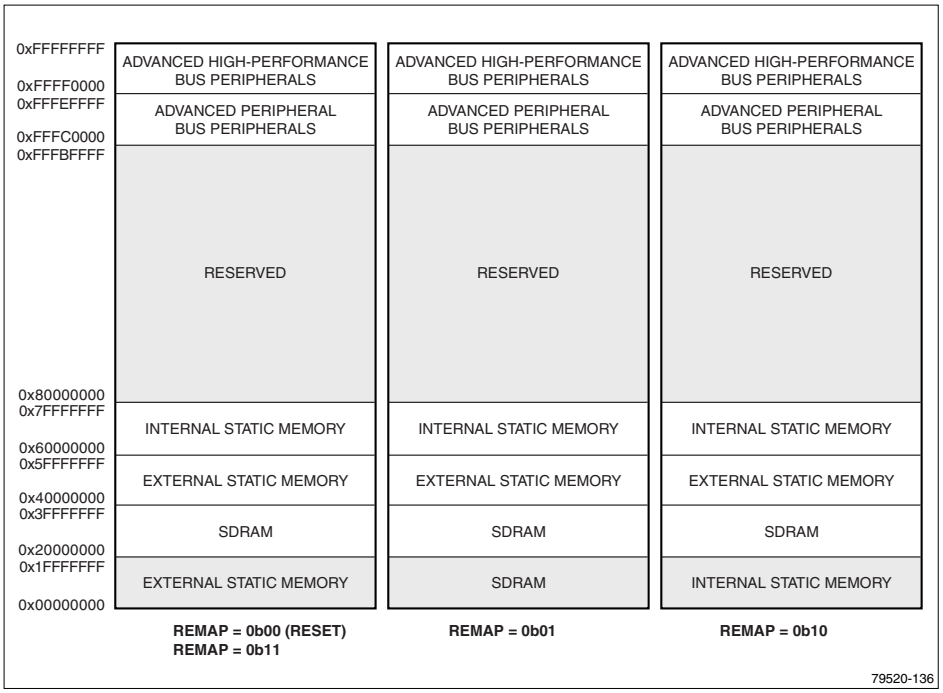

Figure 1. LH79520 Memory Configurations

Addressing mirroring describes what happens when your program tries to access memory at an address that is past the last physical address of a particular device. With REMAP equal to 0b10, the 32KB on-chip SRAM has the physical address range of 0x00000000 - 0x00007FFF. The on-chip SRAM's address bus has only 15 bits. If your code tries to access memory at address 0x00008000, then bits 14 through 0 of the SRAM's address bus will be 0; the fact that address bit 15 is set to 1 is ignored because it is not wired. Therefore, an access to 0x00008000 will actually access memory at address 0x00000000. As Figure 2 shows, in the address range 0x00000000 - 0x1FFFFFFFF, this address wrapping phenomenon causes the on-chip SRAM to appear to be mirrored every 32KB in the address space.

Therefore, to create a 75KB frame buffer out of on-chip SRAM and SDRAM, set the CLCDC upper panel frame buffer at address 0x1FFF8000. The frame buffer will span from 0x1FFF8000 - 0x2000ABFF.

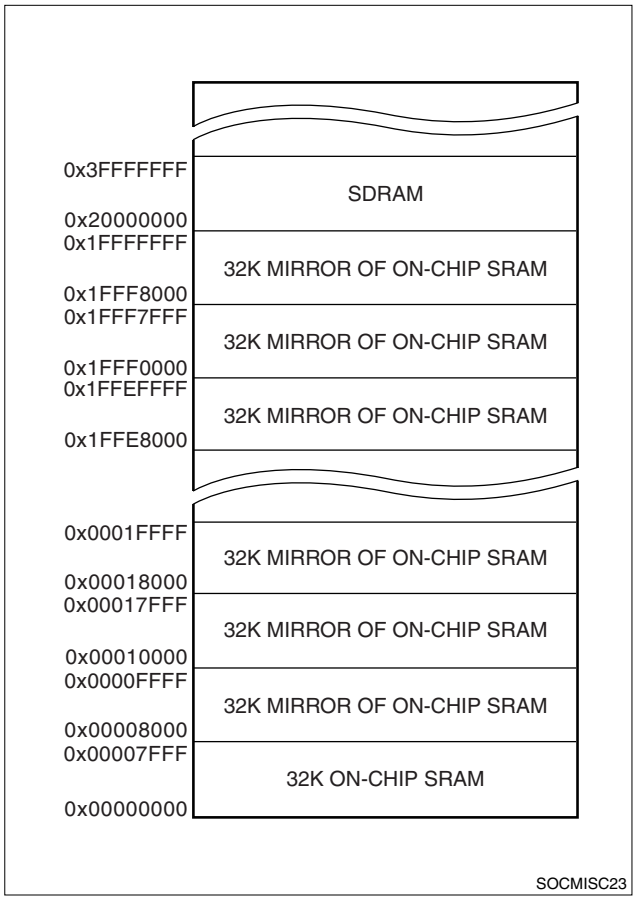

Figure 2. Address Mirroring of On-chip SRAM, REMAP = 0b10

OTHER CONSIDERATIONS

Most LH79520 applications require exception vectors to be located starting at virtual address 0x00000000. Since you have set the REMAP register to 0b10, the physical address space starting at 0x00000000 is already taken by the first 32KB or your frame buffer. For systems that have a high interrupt rate, your program might benefit from using some of the on-chip SRAM for exception processing. For such systems, simply set the on-chip frame buffer start address in the CLCDC to the address within internal memory that follows all exception processing code. For example, if the exception handling code takes 1KB, set the CLCDC frame buffer start address to 0x1FFF8400.

On the other hand, since the LH79520 fetches instructions using virtual addresses, you don't have to reserve the space exception vectors require from use by your frame buffer. The MMU allows you to put any memory you want at virtual address 0x00000000. For example, you could map a 4KB page of SDRAM to virtual address 0x00000000 and copy your exception vectors to the new virtual address. Of course, you will have to use the MMU to create a contiguous virtual memory space for the frame buffer, too. If you have a fast graphics library, program the MMU so that the frame buffer's virtual memory space is cached, but not write buffered. This will minimize the latency of frame buffer updates. For more details on how the MMU works, see the ARM720T Technical Reference Manual, ARM Doc Number DDI0191A, available at http://www.nxp.com/redirect/arm.com.

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