Static Memory System Design

INTRODUCTION

The LH79524 and LH79525 incorporate a highly efficient External Memory Controller (EMC). This controller interfaces the MCU to both static and dynamic external memory and peripheral devices. This application note addresses the unique features of the EMC in static memory system designs. In the balance of this application note, 'EMC' will refer specifically to the static memory interface characteristics of the controller. For additional information, refer to the LH79524/LH79525 User's Guide.

STATIC MEMORY OPERATION

The EMC increases addressing efficiency by automatically shifting the addresses output on the external memory bus, depending on the size of memory devices being addressed. For 8-bit memory systems, address *signal* A0 is connected to address *pin* A0. With a 16-bit system, addressing does not require address signal A0 since accesses begin on half-word boundaries. For 32-bit systems, both address signal A0 and A1 are not needed because memory accesses begin on word boundaries. Byte Lane Enables should be used for addressing individual bytes.

Figure 1 shows how the internal address *signals* are switched to the address *pins*. For example, in the configuration shown in Figure 1, the memory device width has been programmed to 32 bits by programming the SCONFIGx:MW field to 0b10. You should note that this is the width of the connected memory system, not the device. Thus, if you connect two 16-bit memory devices as a 32-bit wide system, the MW field is programmed to 0b10 for 32 bits. If you connect the 16-bit devices as a 16-bit wide system, program MW to 0b01, and the switches in Figure 1 would then move to the '01' position, which connects address signal A1 to pin A0 and so forth. Shifting the address automatically greatly simplifies your hardware design and PC board layout. In addition, because all 23 external address lines can be used for 16- and 32-bit systems, the number of addressable locations doubles or quadruples (respectively) compared to memory controllers that do not shift the addresses. The EMC allows the identical number of 8-bit, half-word, and full-word locations to be addressed with the same external address bus.

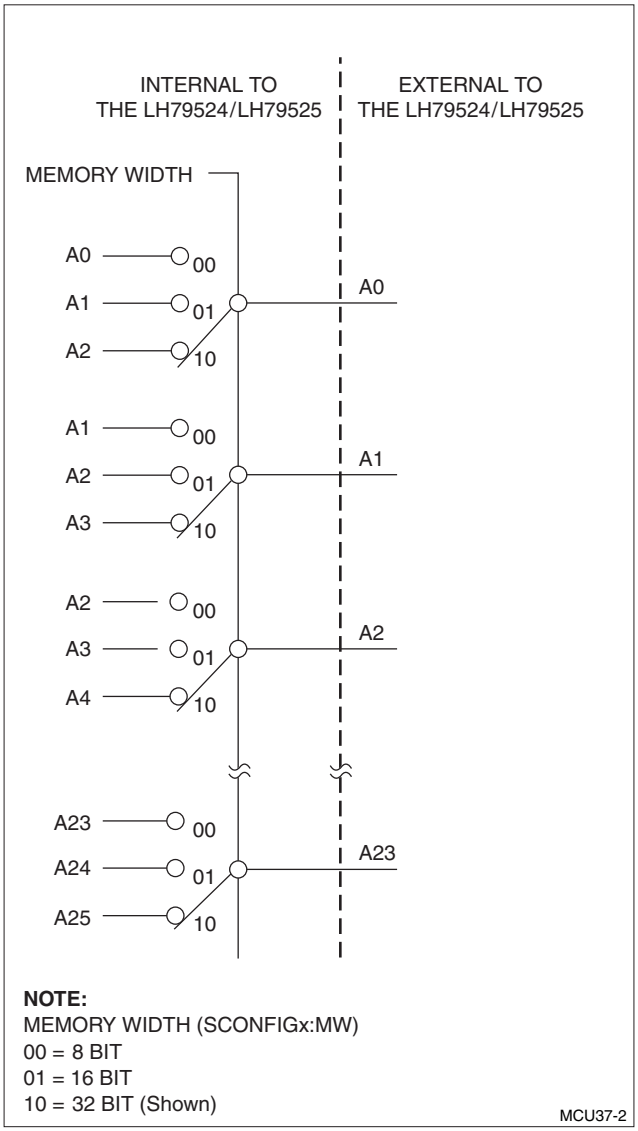

Figure 1. Automatic Address Shifting

HARDWARE DESIGN

Automatic address shifting makes your hardware design much simpler. Rather than connecting different address pins to different memory devices depending on the width, MCU pin A0 always connects to device pin A0, MCU A1 to device A1, continuing through MCU pin A23 connecting to device pin A23.

Figure 2 through Figure 4 illustrate typical static memory system design using the LH79524 and LH79525 with automatic address shifting.

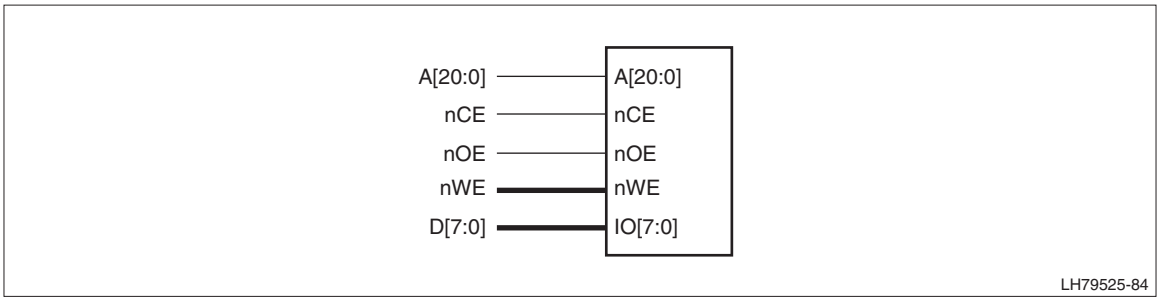

Figure 2. Eight-bit Memory Connection

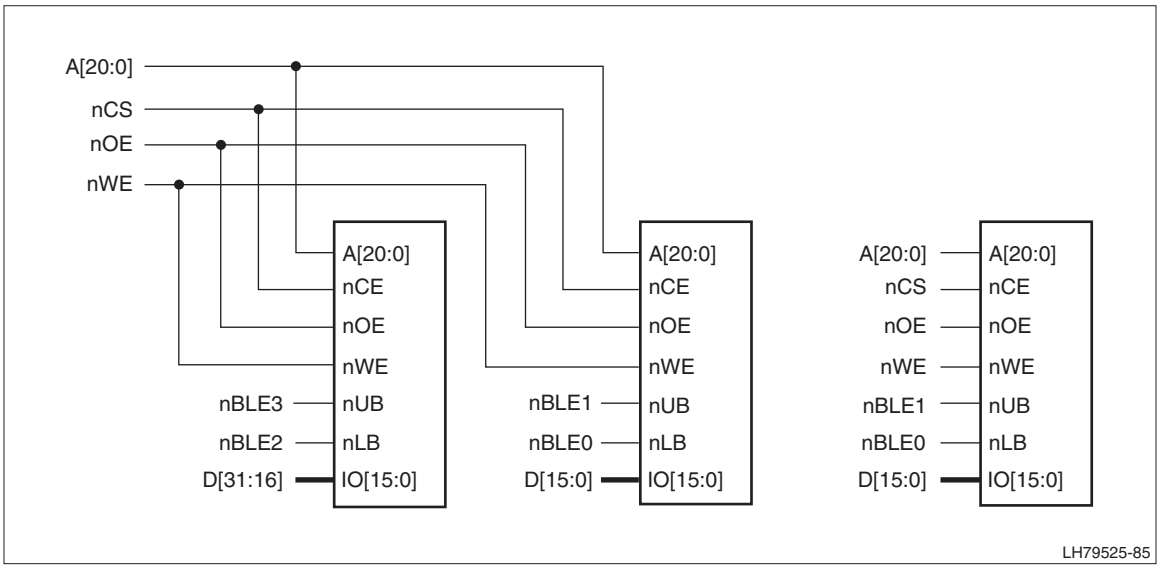

Figure 3. Sixteen-bit Memory Connected for 32-bit System (left) and 16-bit System (right)

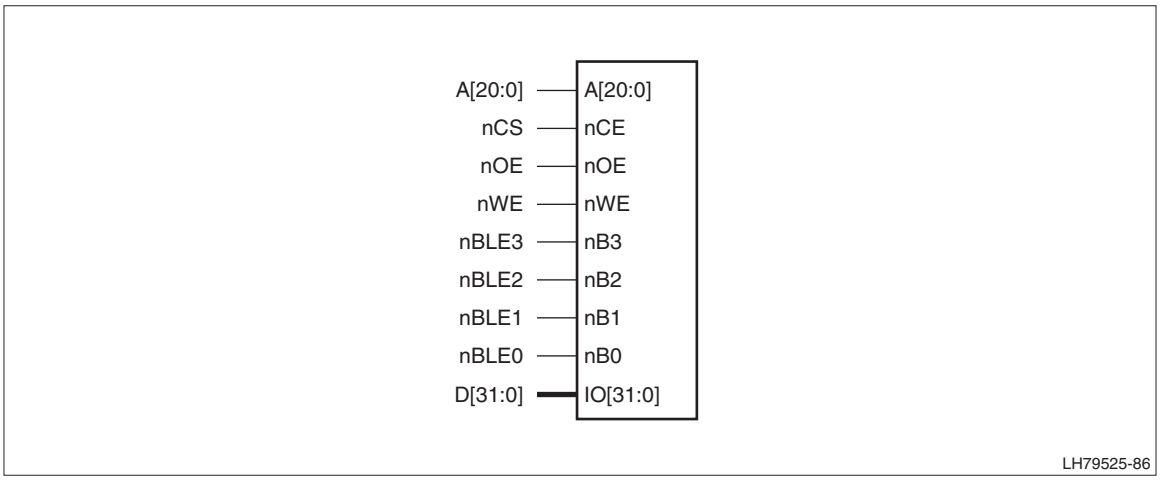

Figure 4. Thirty-two-bit Memory Connection

SOFTWARE DESIGN

For the bulk of software designs, the automatic address shifting is completely transparent and no software considerations are needed. However, in instances where software must control the signal on a specific address *pin*, your design must account for any address shifting.

Simple Shifting Subroutine

If your application requires specific signals on specific address lines, it may be necessary to pre-shift the address before executing a Read or Write. When addressing 16- or 32-bit wide devices, a subroutine based on the flow chart in Figure 5 handles the necessary pre-shifting. 'Device Width' can be determined by reading the SCONFIGx:MW field.

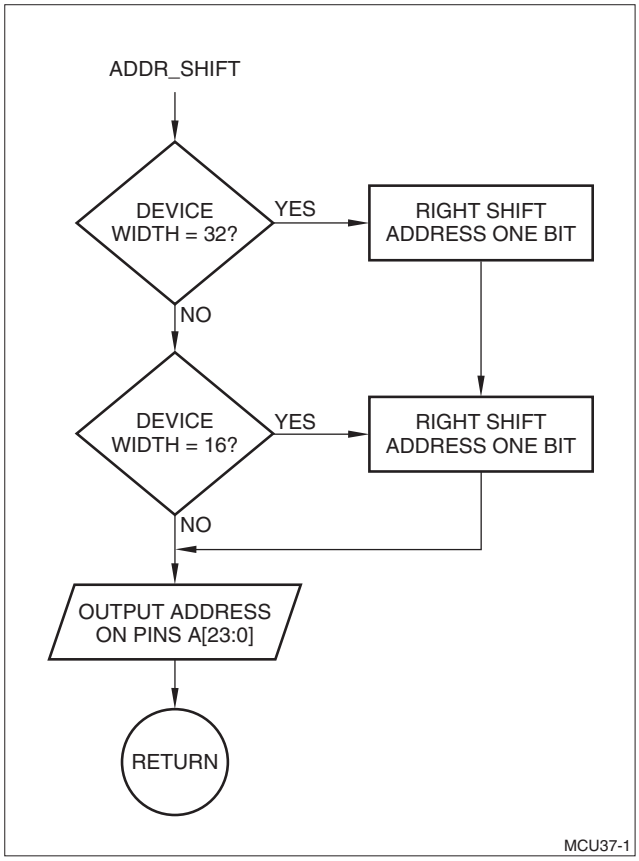

Figure 5. Pre-shifting Routine

INTERFACING WITH NAND FLASH

The EMC interface for NAND Flash has two modes: one for booting and one for normal accesses. During boot, the Boot ROM handles the logic for generating control signals on the four address lines used for the Address Latch Enable (ALE), Command Latch Enable (CLE), Flash Write Enable (nFWE), and Flash Read Enable (nFRE) signals. When used for booting, the NAND Flash must be selected with chip select nCS0. If not used for booting, it can be selected with any chip select signal.

Booting Example

Booting from NAND Flash is defined by the static signals on Port C[7:4] at reset, as shown in Table 1.

If your application uses the on-board Boot ROM to direct a boot from external NAND Flash, four address lines function as NAND Flash control pins. Connection of the MCU to the NAND Flash is illustrated in Figure 6.

Table 1. Boot Configuration

PC[7:4]	BOOT CONFIGURATION
0x0	NOR Flash or SRAM; 16-bit data; nBLEx is LOW for reads
0x1	NOR Flash or SRAM; 16-bit data; nBLEx is HIGH for reads
0x2	NOR Flash or SRAM; 8-bit data; nBLEx is LOW for reads
0x3	NOR Flash or SRAM; 8-bit data; nBLEx is HIGH for reads
0x4	NAND Flash; 8-bit data; 3-byte address
0x5	NAND Flash; 8-bit data; 4-byte address
0x6	NAND Flash; 8-bit data; 5-byte address
0x7	NAND Flash; 16-bit data; 3-byte address
0x8	NOR Flash or SRAM; 32-bit data; nBLEx is LOW for reads
0x9	NOR Flash or SRAM; 32-bit data; nBLEx is HIGH for reads
0xA	Undefined
0xB	Undefined
0xC	NAND Flash; 16-bit data; 4-byte address
0xD	NAND Flash; 16-bit data; 5-byte address
0xE	I^2C
0xF	UART

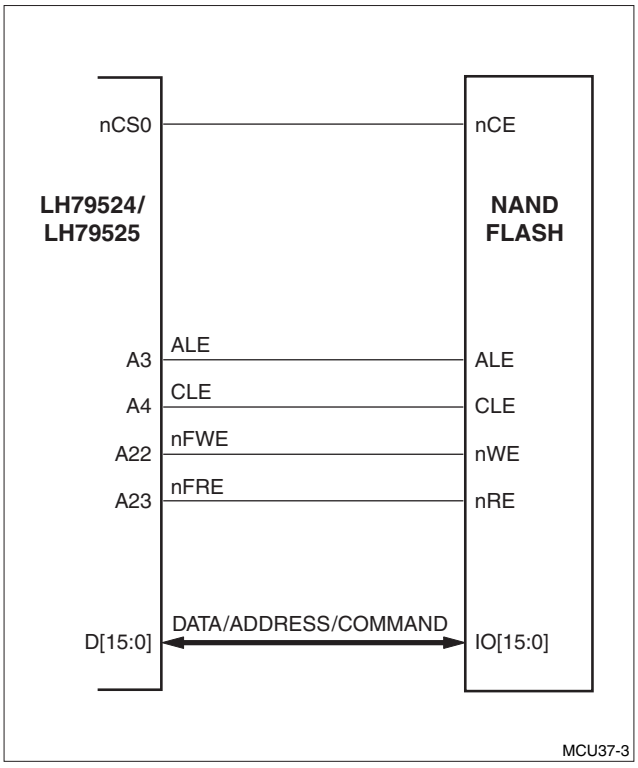

Figure 6. Connection to 16-bit NAND Flash

During boot, the Boot ROM in the LH79524/LH79525 automatically controls the logic to present the proper signals at the proper times on the address lines acting as control signals. Thus, care must be taken to either not use nCS0 for other devices, or ensure that the NAND Flash is not inadvertently accessed by addresses in the nCS0 address space.

Normal NAND Flash Access

At all other times but boot, the address lines function as addresses, and the NAND Flash control signals must be generated by your software. For this example, we will use the design in Figure 6, with the four address lines connected to ALE, CLE, nWE, and nRE on the NAND Flash. You could, obviously, use any address lines or GPIO to control the device.

Since NAND Flash devices are available in 8-bit and 16-bit width, it is up to your software to ensure that the proper control signals appear on the proper address pins for correct operation.Using pins D[15:0] to communicate with the NAND Flash requires programming SCONFIGx:MW to 0b01 for 16-bit wide external memory transactions. This also causes the automatic address shift to place the A1 address signal on pin A0. Thus, if you are using a 16-bit NAND Flash, software must assure TRUE conditions on the address signals for the operation being executed, as shown in Table 2.

Table 2. 16-bit Address Mapping

Signal	Output Pin
A3	A2 (ALE)
A4	A3 (CLE)
A23	PC6/A22/nFWE
A24	PC7/A23/nFRE

EXAMPLE TRANSACTION

A quick example illustrates one way for your software to handle 16-bit NAND Flash transactions. This example shows a simple data Write to the NAND Flash, but Reads and Commands work similarly. Figure 7 shows the timing generated by the following sequence.

With all control signals FALSE, the address of the location to be written in the NAND Flash is placed on the LH79524/LH79525 D[15:0] pins (‘A’ in the figure). Software, with the proper signals on D[15:0], then programs a Write to location 0xCXXX10, causing ALE and nFWE to go HIGH (‘B’). With the same data on D[15:0], a write to location 0x4XXX10 causes nFWE to go LOW (‘C’). Writing to location 0xCXX10 again drives nFWE HIGH, which latches the address in the NAND Flash (‘D’). Finally, to clear the interface, 0xCXXX00 is written to, forcing ALE to LOW (‘E’).

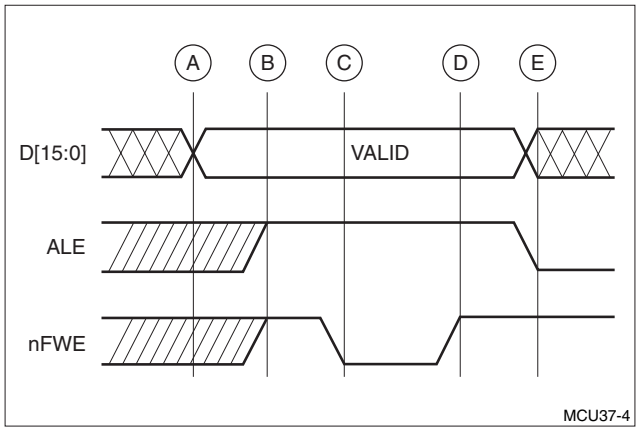

Figure 7. NAND Flash Timing Example

CONCLUSION

For accessing SRAM, PC Cards, and most other static memory devices, the EMC offers seamless control, transparent to the software. By shifting unused address bits to the right for 16- and 32-bit devices, maximum efficiency and address space is obtained.

When specific signals must appear on specific pins, such as when addressing NAND Flash outside of booting, a simple address shifting subroutine that automatically shifts one or two bits depending on the width of the external memory device.

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