Interfacing the Static Memory Controller with I/O Devices

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INTRODUCTION

The Static Memory Controller (SMC) in the LH7A400, LH7A404, LH794xx, and LH79520 MCUs was designed to efficiently interface with static memory and flash devices. To minimize power consumption, the SMC changes the fewest number of control lines that will allow correct memory accesses. The timing of the control signals works very well for accessing memory devices. However, certain custom I/O devices may require careful consideration in order to allow seamless operation with the SMC.

STATIC MEMORY SIGNAL TIMING

During write access to a device that is connected to the Static Memory Controller, one of the active LOW Chip Select signals (nCSx, x = 0, 1, 2…6) goes LOW about one bus clock cycle after the address is presented on the address bus. At about the same time, the write enable strobe (nWE) goes LOW. Figure 1 shows a representative timing of this transaction, in this case the LH7A404. Timing for other MCUs may be slightly different; consult the product Data Sheet for the particular chip of interest.

During read access from a device that is connected to the SMC, one nCSx goes LOW about the same time the address becomes valid. The read enable strobe (nOE) also goes LOW at about the same time: the loading on each signal and delays inside the chip determine which signal goes active first. The chip design guarantees that one nCSx and one of nOE or nWE signals will go active during the same bus clock cycle. It is possible that the data strobe signals could go active before nCSx goes active. During Reads, it is possible for nOE to go active before the address is stable or the Chip Select is LOW. All NXP MCU data sheets show this timing explicitly, but details such as this are often easy to miss.

If your external I/O device has timing requirements on nCSx versus the falling edge of nOE or nWE (for example, to latch the address and Chip Select status on the falling edge of a data strobe), you must take care to make sure that your device gates nOE and nWE with nCSx. Furthermore, you must make sure your gate circuit provides enough setup time for your address latches to work. The sample circuits in Figure 2 through Figure 4 allow additional delay between nCSx and nOE. More gates may be added as needed. The circuit in Figure 4 also allows for the adjustment of CLKOUT to meet timing requirements.

Optionally, the PCMCIA interface may be used instead of the SMC interface. The PCMCIA interface guarantees Chip Select and read strobe signals for each access and allows fine-tuning of signal timing relationships. The PCMCIA has a 16-bit data size limitation.

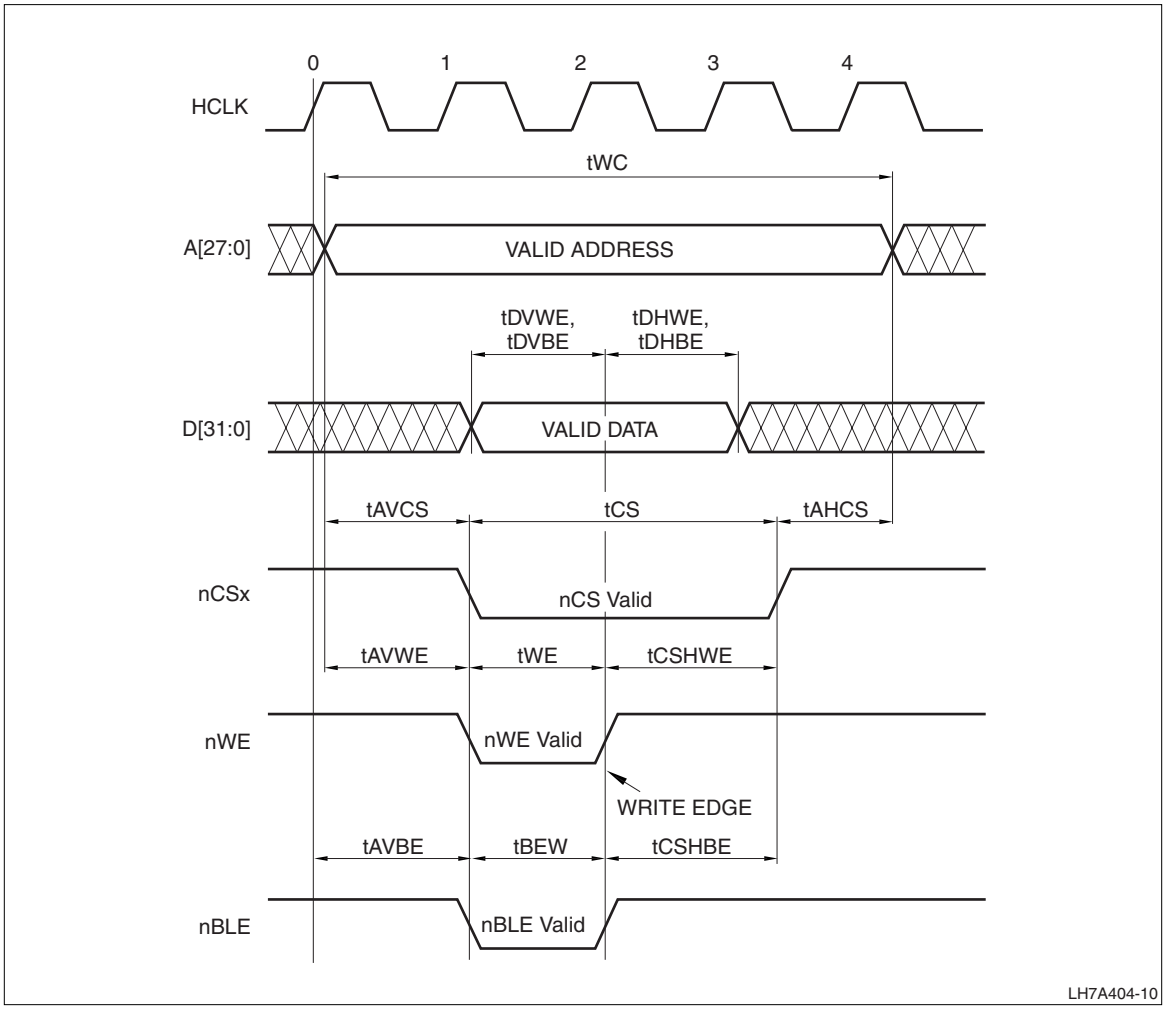


Figure 1. Static Memory Write

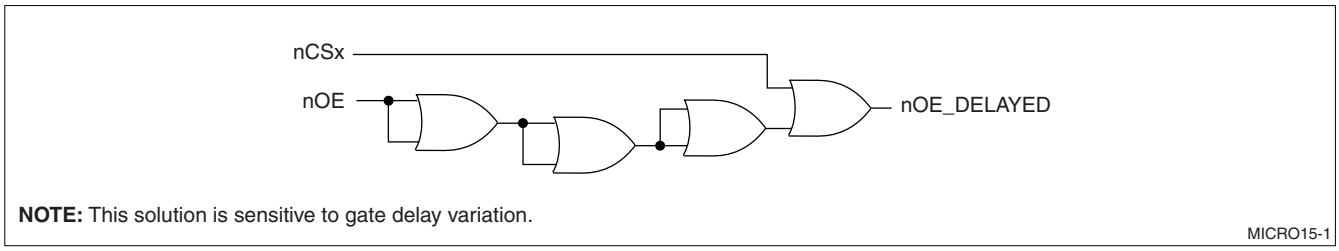


Figure 2. Delay Using Gates

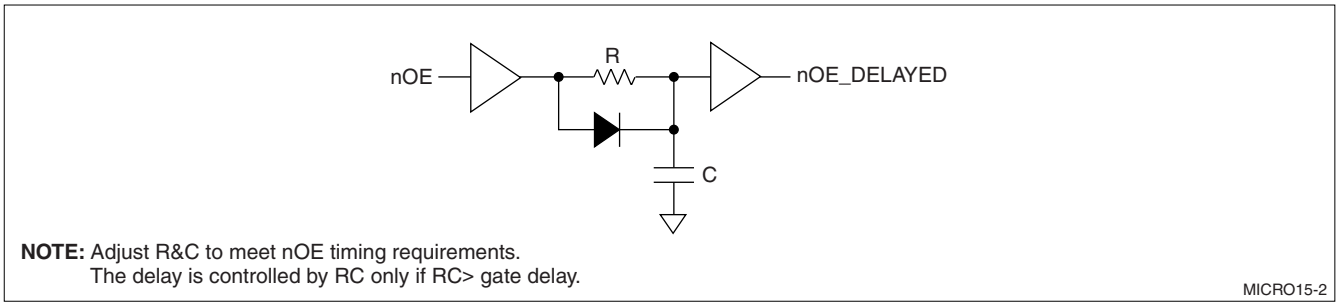
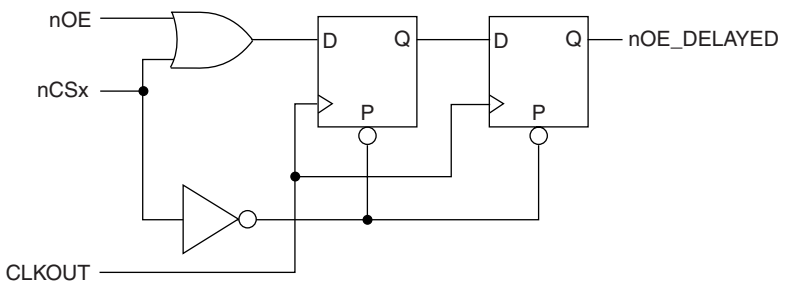


Figure 3. Delay Using RC Time Constant



NOTE: This design requires CLKOUT to be set to match the bus clock frequency. The setup time will depend on the current bus clock.

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Figure 4. Delay Using Flip-flops

CHIP SELECT (nCSx) STAYS ACTIVE

Once the SMC asserts one of the nCSx signals for either a Read or Write, it may keep that signal asserted until another device is addressed, the bus state transitions from Read to Write or Write to Read, or the external bus goes inactive.

Although an SMC-generated Chip Select can normally be deasserted by accessing another device or chip region, such as internal SRAM or SDRAM, many factors such as cache, write buffering, Direct Memory Access (DMA), or processor instructions may occur that keep the Chip Select asserted across multiple accesses. When this type of access occurs, more than one transfer operation will occur for a single Chip Select assertion cycle as show in Figure 5, where three read accesses are performed in one Chip Select cycle.

If your I/O device requires nCSx to deassert in order to advance a state machine, then your software driver must guarantee nCS will deassert before the next access. Code executing from cache or internal SRAM which polls or performs multiple read operations from an SMC memory region assigned to a single nCSx, or processor multiword transfer operations (LDM, STM), are examples of operations that will perform multiple accesses in a single Chip Select cycle and prevent nCSx from deasserting.

The only way to guarantee that a Chip Select cycle will deassert on consecutive access cycles is to access another uncached SMC Chip Select prior to the next access cycle. This forces the current Chip Select to deassert and then reassert on the next access.

The pseudo-code below shows several examples of sequences that will not guarantee Chip Select cycle deassertion:

```
/* Example 1: Chip Select will not toggle
   This example copies data from the SMC chip
   select 1 to SDRAM. It uses the memmove()
   function, which will most likely use the
   processor LDM/STM instructions. The Chip
   Select will stay asserted for this code. */
memmove(sdram_buffer, cs1_buffer, 128);
/* Example 2: Chip Select is not guaranteed
   to toggle
   This example copies data from the SMC Chip
   Select 1 to SDRAM. It uses a tightly packed
   loop to transfer the data and may or may
   not be running from cache. The Chip Select
   may stay asserted for this code. */
int *sdram_buffer, *cs1_buffer;
sdram_buffer = (int *) 0xC0010000;
cs1_buffer = (int *) 0x10001000;
for (i = 0; i < (128 / 4); i++) {
   *sdram_buffer = *cs1_buffer;
   sdram_buffer++;
   cs1_buffer++;
}
```

The following pseudo-code shows an example of what to do if Chip Select deassertion is required:

```
/* Example 3: Chip Select is guaranteed to
toggle
   This example copies data from the SMC Chip
   Select 1 to SDRAM. It uses a tightly packed
   loop to transfer the data and may or may
   not be running from cache. Unlike example
   2, a dummy read to Chip Select 2 is per-
   formed after each read of chip select,
   which will force the Chip Select 1 to de-
   assert between accesses. */
volatile int temp, *cs2_buffer;
int *sdram_buffer, *cs1_buffer;
sdram_buffer = (int *) 0xC0010000;
cs1_buffer = (int *) 0x10001000;
cs2_buffer = (volatile int *) 0x20000000;
for (i = 0; i < (128 / 4); i++) {
   *sdram_buffer = *cs1_buffer;
   temp = *cs2_buffer;
   sdram_buffer++;
   cs1_buffer++;
}
```

OUTPUT ENABLE (nOE) STAYS ACTIVE

If the SMC performs a series of read accesses from an area in static memory that is controlled by a single Chip Select signal, nCSx, and the nCSx signal stays asserted, then the nOE also stays asserted. Figure 6 shows this sequence for multiple Read and Write accesses inside a Single Chip select access cycle. If the address changes during sequential accesses but stays within the memory bank, only the address lines will change. Both nCSx and nOE will remain asserted during multiple Read accesses. nWE will toggle across multiple Write accesses as shown in Figure 6.

If your I/O device relies on nOE to deassert to advance a state machine, then your software driver must guarantee nOE will deassert before the next access. The methods of forcing nOE to toggle are the same as the methods for nCSx and the examples in the Chip Select explanation also apply to nOE.

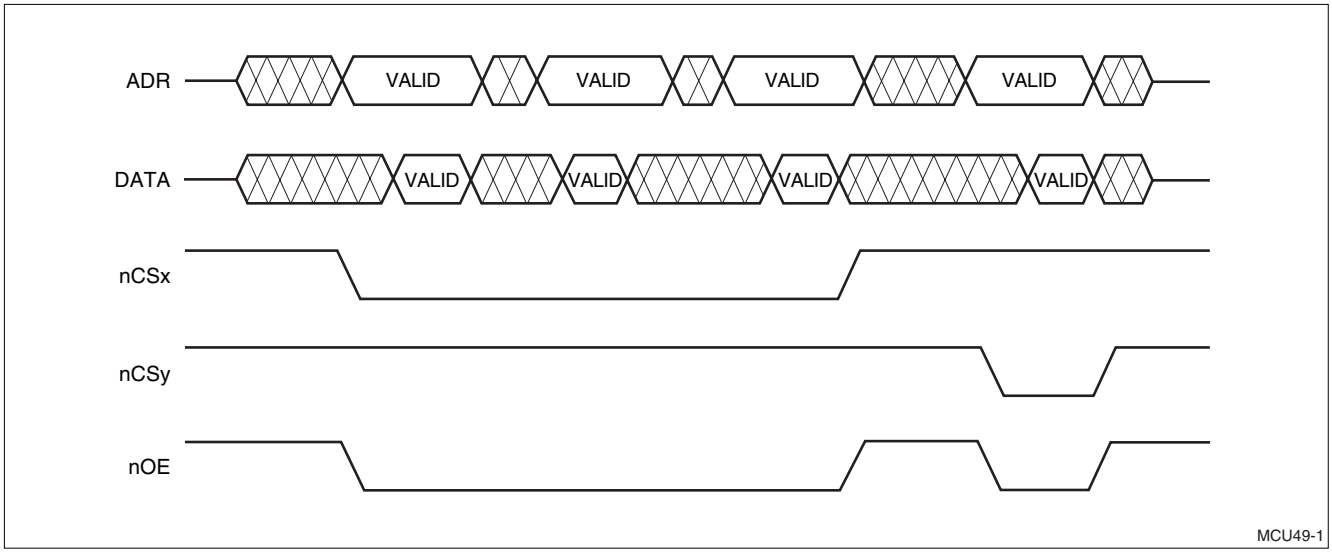

Figure 5. Static Memory Reads From the nCSx Domain Followed by a Read From the nCSy Domain

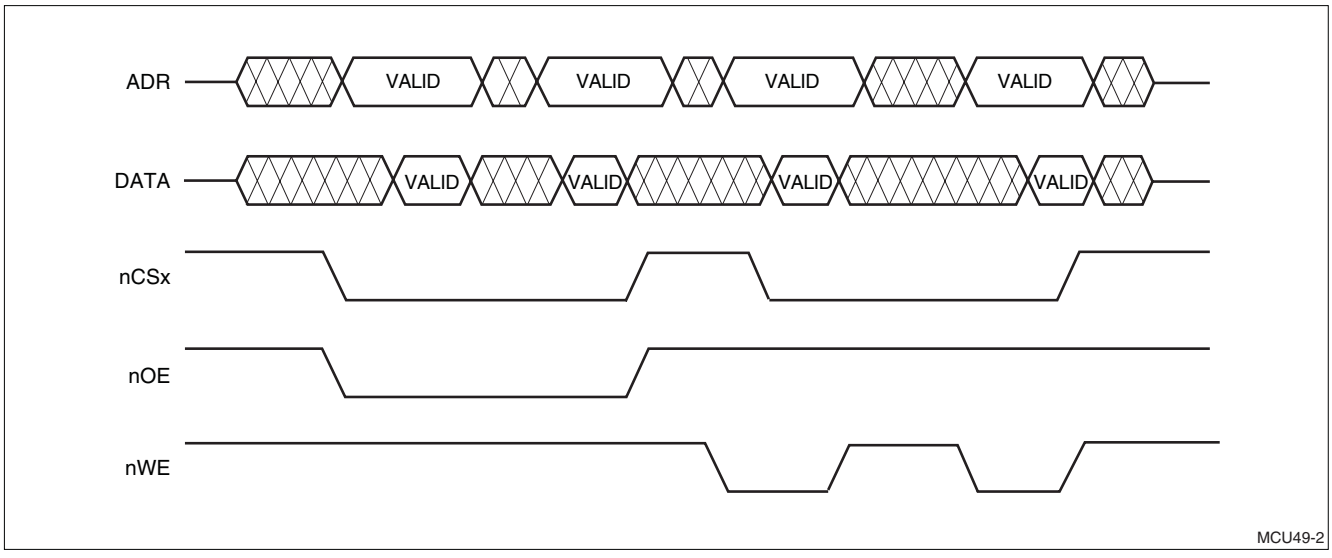

Figure 6. Static Memory Read With Multiple Reads From the nCSx Domain Followed by Multiple Writes From the Same Domain

USING PCMCIA TO GUARANTEE CHIP SELECT AND READ STROBE TIMING

If static memory signal timing and guaranteed Chip Select and Read strobes are very important, it may be better to use the PCMCIA interface for the device. The PCMCIA guarantees ISA-like timing to devices with data widths of 8- and 16-bits. Unlike the normal SMC interfaces of Chip Selects 0 - 3, 6, and 7, the PCMCIA interface allows configuration of chip select to Read and Writing timing, access hold timing, and bus release timing. Chip Select and Read signals are guaranteed on this bus for all operation types, including cached code execution and processor LDM/STM instructions.

Using the PCMCIA bus may require some external logic such as pull-ups or additional bus decoding. Since the PCMCIA bus isn't initialized on chip reset and most PCMCIA control signals are floating, care must be taken so that signals for the PCMCIA bus are in known states until the PCMCIA bus is initialized. This requires a minimum of 3 external pull-up resistors, but may be a small trade-off when guaranteed timing is needed.

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