



Intel[®] StrongARM^{*} SA-1111 Development Module

Schematics

May 2000

Phase 5





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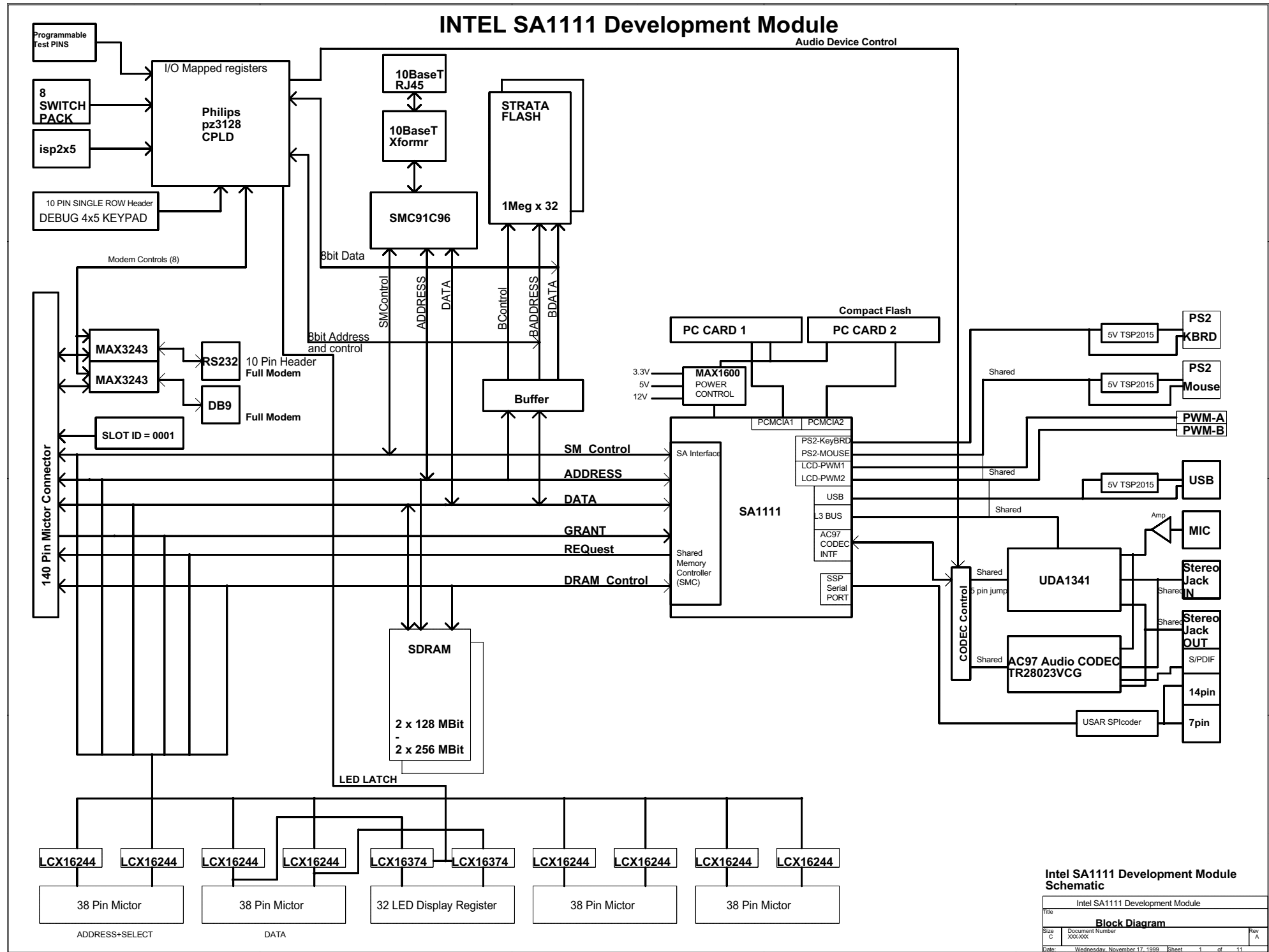
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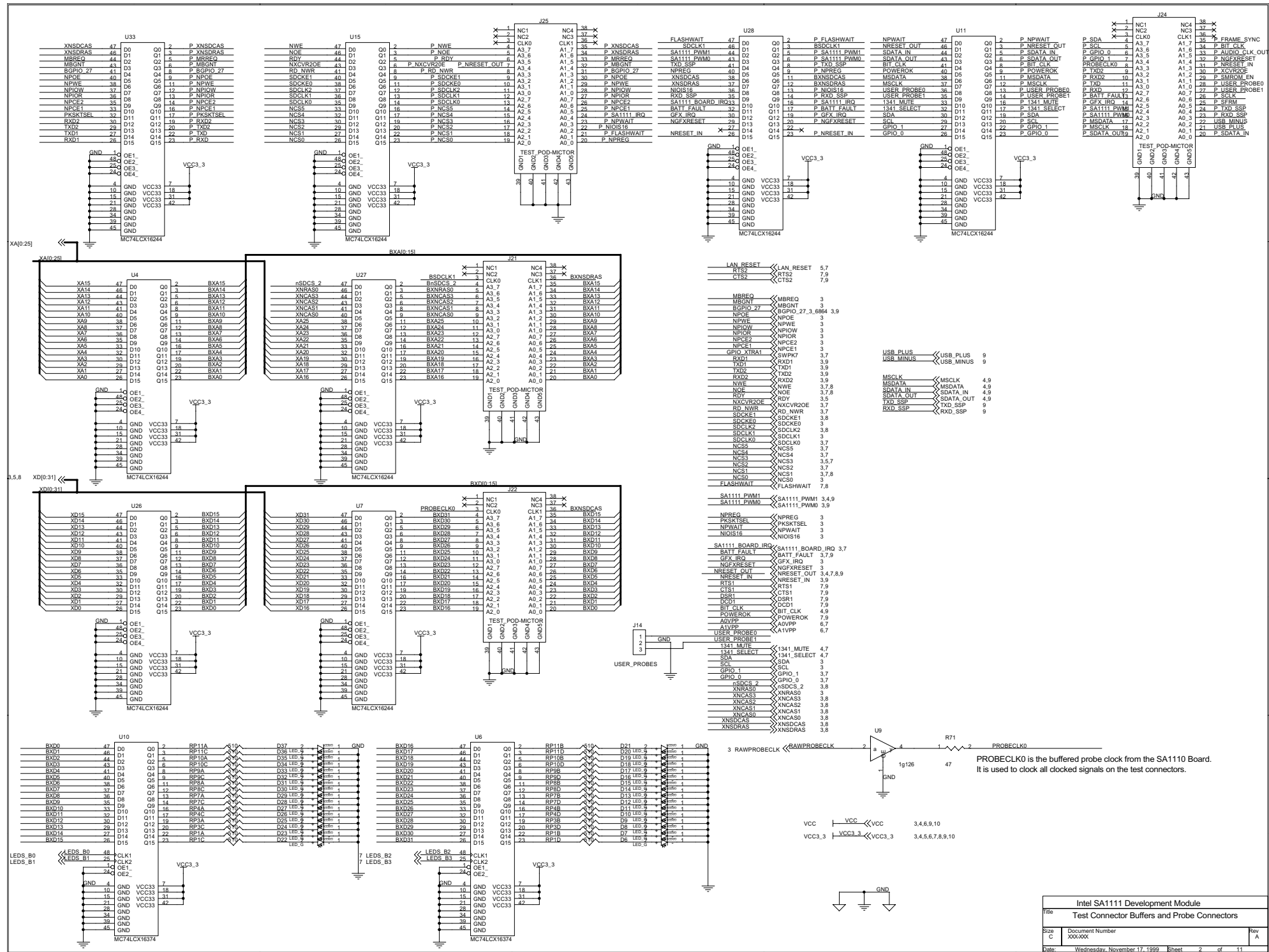


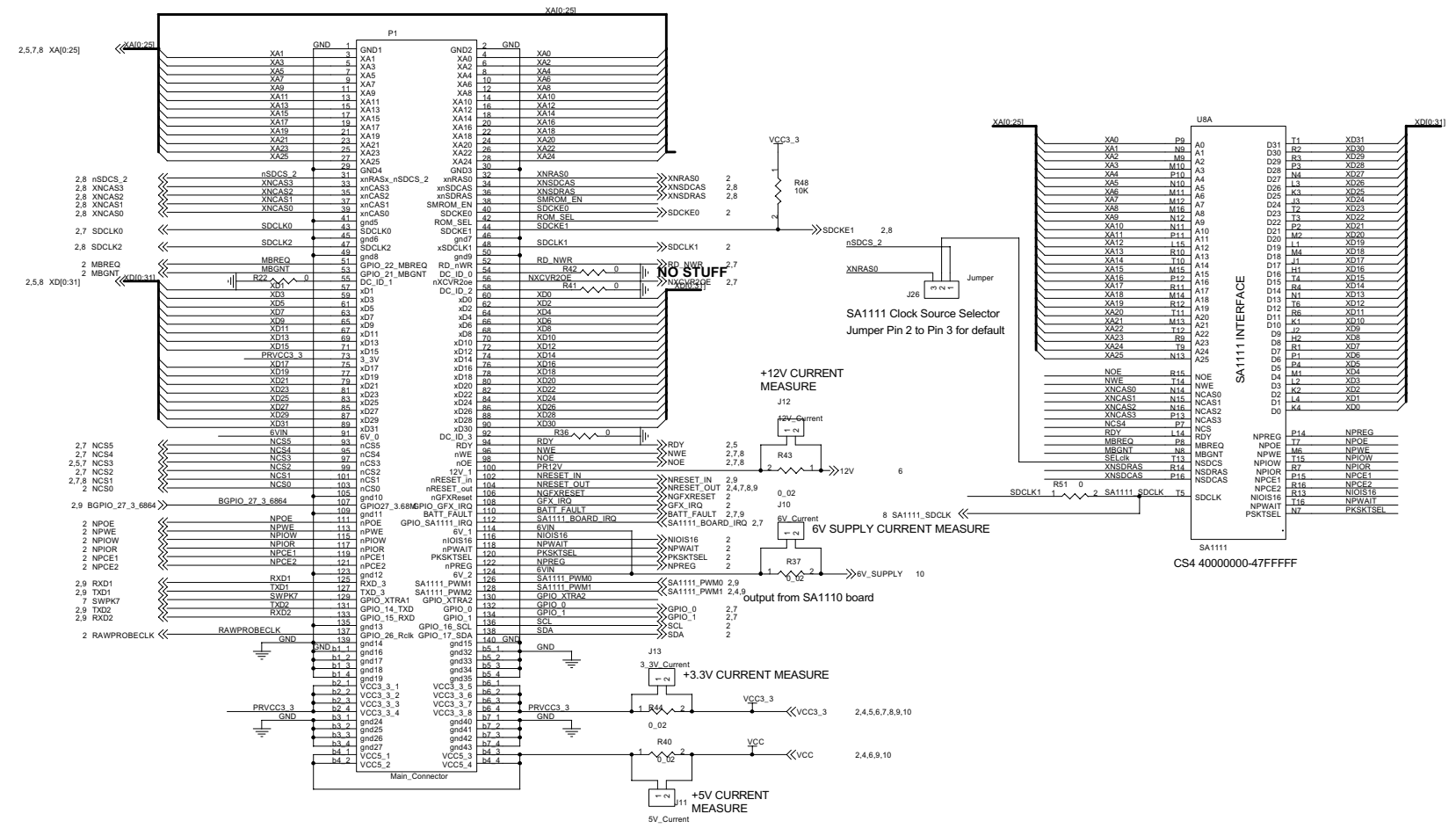
1.0 SA-1111 Development Module Schematics

This document contains the electrical schematics and revision information for the Intel® StrongARM® SA-1111 Development Module (SA-1111 Development Module).

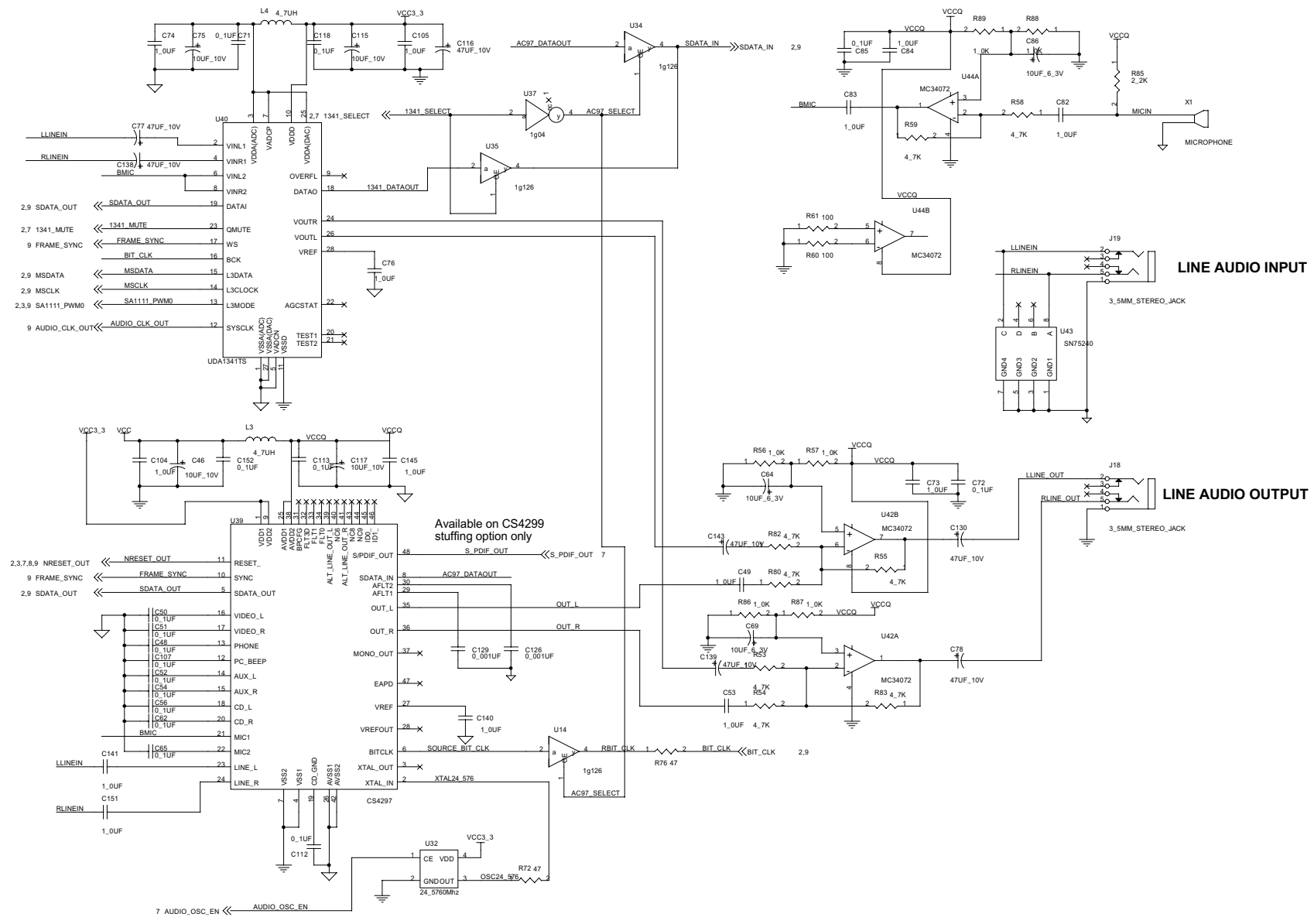
Note: This document and module are for the Phase 5 hardware build of this product. For the latest information and updates, see the hardware release notes that are provided in hardcopy format, and the software readme.txt files that are provided in the software kits.
Sheet 11 of 11 has been omitted because it contains historical information.







Intel SA1111 Development Module		
File	MAIN CONNECTOR TO SA1110 BOARD	
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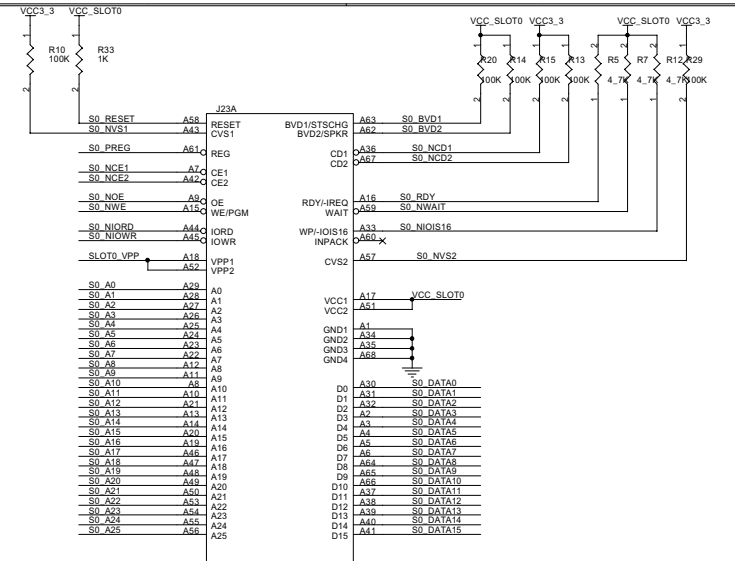
Available on CS4299
stuffing option only

VCC VCC3_3 VCC3_3
VCC3_3 VCC3_3 VCC3_3
2,3,6,9,10 2,3,5,6,7,8,9,10

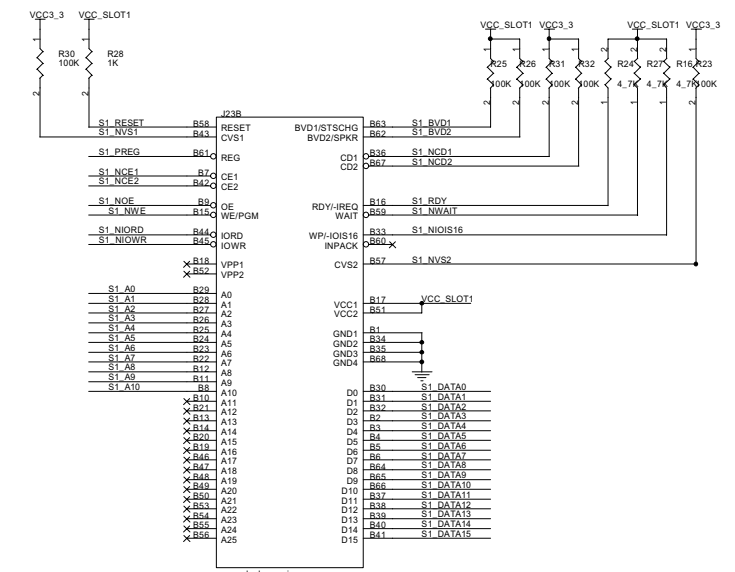
Intel SA1111 Development Module		
AUDIO Components		
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	300000X	A
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SA1111 PCMCIA INTERFACE

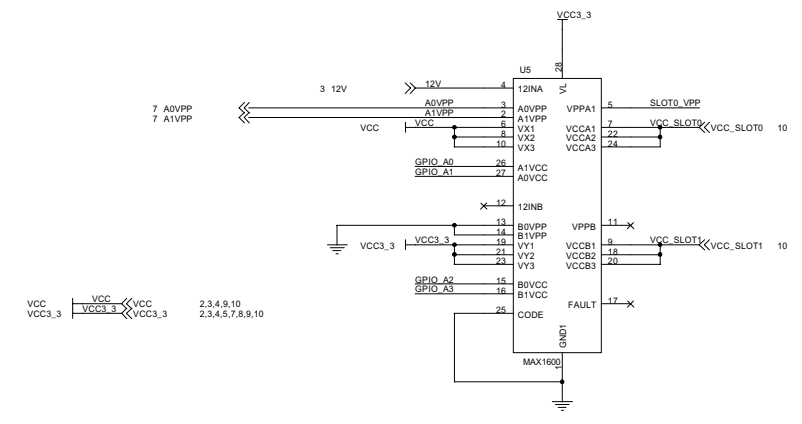
UBB		SA1111		PCMCIA	
S1_PREG	H16	S1_PREG	SO_NPREG	A11	SO_PREG
S1_A0	J14	S1_A0	SO_A0	D11	SO_A0
S1_A1	J13	S1_A1	SO_A1	B11	SO_A1
S1_A2	H12	S1_A2	SO_A2	E9	SO_A2
S1_A3	H13	S1_A3	SO_A3	R10	SO_A3
S1_A4	G14	S1_A4	SO_A4	C9	SO_A4
S1_A5	G12	S1_A5	SO_A5	A9	SO_A5
S1_A6	G16	S1_A6	SO_A6	E8	SO_A6
S1_A7	F12	S1_A7	SO_A7	D8	SO_A7
S1_A8	F14	S1_A8	SO_A8	B8	SO_A8
S1_A9	F16	S1_A9	SO_A9	B4	SO_A9
S1_A10	D14	S1_A10	SO_A10	A1	SO_A10
S1_A11		S1_A11	SO_A11	C4	SO_A11
S1_A12		S1_A12	SO_A12	B6	SO_A12
S1_A13		S1_A13	SO_A13	D2	SO_A13
S1_A14		S1_A14	SO_A14	B6	SO_A14
S1_A15		S1_A15	SO_A15	C2	SO_A15
S1_A16		S1_A16	SO_A16	C2	SO_A16
S1_A17		S1_A17	SO_A17	C2	SO_A17
S1_A18		S1_A18	SO_A18	A6	SO_A18
S1_A19		S1_A19	SO_A19	C6	SO_A19
S1_A20		S1_A20	SO_A20	A7	SO_A20
S1_A21		S1_A21	SO_A21	E5	SO_A21
S1_A22		S1_A22	SO_A22	E7	SO_A22
S1_A23		S1_A23	SO_A23	D2	SO_A23
S1_A24		S1_A24	SO_A24	A6	SO_A24
S1_A25		S1_A25	SO_A25	B9	SO_A25
S1_DATA0	J12	S1_DATA0	SO_DATA0	A12	SO_DATA0
S1_DATA1	K19	S1_DATA1	SO_DATA1	E11	SO_DATA1
S1_DATA2	L13	S1_DATA2	SO_DATA2	C12	SO_DATA2
S1_DATA3	R11	S1_DATA3	SO_DATA3	A3	SO_DATA3
S1_DATA4	D13	S1_DATA4	SO_DATA4	D6	SO_DATA4
S1_DATA5	A14	S1_DATA5	SO_DATA5	F5	SO_DATA5
S1_DATA6	B14	S1_DATA6	SO_DATA6	D3	SO_DATA6
S1_DATA7	B16	S1_DATA7	SO_DATA7	C1	SO_DATA7
S1_DATA8	K18	S1_DATA8	SO_DATA8	B10	SO_DATA8
S1_DATA9	K18	S1_DATA9	SO_DATA9	D12	SO_DATA9
S1_DATA10	E14	S1_DATA10	SO_DATA10	E12	SO_DATA10
S1_DATA11	C13	S1_DATA11	SO_DATA11	D1	SO_DATA11
S1_DATA12	E13	S1_DATA12	SO_DATA12	D4	SO_DATA12
S1_DATA13	A16	S1_DATA13	SO_DATA13	D2	SO_DATA13
S1_DATA14	A16	S1_DATA14	SO_DATA14	B1	SO_DATA14
S1_DATA15	C14	S1_DATA15	SO_DATA15	A2	SO_DATA15
S1_NCD1	L12	S1_NCD1	SO_NCD1	E2	SO_NCD1
S1_NCD2	L16	S1_NCD2	SO_NCD2	C5	SO_NCD2
S1_RDY	F13	S1_RDY	SO_RDY	E6	SO_RDY
S1_NCE1	C16	S1_NCE1	SO_NCE1	B4	SO_NCE1
S1_NCE2	C16	S1_NCE2	SO_NCE2	C3	SO_NCE2
S1_NOE	D16	S1_NOE	SO_NOE	B3	SO_NOE
S1_NWE	F16	S1_NWE	SO_NWE	D6	SO_NWE
S1_NIOR	D16	S1_NIOR	SO_NIOR	C2	SO_NIOR
S1_NIOWR	E16	S1_NIOWR	SO_NIOWR	A4	SO_NIOWR
S1_NWAIT	H14	S1_NWAIT	SO_NWAIT	D10	SO_NWAIT
S1_NIOIS16	G16	S1_NIOIS16	SO_NIOIS16	A13	SO_NIOIS16
S1_RESET	G13	S1_RESET	SO_RESET	A10	SO_RESET
S1_BVD1	J16	S1_BVD1	SO_BVD1	C11	SO_BVD1
S1_BVD2	J16	S1_BVD2	SO_BVD2	E10	SO_BVD2
S1_NV_S1	K14	S1_NV_S1	SO_NV_S1	E4	SO_NV_S1
S1_NV_S2	K16	S1_NV_S2	SO_NV_S2	E1	SO_NV_S2
GPIO_A0	H5	GPIO_A0			
GPIO_A1	F3	GPIO_A1			
GPIO_A2	F4	GPIO_A2			
GPIO_A3	F1	GPIO_A3			



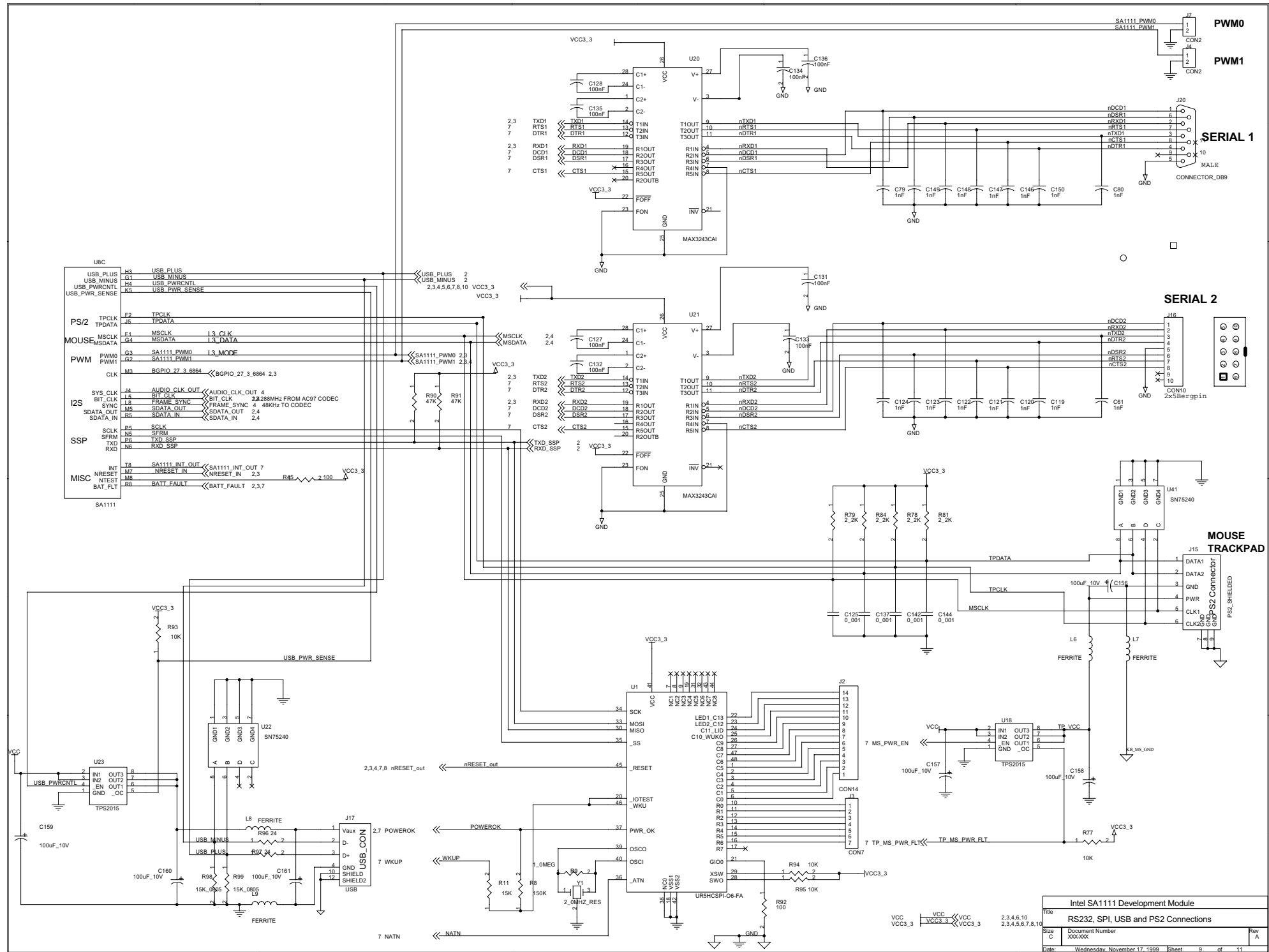
OUTER SLOT

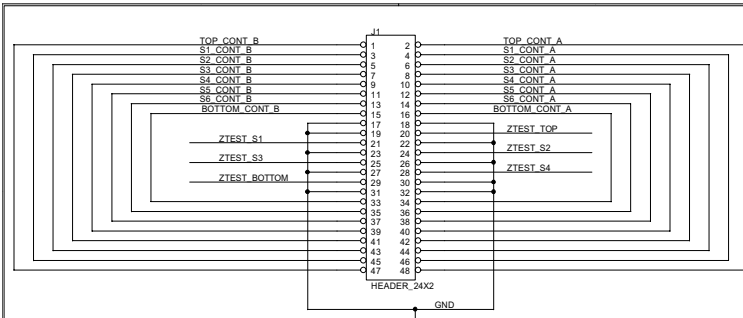


INNER SLOT
COMPACT FLASH



Intel SA1111 Development Module		
File	PCMCIA / Compact Flash Connections	
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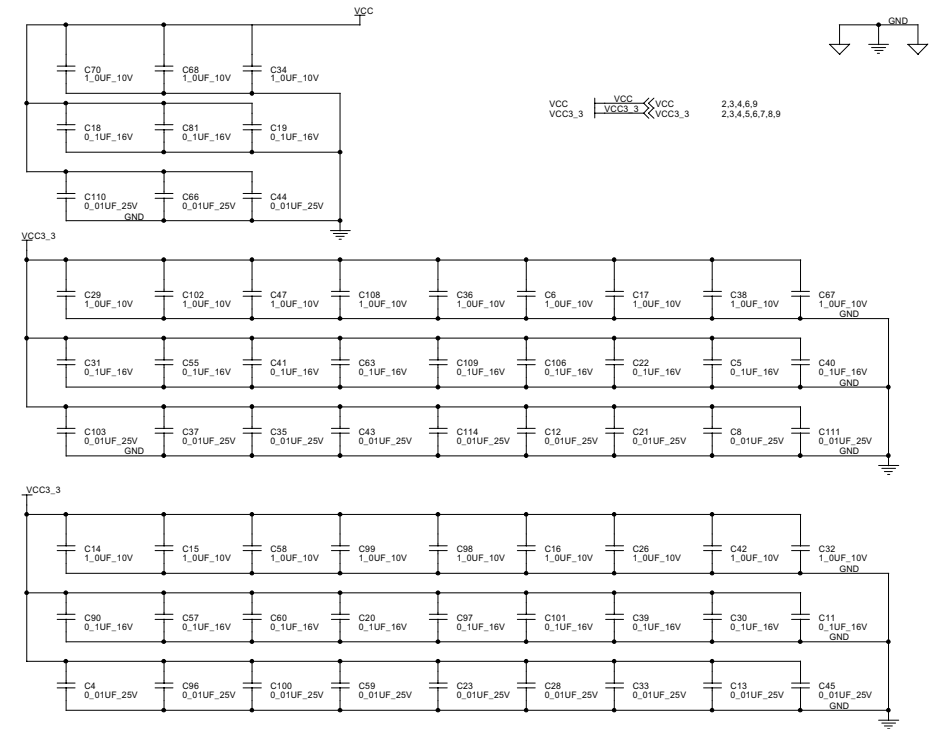
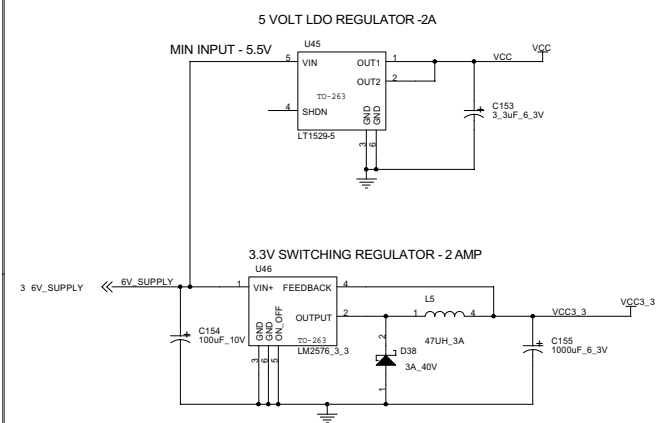
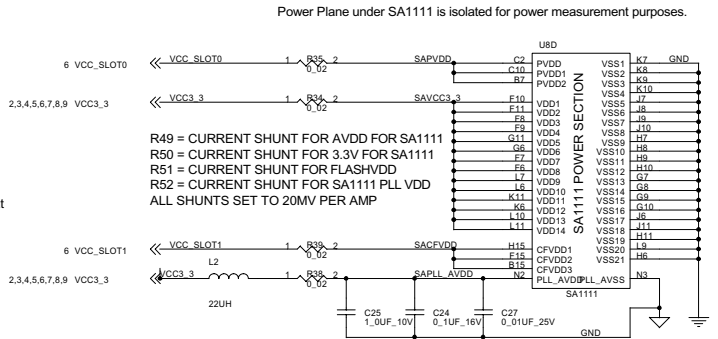
NO STUFF

Board test coupon

TEST HEADER IS 25 MIL PAD WITH 10 MIL DRILL SPACED 50 MIL SEPERATION. PATTERN IS 20 X 2 PLACED NEAR BOARD EDGE

ZTEST "layer" line set to nominal line widths on each layer - minimum length = 6 Inches. These traces should be surrounded by theiving traces space 40 mils from test trace where possible. Nominal impedance should be 60 ohms +/- 10%.

"LAYER_CONT_A" and "LAYER" _CONT_B Traces are minimum trace width, 5 mil internal, 5 mil top and bottom, and minimum seperation, 5 mil external and internal, that are run around the edge of the board on as long a path as possible. This is an overetch and underetch test.



Intel SA1111 Development Module		
File	POWER Supplies, Test Coupon, and MISC	
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