
Errata

- Releasing Reset Condition without Clock
- Reset during EEPROM Write
- Serial Programming at Voltages below 2.9 Volts

3. Releasing Reset Condition without Clock

If an external reset or a watchdog reset occurs while the clock is stopped and the reset is released before the clock is restarted, the internal reset will time out after the start-up delay, which is independent of the external clock. If no external clock pulses are present in the period when internal reset is active, the reset does not correctly cause tri-stating of the I/O while the reset is held. However, if the internal reset is released before the clock starts running, the part does not clear its I/O registers, nor set PC to 0x00. Here, stopping the clock refers to gating the external clock input. Power-down mode does not have this issue.

Problem Fix/Workaround

Make sure the clock is running whenever an external reset can be expected. If the watchdog is used, never stop an external clock.

2. Reset during EEPROM Write

If reset is activated during EEPROM write, the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

1. Serial Programming at Voltages below 2.9 Volts

At voltages below 2.9 Volts, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} at 2.9 Volts or higher during In-System Programming.



8-bit AVR[®]
Microcontroller
with 1K Byte
In-System
Programmable
Flash

AT90S1200/A
Rev. F
Errata Sheet





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