

Errata

- Releasing Reset Condition without Clock
- Lock Bits at High V_{CC}
- Reset during EEPROM Write
- Serial Programming at Voltages below 2.9 Volts
- UART Loses Synchronisation if RDX Line is Low when UART Receive is Disabled

5. Releasing Reset Condition without Clock

If an external reset or a watchdog reset occurs while the clock is stopped and the reset is released before the clock is restarted, the internal reset will time out after the start-up delay, which is independent of the external clock. If no external clock pulses are present in the period when internal reset is active, the reset does correctly causes tri-stating of the I/O while the reset is held. However, if the internal reset is released before the clock starts running, the part does not clear its I/O registers, nor sets PC to 0x00. Here, stopping the clock refers to gating the external clock input. Power-down mode does not have this issue.

Problem Fix/Workaround

Make sure the clock is running whenever an external reset can be expected. If the watchdog is used, never stop an external clock.

4. Lock Bits at High V_{CC}

On some devices, the lock bits will not erase at high V_{CC} . In this situation, it will not be possible to reprogram the devices when the lock bits are set.

Problem Fix/Workaround

Lower V_{CC} below 4.0V before performing a chip-erase. Then the device will unlock, and it will be possible to reprogram the device at any V_{CC} .

3. Reset During EEPROM Write

If reset is activated during EEPROM write, the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

2. Serial Programming at Voltages below 2.9 Volts

At voltages below 2.9 volts, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} above 2.9 volts during in-system programming.

1. UART Loses Synchronization if RXD Line is Low when UART Receive is Disabled

The UART will detect a UART start-bit and start reception even if the UART is not enabled. If this occurs, the first byte after re-enabling the UART will be corrupted.

Problem Fix/Workaround

Make sure that the RX line is high at start-up and when the UART is disabled. An external RS-232 level converter keeps the line high during start-up.



8-bit **AVR**[®]
Microcontroller
with 2K Bytes of
In-System
Programmable
Flash

AT90S2313
Rev. B/C
Errata Sheet





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