Active Errata List

- **PGM: PSCxRB Fuse**
- **PSC: Prescaler**
- **PSC: PAOCnA and PAOCnB Register Bits (Asynchronous output control)**
- **PSC: PEVxA/B Flag Bits**
- **PSC: Output Polarity in Centered Mode**
- **PSC: Output Activity**
- **VREF**
- **DALI**
- **DAC: Register Update**
- **DAC: Output spikes**
- **DAC driver: Output Voltage linearity**
- **ADC: Conversion accuracy**
- **Analog comparator: Offset value**
- **Analog comparator: Output signal**
- **PSC: Autolock modes**
- **DALI: 17th bit detection**
- **PSC: One ramp mode with PSC input mode 8**

Errata History

Mask Revision	Lot Number	Errata List
REV A	04103x	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17

Errata Description

1. PGM: PSCxRB Fuse

The use of PSCXRB fuse can make the ISP fail.

Workaround:

When PSCxRB fuses are used, use the parallel programming mode to load a new program version.

2. PSC: Prescaler

The use of PSC's prescaler have the following effects :

It blocks the sample of PSC inputs until the two first cycles following the set of PSC run bit.

A fault is not properly transferred to other (slave) PSC.

Workaround:

Clear the prescaler PPREx bit when stopping the PSC (prun = 0), and set them to appropriate value when starting the PSC (prun = 1), these bits are in the same PCTL register

Do not use the prescaler when a fault on one PSC should effect other PSC’s

3. PSC: PAOCnA and PAOCnB Register Bits (Asynchronous output control)

These register bits are malfunctioning.

Workaround:

Do not use this feature.

4. PSC: PEVxA/B flag bits

These flags are set when a fault arises, but can also be set again during the fault itself.

AVR MCUs

AT90PWM2
AT90PWM3

Errata Sheet

4437B–AVR–08/05

Workaround:

Don't clear these flags before the fault disappears.

5. **PSC: Output Polarity in Centered Mode**

   In centered mode, PSCOUTn1 outputs are not inverted, so they are active at the same time as PSCOUTn0.

   Workaround:

   Use an external inverter (or a driver with inverting output) to drive the load on PSCOUTn1.

6. **PSC : POACnA/B Output Activity**

   These register bits are not implemented in rev A.

   Workaround:

   Do not use this feature.

7. **VREF**

   Remark: To have Internal Vref on AREF pin select an internal analog feature such as DAC or ADC.

   Some stand by power consuption may be observed if Vref equals AVcc

8. **DALI**

   Some troubles on Dali extension when edges are not symmetric.

   Workaround:

   Use an optocoupler providing symmetric edges on Rx and Tx DALI lines (only recommanded for software validation purpose).

9. **DAC: Register Update**

   Registers DACL & DACH are not written when the DAC is not enabled.

   Workaround:

   Enable DAC with DAEN before writing in DACL & DACH. To prevent an unwanted zero output on DAC pin, enable DAC output, with DAOE afterwards.

10. **DAC : Output spikes**

    During transition between two codes, a spike may appears

    Work around:

    Filter spike or wait for steady state

    No spike appears if the 4 last signifiant bits remain zero.

11. **DAC driver: Output Voltage linearity**

    The voltage linearity of the DAC driver is limited when the DAC output goes above Vcc - 1V.

    Work around:

    Do not use AVcc as Vref ; internal Vref gives good results

12. **ADC : Conversion accuracy**

    The conversion accuracy degrades when the ADC clock is 1 & 2 MHz.

    Work around:

    When a 10 bit conversion accuracy is required, use an ADC clock of 500 kHz or below.

13. **Analog comparator: Offset value**

    The offset value increases when the common mode voltage is above Vcc - 1.5V.

    Work around:

    Limit common mode voltage

14. **Analog comparator: Output signal**

The comparator output toggles at the comparator clock frequency when the voltage difference between both inputs is lower than the offset. This may occur when comparing signal with small slew rate.

Work around:

This effect normally do not impact the PSC, as the transition is sampled once per PSC cycle

Be carefull when using the comparator as an interrupt source.

15. PSC : Autolock mode

This mode is not properly handled when CLKPSC is different from CLK IO.

Work around:

With CLKPSC equals 64/32 MHz (CLKPLL), use LOCK mode

16. DALI : 17th bit detection

17th bit detection do not occurs if the signal arrives after the sampling point.

Workaround:

Use this feature only for sofware development and not in field conditions

17. PSC : One ramp mode with PSC input mode 8

The retriggering is not properly handled in this case.

Work around:

Do not program this case.

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