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## Errata

- Releasing Reset Condition without Clock
- Error in Writing Reset Status Bits
- Frequency Range of External RC Oscillator

### 3. Releasing Reset Condition without Clock

If an external reset or a watchdog reset occurs while the clock is stopped (and reset is released before the clock is restarted), the reset is not remembered. The reset does correctly cause tristating of the I/O, while the reset is held – but if the reset is released before the clock starts running, the part does not clear I/O registers, nor set PC to 0x00. Here, stopping the clock refers to gating the external clock input. Power-down mode does not have this issue.

#### Problem Fix/Workaround

Make sure the clock is running whenever an external reset can be expected. If the Watchdog is used, never stop an external clock.

### 2. Error in Writing Reset Status Bits

The EXTRF flag in MCUSR will be cleared when clearing the PORF-flag. The flag does not get cleared by writing a “0” to it.

#### Problem Fix/Workaround

Finish the test of both flags before clearing any of them. Clear both flags simultaneously by writing “0” to both PORF and EXTRF in MCUCR.

### 1. Frequency Range of External RC Oscillator

The frequency range in which the external RC oscillator can be used is more limited than stated in the datasheet. It should only be used for frequencies between 500 kHz and 4 MHz.

#### Problem Fix/Workaround

Use the external RC oscillator only for frequencies between 500 kHz and 4 MHz. Outside this frequency range, use another clock option.

## Significant Datasheet Changes

When waking up from Power-down mode by a pin change interrupt, two instruction cycles are executed before the interrupt flags are updated. During these cycles, the processor executes instructions, but the interrupt condition is not readable and the interrupt routine has not started.



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**8-bit AVR<sup>®</sup>**  
**Microcontroller**  
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**ATtiny11**  
**Rev. D**  
**Errata Sheet**

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